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Commentary

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Improving The Reliability Of Silicon Carbide Power Devices

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Silicon carbide (SiC) devices offer many advantages, especially in power-conversion circuits for applications where efficiency is at a premium. These include solar inverters and electric vehicles, which may also be expected to remain in service for decades. For these applications, a combination of very high efficiency and long-term reliability is essential.

The challenge in deploying SiC in such applications is that the technology is at an earlier stage of development than silicon. This means that the best ways of deploying SiC are still being explored, and that some failure modes unique to SiC devices still need to be better understood and more effectively mitigated. Infineon has been working on these issues for years and so has the insights and experience necessary to both help customers deploy SiC devices to their advantage, and to understand and mitigate their failure mechanisms to ensure the necessary reliability.

Why Do We Care About SiC?

SiC is a wide-bandgap semiconductor, which means it takes more energy to promote an electron from the material's valence band to its conduction band than it would in silicon. This enables SiC devices to operate at internal electric fields at which silicon devices would fail and to switch higher voltages at higher frequencies than would be possible in silicon, while reducing cooling needs. These characteristics broaden designers' options, as well as make it possible to simplify some established circuit topologies.

However, the higher electric field strengths formed within SiC devices do stress the material itself and its surroundings, so it has its own set of challenges. MOSFET devices in SiC exhibit different tunneling barriers for electrons and holes, increasing the likelihood of hot carriers entering the sensitive gate oxide. The wider bandgap also increases the likelihood of interface defects in the forbidden gap between its conduction and valence bands, potentially altering its electrical characteristics. Carbon oxidation products created during gate formation, such as carbon monoxide and carbon dioxide, can also be responsible for additional charged centers that change the device's electrical characteristics.

SiC is also a very stiff material, and this limits its ability to take up and release mechanical stresses caused by thermal cycling and power cycling. If this issue isn't properly addressed, it can cause further long-term damage, especially at physical interfaces between the different layers of the device.

SiC device performance enables new operating modes never tested in silicon. SiC devices can handle switching rates (dV/dt) at 1 kV that silicon devices see typically at 50 V. The promise here is of much more efficient high-power conversion circuitry: the challenge is that this is uncharted territory, a new operating mode that has yet to be fully explored for its obvious advantages and potential drawbacks.

As is so often the case in design, addressing these issues means making a series of tradeoffs. For example, the defectivity of SiC gate oxides is 10,000 times that of such oxides in silicon devices. We know that thickening the gate oxide aids proper screening to drop down defect density levels close to the silicon status (a good thing), but at the cost of higher resistance (a bad thing). However, it is known that device reliability increases exponentially with gate-oxide thickness due to the obtainable screening efficiency, while resistance only increases linearly. We choose, therefore, to gain a lot of reliability by thickening the gate oxide at the cost of a lesser gain in its resistance.

Another novel behavior that we need to address in SiC devices is the way that threshold voltages, and hence device resistance, can alter over time. There are three mechanisms involved here. The first is reversible threshold voltage hysteresis, not being relevant in the application with respect to long-term stability. The second is a more permanent shift in threshold voltage, caused by bias temperature instability. And the third is a product of switching, for which we provide an application note[1] that encourages designers to avoid this effect by ensuring their designs stay within our defined operating parameters.

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SiC MOSFETs may also suffer from defects when operated in bipolar mode. Used in this way, electron/hole recombination can accelerate the propagation of stacking faults in the SiC material. The result is an increase in $R_{DS(ON)}$ and V_{SD} over the device's lifetime (which saturates eventually).

Our approach to ensuring our customers get good devices is threefold. First, we have implemented effective measures to reduce density of defects being responsible for the growth of stacking faults in the crystal lattice. Next, we have used device concepts which avoid electron/hole recombination at stacking faults so that they don't propagate. And finally to be really on the safe side, we screen them so that we know that that supplied devices are free of defects leading to drift effect violating the datasheet limits over the operational lifetime.

Our experience with SiC devices, which has allowed us to understand their properties and mitigate some of their negative characteristics, has also made us realize that we need new ways of characterizing them. This is especially true for applications such as solar power conversion and electric vehicles, as mentioned earlier, where devices may be expected to operate for many years.

For example, we apply a series of tests to our SiC devices including a high temperature reverse bias test at 1200-V V_{DS}, 175°C and 0-V V_{GS} for 2000 hr. We run a 1000-hr high-temperature gate stress test with devices that have already been short-circuited ten times. And for our power modules, testing is extended to long-term (ex. 120 day) newly developed humidity and temperature cycling while the device is being switched at kilohertz rates.

At Infineon, we're also testing devices beyond levels required by industry standards. For example, the automotive industry has traditionally defined the AEC-Q101 standard as a way of ensuring the quality of components used in cars. The standard defines a "mission profile" for electric vehicle driving and charging, in other words, how long a vehicle will operate at various voltages in each scenario throughout its lifetime.

We're running tests to mimic these usage profiles, and adding more operating voltages and temperatures, new scenarios for climatic tests, and longer high-temperature reverse-bias tests. We're also doing more testing at high voltages and incorporating transients and overshoot signals. All of this because we think that while the AEC Q101 standard is necessary for the automotive industry, it is no longer sufficient in the age of SiC devices.

We're taking a similar approach to testing packaged devices because we have found that devices that meet the requirements of AEC-Q101 can still fail our high-temperature, high-humidity, high-voltage reverse-bias tests (see the figure). The same is true for the delamination between chips and the mold compounds during temperature cycling of packaged discrete devices.

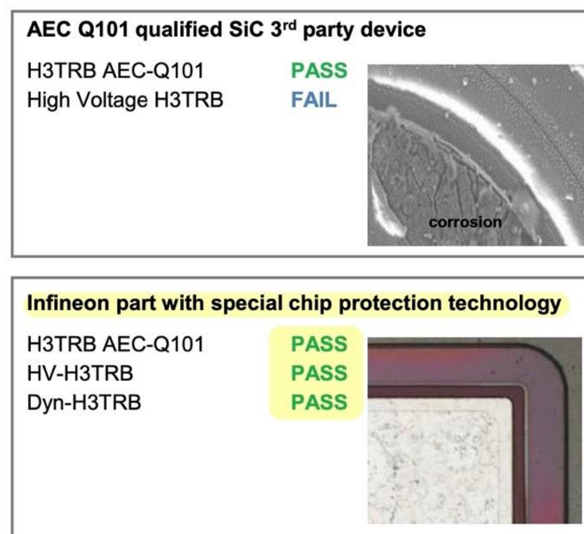

Figure. Infineon performs environmental stress testing of its SiC devices at the wafer level beyond the requirements of AEC Q101.

SiC devices offer great promise for improving the efficiency of power conversion in many market segments, but the technology is relatively new, and we are still developing our understanding of the best ways to use it—and the ways in which it fails. At the same time, customers are concerned about the long-term stability and

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reliability of all switching devices, especially if they're for applications that are expected to operate for a relatively long time.

Infineon knows this and has been developing its understanding and experience with the technology for many years, enabling us to design and make devices that minimize SiC intrinsic issues, while also mitigating their effects through extensive device screening, targeted technology improvement programs, and qualification to levels beyond industry standards. This is all done to ensure that SiC device technology can now deliver as much performance and reliability in practice as it promises in theory.[2]

References

1. "Guidelines for CoolSiC MOSFET gate drive voltage window," Infineon application note AN2018-09, 2022.

2. Learn more about SiC

About The Author

Peter Friedrichs has worked in the power semiconductor industry for over 25 years and currently serves as vice president SiC at Infineon Technologies. Previously, he was the the managing director of SiCED, a joint venture of Siemens and Infineon, which was later integrated within Infineon. Prior to that he was involved in the development of power devices on SiC at Siemens.

Peter holds numerous patents in the field of SiC power devices and technology, and has authored or co-authored more than 50 scientific papers and conference contributions. He received his Dipl.-Ing. in microelectronics from the Technical University of Bratislava and his Ph.D from the the Fraunhofer Institut FhG-IIS-B in Erlangen. His focus area of expertise was the physics of the MOS interface in SiC. Peter also holds a Dipl.-Wirt.-Ing. from the University of Hagen.

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