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System-In-Package Incorporates Complete Power System For Advanced SoC

[Octavo Systems](#), a provider of mass market system-in-package (SiP) solutions, has introduced the OSDZU3, a family of SiP devices based on the AMD Xilinx Zynq UltraScale+ MPSoC Architecture. The OSDZU3 provides the benefits of system-in-package while delivering the performance and flexibility expected from the Zynq UltraScale+ architecture. The OSDZU3 integrates the AMD-Xilinx ZU3 Zynq UltraScale+ MPSoC, with 2 GB (16 Gb) of LPDDR4, power management and other required components in a single BGA package (Figs. 1 and 2).

According to the company, the OSDZU3 is about 60% smaller than an equivalent system design with discrete components. "The integration not only makes the OSDZU3 perfect for anybody concerned about the size, weight, and power (SWaP) of their product, it is also ideal for anybody looking to move quickly through their design," says Greg Sheridan, VP strategy and marketing at Octavo Systems. "Removing the need to design complicated power systems or DDR has saved our customers upwards of 9 months of design."

The company asserts that the OSDZU3 enables the lowest cost of ownership. In addition to the reduction in engineering design time, the OSDZU3 reduces the number of layers required for the customer's board (which reduces PCB costs), simplifies manufacturing (pick and place is reduced from a few hundred components to 1) and reduces supply chain management. Nevertheless, from strictly a BOM price point of view, the OSDZU3 costs about 15% to 20% more than the BOM for a discrete implementation, says the vendor.

In terms of power system design, using the OSDZU3 saves the customer from having to route the 13 power rails required by the Zynq UltraScale+ MPSoC. Instead the customer only needs to route a single rail.

The SiP provides access to all the interfaces and features on the ZU3. The 1-mm pitch 600-pin ball map provides access to every I/O on the ZU3 in just two PCB layers using low-cost design rules. Additionally, the power system also allows the designer to leverage all the power modes the ZU3 supports.

"System-level solutions are increasingly important to our customers, as they seek to deploy cutting-edge embedded computing and machine learning capabilities within increasingly compressed development timeframes," said Hanneke Krekels, vice president of Core Vertical Markets, Adaptive & Embedded Computing Group, AMD. "In-line with these objectives, we have worked closely with Octavo Systems to bring the first System-in-Package solution based on the powerful Zynq UltraScale+ MPSoC. This offering enables our users to accelerate innovation and simplify system design for the most size-constrained applications."

The OSDZU3 is compatible with the AMD-Xilinx development tools, Xilinx Vivado Design Suite and Xilinx Vitis unified software platform. Octavo Systems worked closely with DesignLinx, an AMD-Xilinx Premier Design Service Partner, to develop the base software platform needed to ensure the SiP integrates into the standard AMD-Xilinx tool flow.

Along with the OSDZU3, Octavo Systems will be releasing the OSDZU3-REF reference platform. It features popular interfaces like USB-C, USB 3.0, SATA Host, 1Gb Ethernet, and an FMC LP Connector. It also supports displays through Display Port and a LVDS touch display connector. It will ship with a PetaLinux Distribution and demos that are also developed by DesignLinx.

Octavo Systems has Engineering Samples available today through their Beta program. Design engineers who are interested in gaining access to the Beta program can contact their local Avnet, Octavo Systems, or AMD-Xilinx sales representative.

The reference platform will be available to the general market in Q3 CY2022 and the OSDZU3 will be in production by the end of CY2022. For more information, see the OSDZU3 [page](#) and the OSDZU3-REF reference platform [page](#).

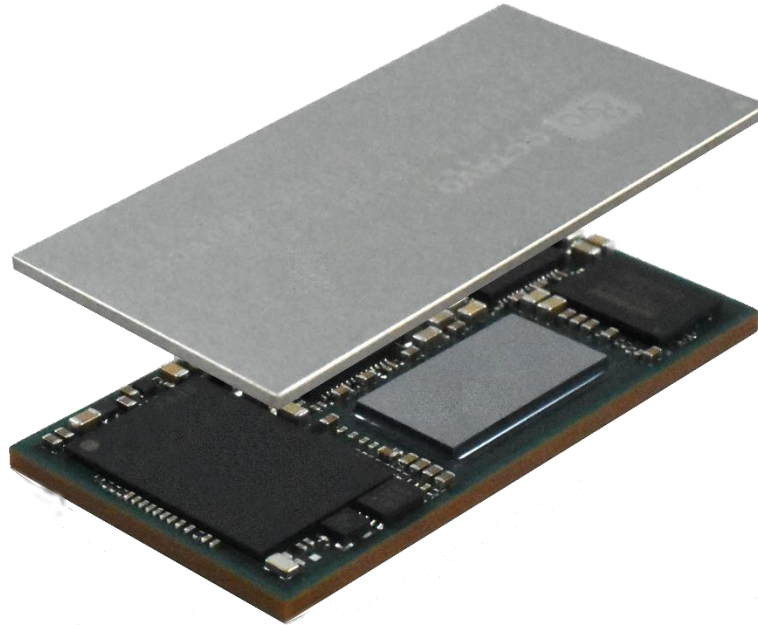


Fig. 1. The OSDZU3 leverages IC manufacturing technology to integrate an AMD-Xilinx Zynq UltraScale+ MPSoC ZU3, a complete and flexible power system, an LPDDR4, an EEPROM, a QSPI interface, MEMS oscillators and over one hundred passives—all in a single 20.5-mm x 40-mm BGA.

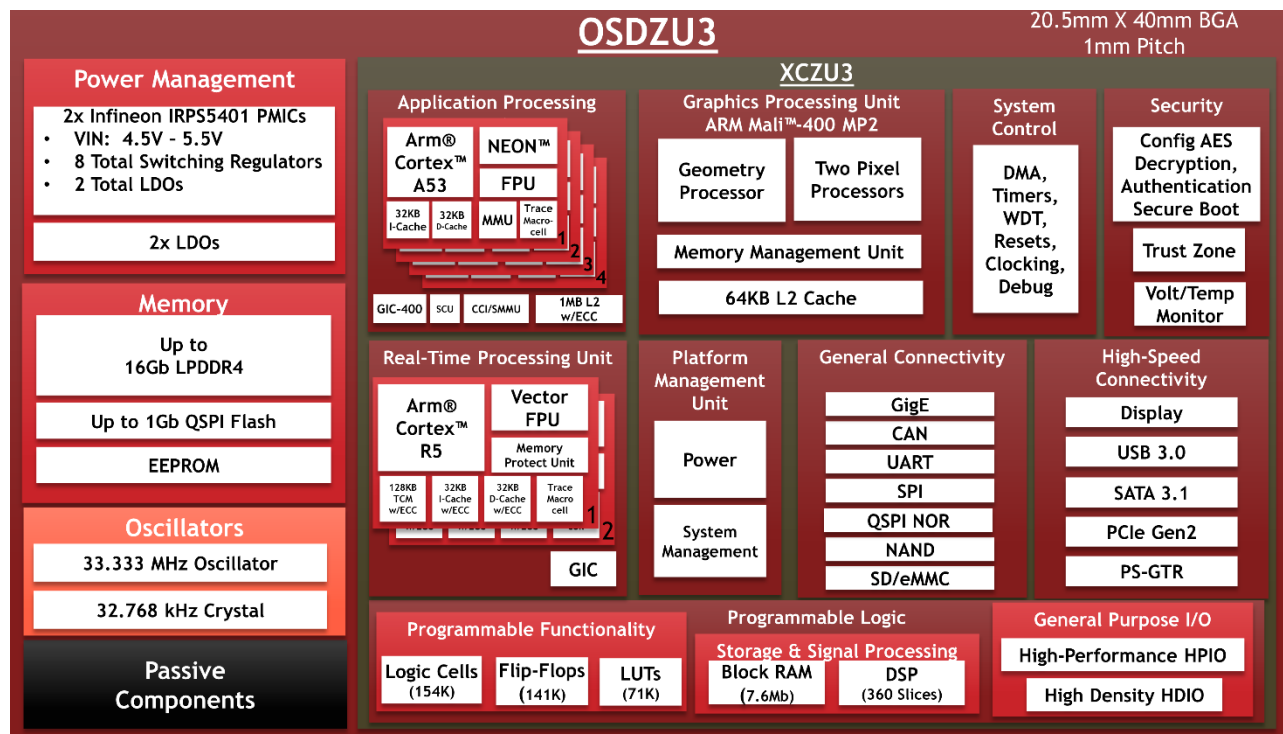


Fig. 2. The OSDZU3 system in package is described as the the fastest and most flexible way to develop a system around the AMD Xilinx Zynq UltraScale+ MPSoC. It allows you to harness the performance of the ZU3 MPSoC, while removing the complexities without sacrificing flexibility. It saves "upwards of 9 months of design" time by eliminating the need to design a complex power system or DDR, according to Greg Sheridan, VP strategy and marketing at Octavo Systems.