1200-V SiC FETs Ease Design Optimization

UnitedSiC (now Qorvo) has expanded its 1200-V product family, extending its Gen 4 SiC FET technology to higher-voltage applications. Six new products in the new UF4C/SC series ranging from 23 mΩ to 70 mΩ are now available with 23-mΩ and 30-mΩ SiC FETs offered in the TO247-4L (kelvin connected) package and 53-mΩ and 70-mΩ SiC FETs offered in both TO247-4L and TO247-3L packages.

The part numbers for these 23-, 30-, 53- and 70- mΩ devices are UF4SC120023K4S, UF4SC120030K4S, UF4C120053K4S/K3S and UF4C120070K4S/K3S, respectively. As with all of the company's SiC FETs, these are cascode devices combining a SiC JFET with a low-voltage silicon MOSFET.

These are the company's first Gen 4 SiC FETs at 1200 V. The company previously introduced 750-V devices in this family (See "What We Missed At APEC [2020]: Silicon Carbide Marches On And Other Power Product News".) According to Anup Bhalla, VP of engineering at UnitedSiC, the six new 1200-V SiC FETs also fill in the gap between the previously introduced 16-mΩ and 80-mΩ 1200-V SiC FETs—the company's Gen 3 devices—enabling customers to make more-optimized tradeoffs of performance versus cost. (For more on the Gen 3 SiC FETs, see "SiC FETs Lower On-Resistance To Less Than 10 mΩ".)

These SiC FETs offer superior performance and are described as excellent options for the growing EV market evolution towards 800-V on-board chargers (OBCs) and dc-dc converters. As with previous generations, the new FETs are also well suited for industrial battery chargers and power supplies, PV converters, UPS and various other power conversion applications.

The company says these devices offer industry best figures-of-merit (FOMs) in several categories. These include lowest $R_{DS(ON)}$ x area, $R_{DS(ON)}$ x E_{oss}, $R_{DS(ON)}$ x $C_{oss,(tr)}$ and $R_{DS(ON)}$ x Q_g.

As with the rest of Gen 4 portfolio, the 1200-V FETs can be easily driven with a 0- to 12-V or 0-to 15-V gate drive. With a ±20-V $V_{GS,Max}$ and a high threshold voltage (4.8 V), these SiC FETs offer plenty of gate voltage design and noise margin and are compatible with Si or SiC gate drive voltages. The 1200-V FETs offer an excellent integral diode, with superior forward voltage (1.0 to 1.5 V typically) and low reverse recovery charge (Q_{rr}).

To take full benefit of ultra-low specific on-resistance, the 1200-V SiC FETs employ an advanced Ag-sinter die attach process that gives them superior thermal performance versus solder, says the vendor. The devices maintain good power handling capability allowed by their best in-class (according to the vendor) thermal resistance, R_{thj-c} while achieving a die shrink with lower capacitance and reduced switching losses. When compared with competing SiC MOSFETs, the Gen 4 1200-V SiC FETs are said to offer a 26% to 60% reduction in thermal resistance. These benefits versus existing SiC MOSFETs are depicted in Fig. 1.

Fig. 2 shows the FoMs for power handling ($R_{th,j-c}$), hard-switching ($R_{DS(on)}$ x E_{oss}) and soft-switching ($R_{DS(on)}$ x $C_{oss,(tr)}$), and $R_{DS(on)}$ x Q_g when normalized to the Gen 4 1200-V SiC FETs. Superior performance of each parameter in the spider chart is represented by a lower value. One can see that the 1200V Gen4 SiC FETs offer performance benefits in both hard switching and soft switching circuits at both 25°C and at elevated temperature (125°C). Compared to previous generation SiC FETs, the new devices offer up to 40% lower $R_{DS(on)}$ for a given die area, 37% lower 25°C $R_{DS(ON)}$ x E_{oss}, and 54% lower 25°C $R_{DS(ON)}$ x $C_{oss,(tr)}$, according to the vendor.

The six 1200-V SiC FETs are available in the UnitedSiC (now Qorvo) free online design calculator tool FET-Jet Calculator, which can be used to evaluate device losses, converter efficiency, temperature rise, and identify optimal drive conditions. Using the FET-Jet Calculator tool, it is clear that the 23-mΩ (UF4SC120023K4S) and 30-mΩ (UF4SC120030K4S) FETs are excellent options for the active front end of 800-V bus on-board charger (OBC) applications.

In the 11-kW OBC front end design example shown in Fig. 3a, the UF4SC120030K4S is able to reduce losses (to 37 W per FET), achieve an excellent 98% semiconductor efficiency and run cooler (T_j = 115°C), all with a reduced die size. The design shown assumes a hard-switched frequency of 150 kHz and a heatsink temperature of T_{HS}=80°C allowing users to achieve high power density.

The 1200-V SiC FET series also offers choices for the isolated dc-dc converter stage of the OBC where the Gen 4 FETs' low conduction loss, low diode forward drop, low driver losses (low V_g, low Q_g) and low $R_{DS(on)}$ x $C_{oss,(tr)}$ are well suited to the high-frequency, soft-switching topologies used in this stage.

An 11-kW, 800-V full-bridge CLLC design example is shown in Fig. 3b with 1200-V SiC FETs in each of the primary-side switch positions. The assumed operating frequency is 200 kHz and the heat sink temperature is again T_{HS} = 80°C. The performance summary table as predicted with the FET-Jet Calculator shows the benefit of the Gen4 1200-V SiC FETs versus the company's Gen 3 devices.

With a similar die size, the UF4C120053K4S/K3S offer lower losses and excellent semiconductor efficiency (99.5%) and run cooler (T_j < 100°C). The cost-effective UF4C120070K4S/K3S are also attractive cost/performance solutions, offering good efficiency (99.4%) with slightly higher losses, according to the company.

For more information, see theGen 4 SiC FETs page.

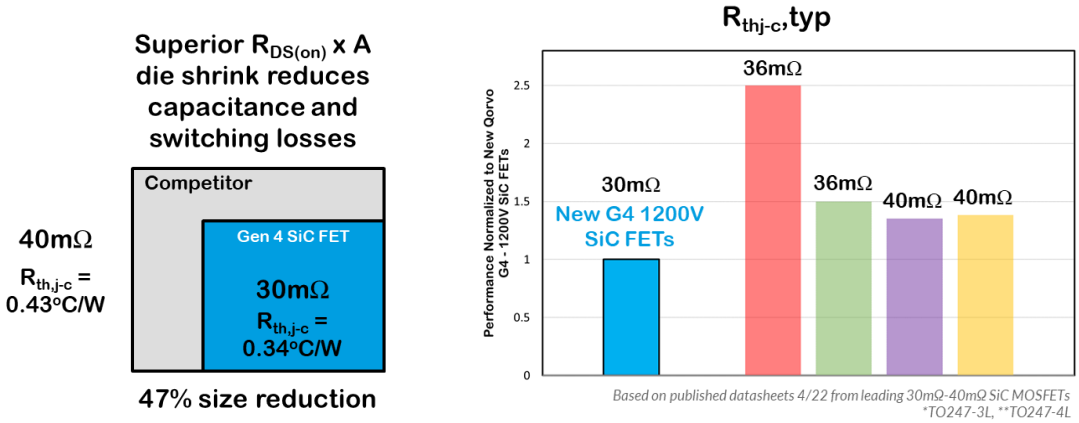


Fig. 1. The 1200-V Gen 4 SiC FETs achieve better thermal performance with advanced Ag-sintering technology. Here the junction-to-case thermal performance of one of these devices is compared with that of competing SiC MOSFETs.

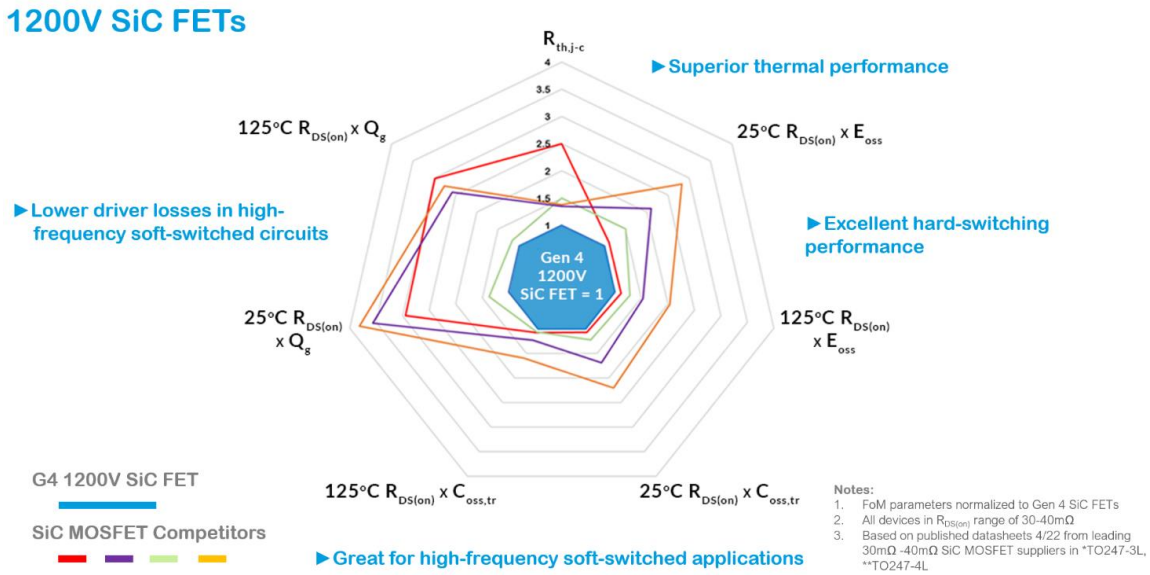
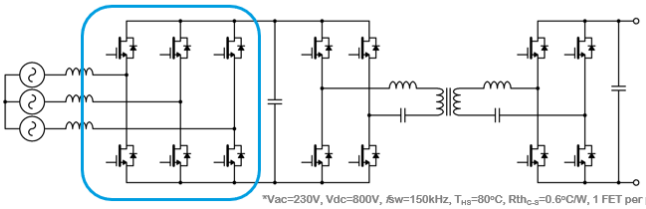


Fig. 2. Comparing FoMs of the 1200-V Gen 4 SiC FETs with competing 1200-V SiC MOSFETs.

Automotive OBC – 11kW 3-phase front end

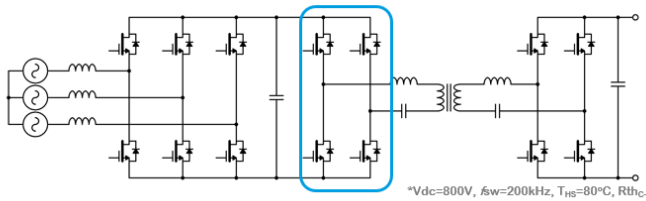


SiC FET hard switching
Offers excellent cost/performance options for OBC FE

	UF3C120040K4S	UF4C120030K4S	Gen 4 Benefits
Generation	Gen 3	Gen 4	Reduced die size ↓
Losses per FET	44.3W	37W	Reduced losses ↓
Semiconductor efficiency	97.6% 88.6W/phase	98.0% 74W/phase	Improved efficiency ↑
Tj	119°C	115°C	Runs cooler ↓

(a)

Automotive OBC – 11kW Full-bridge CLLC



SiC FET soft switching
Offers excellent cost/performance options for isolated DC/DC

	UF3C120080K4S	UF4C120053K4S	Gen 4 Benefits
Generation	Gen 3	Gen 4	Similar die size
Losses per FET	17.6W	14.1W	Reduced losses ↓
Semiconductor efficiency	99.4% 70.4W	99.5% 56.4W	Improved efficiency ↑
Tj	101°C	97°C	Runs cooler ↓

(b)

Fig. 3. An 11-kW OBC example using Gen 4 UF4SC120030K4S SiC FETs in the front end design (a) and Gen 4 UF4C120053K4S SiC FETs in the full-bridge CLLC design (b).