IC Simplifies Analog Control Of The Totem-Pole PFC Stage

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The totem-pole power factor correction (TPFFC) circuit was described in 1995[1] as a solution to regain the precious percent of efficiency lost in the front-end bridge of high-power pre-converters. At the time of the publication, silicon MOSFETs were available to implement this circuit but their body diode characteristics made them impractical for switching operation in high-frequency converters operated in continuous conduction mode (CCM). The losses would have been excessive, negating the intended efficiency benefit of the TPPFC.

The situation has changed with the introduction of wide-bandgap semiconductors such as silicon-carbide (SiC) and gallium-nitride (GaN) power switches which are now available in mass production. Not only do these elements switch at a very high speed but they also allow—in the case of the GaN devices—current conduction in both directions without the penalty of reverse-recovery losses. The TPPFC architecture offers a perfect fit for these semiconductors, especially in high-density projects.

TPPFC solutions are currently implemented using digital control carried out by a microcontroller. However, analog solutions are now emerging, such as the NCP1680 from onsemi which brings a fully integrated product for operating a borderline conduction mode (BCM) TPPFC. This circuit lends itself well to powering converters up to a level of 300 W for a universal mains application (85 to 265 V ac), while incorporating the benefits of higher efficiency and increased power density which the TPPFC supports.

The Two Sides Of The Input Line

An active PFC stage can be implemented in different ways, but the boost converter dominates the market with variations such as the bridgeless and totem-pole approaches. A traditional structure associates a low-frequency bridge rectifier with a pair of power switches like a MOSFET and a diode for the most common circuits. The front-end bridge operates at the line input frequency—50 Hz or 60 Hz—while the power switch and the diode chop the current at a higher frequency, typically at several tens of kilohertz or beyond with modern components. Fig. 1 shows the typical simplified configuration of a boost converter regardless of its operating mode.

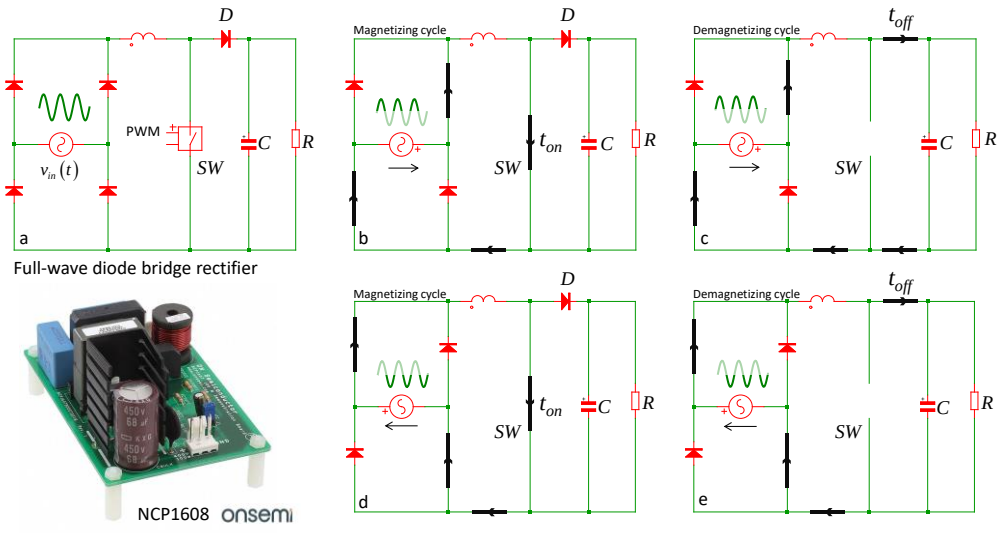

Fig. 1. In a classic PFC stage with a bridge rectifier on the input, two diodes are always conducting and can contribute a significant power budget.

As the input sine wave changes polarity every 10 ms for a 50-Hz line frequency, separate pairs of active front-end diodes are alternately biased or blocked. Two diodes always see the average low-frequency input current

for half of the line cycle, neglecting the high-frequency ripple current. As such, along a 10-ms cycle, the bridge permanently dissipates an average power of

$$P_d \approx 2V_f I_{d,avg} \quad (1)$$

with an average diode current equal to

$$I_{F,avg} = \frac{2}{\pi}\frac{\sqrt{2}P_{out}}{V_{ac,LL}\eta} \quad (2)$$

Considering a 300-W PFC featuring a 100% efficiency for the dc-dc portion and supplied from a 90-V rms input source, the power dissipated by the bridge would then amount to roughly 5 W, reducing the efficiency by 1.7%.

In the embodiment of Fig. 1, the front-end diodes rectify the input mains and provide a strictly positive bias to the switch which performs the chopping action while the diode D operates in freewheel mode. In other words, regardless of the input line polarity, the input and return currents are routed by the diode bridge and the control circuit actuating the power switch does not care about the line polarity.

Removing The Diode Bridge

The simple calculation we performed shows that regardless of the improvements brought to the dc-dc PFC stage, the diode bridge will always increase the overall loss budget. As detailed in reference 2, many techniques have been explored to remove the rectifying diodes and improve efficiency. A bridgeless PFC was described in 1983[3] and appears in Fig. 2.

In this structure, two MOSFETs are referenced to ground and alternatively play a switching role at high or low frequency. When the polarity of the line input is positive, Q_1 and D_1 operate at high frequency as in a classic boost structure while the body diode of Q_2 routes the current back to the source as the low-side diode in the bridge would. D_2, in this mode, is blocked. When the source polarity reverses, Q_2 and D_2 now switch at high frequency while Q_1 routes the current back to the source via its body diode. D_1 has become blocked.

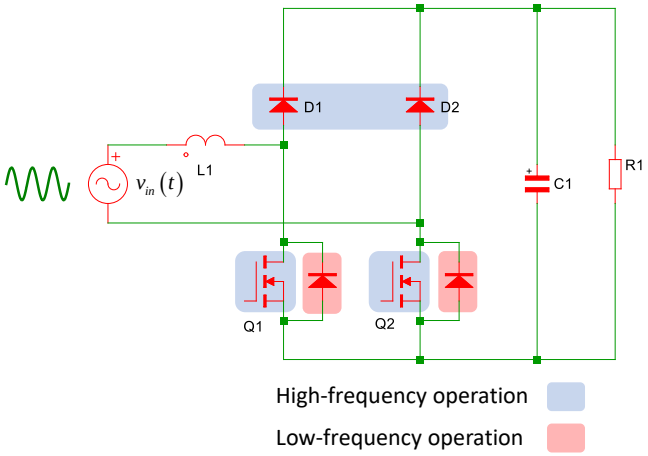

Fig. 2. This bridgeless PFC removes one low-frequency diode but degrades the common-mode noise signature of the converter.

In this approach, a single low-frequency diode is now conducting at a time—the body diode of Q_1 or Q_2—and brings the traditional bridge conduction losses down by a factor of two. The two MOSFETs in this original

embodiment share a common drive signal and no specific control logic is necessary to detect which line polarity is active.

However, the EMI signature raises a point of note. In the PFC circuit illustrated in Fig. 1, the output ground is always referenced with or attached to the input source via one of the conducting low-side diodes of the bridge. The situation changes in the approach illustrated in Fig. 2 since this ground-referenced output is ensured during the positive cycle only—when Q_2's body diode conducts—while it pulses to a high-frequency voltage during the negative cycle.

This configuration, in which the input source connection is not permanently tied to a quiet point—ground or V_{out}—significantly degrades the common-mode performance of the converter. This issue has significantly hampered the adoption of this configuration. Solutions to overcome this issue are presented in reference 2 with a possible practical implementation described in reference 4.

The Totem-Pole PFC Architecture

The TPPFC architecture elegantly solves the common-mode noise issue by rearranging the two active switches in a half-bridge configuration together with two low-frequency diodes. These diodes, as we will later see, can be advantageously replaced by synchronous switches, pushing the overall efficiency to, arguably, the highest possible level.

The TPPFC application circuit proposed in Fig. 3 represents the entire structure with its active phases illustrated on the right. Two switching paths are highlighted. The first, often designated as the *fast leg*, through the left pair of switches, operates at high frequency and performs the classic boost work.

During this mode, one diode of the so-called *slow leg* routes the current back to the source and permanently conducts for half of the mains period. You can immediately see that when D_3 or D_4 is conducting, the source low-side connecting terminal is always referenced to a quiet point, respectively V_{out} or ground. Operating in this way, the TPPFC offers an improved noise signature compared to the version referenced previously in Fig. 2.

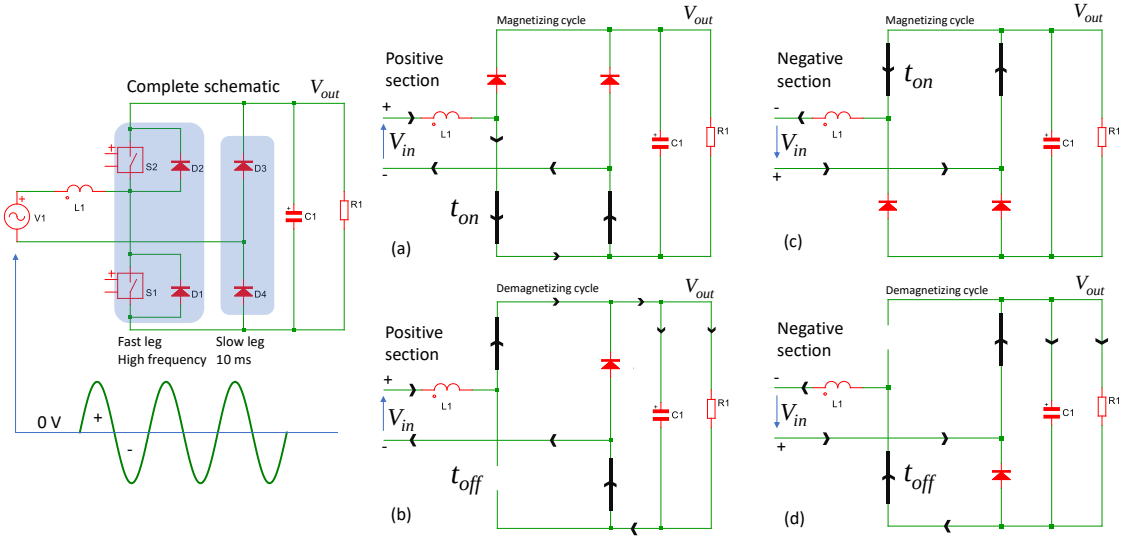

Fig. 3. The totem-pole PFC circuit uses a half-bridge configuration together with two low-frequency diodes.

Unlike in the previous approach where the switching pattern ignores the line polarity, the TPPFC circuit requires management of the line polarity as illustrated in Fig. 4. This is because the fast leg power components will be alternately either a switching transistor or a synchronous rectifier depending on the input polarity.

For a positive input voltage depicted in Fig. 3, parts a and b, the left-side inductor terminal is positive. S_1 plays the role of the high-frequency switching transistor during the on-time (the magnetizing cycle for L_1) while D_2 conducts during the remaining duration of the switching period (the demagnetizing cycle for L_1).

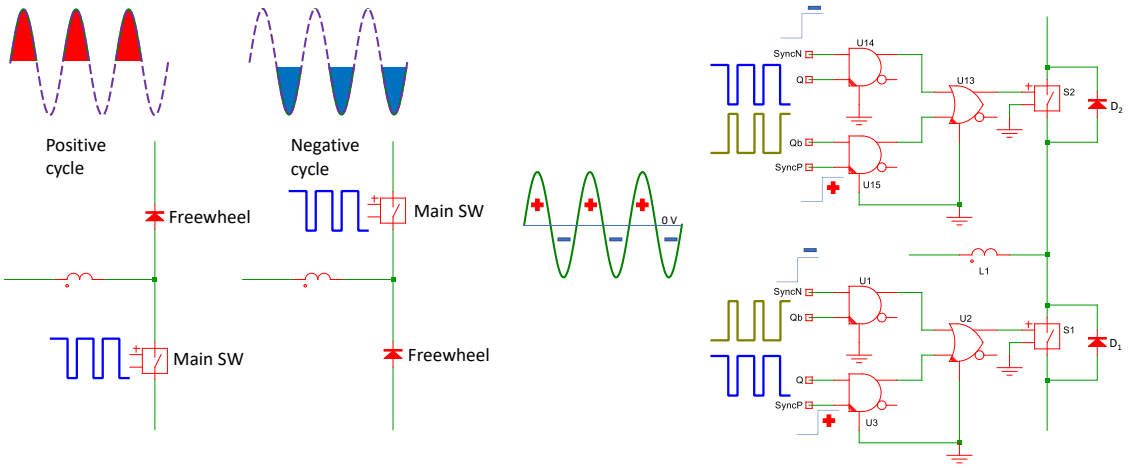

Fig. 4. Input line polarity management is important to ensure correct operation of the TPPFC structure. On the left, the roles of the fast and slow leg components are defined for the two halves of the line cycle. On the right, a possible implementation is shown for controlling the two switches in the fast leg.

To reduce losses, S_2 is then operated in zero-voltage switching (ZVS) conditions bringing synchronous rectification to the conversion process. Diode D_4 permanently ensures current return to the source and fixes the input source terminal to the output ground.

When the line polarity changes, meaning that the junction of D_3 and D_4 is now positive as shown in Fig. 3 parts c and d, S_2 becomes a full-time switching transistor while D_1 now operates as the catch diode with S_1 performing ZVS synchronous rectification. Diode D_3 now conducts the return of the current and fixes the low-side terminal of the source to V_{out}, which is a non-pulsating point.

In this operating mode, the supporting circuitry must permanently observe the input line cycle and instruct the fast components of their role: switching transistor or synchronous rectifier. A potential implementation of this controlling function is shown on the right side of Fig. 4.

Engineers at onsemi have experimented with different types of transistors to perform the switching functions described. For the fast leg, even considering a converter permanently operating in discontinuous mode—where the diode spontaneously blocks—the charge stored in the body diode of superjunction (SJ) MOSFETs remains significant and affects efficiency especially at high switching frequencies. Conversely, GaN transistors conduct in the third quadrant with a significant voltage drop. But, since no charge needs to be recovered, turn-off losses are minimum.

When comparing losses in a 300-W application, the efficiency with GaN transistors reaches 98% in low-line conditions (115 V rms) while it reduces to 96.6% with SJ MOSFETs in similar conditions. At high line or 230 V rms, the difference is smaller as peak currents at turn-off reduce, but, GaN still leads the race with an efficiency above 98%, which is slightly above the SJ MOSFETs with an efficiency of 97.5%.

SiC MOSFETs could of course, be candidates for the fast-switching path but are probably overkill for a 300-W converter (they are typically employed in 2- to 3-kW applications.) For the slow leg, SJ MOSFETs can be selected as an alternative to diodes with suitable control circuitry to improve efficiency still further.

A Mixed-Signal Integrated Solution

Although additional dedicated circuitry is required to detect and manage the switching operation relative to the incoming polarity, any known boost control scheme can be employed in a TPPFC application. Onsemi has adopted a free-running borderline conduction mode for its ease of implementation in power applications up to 300 W or so. In this mode, the converter operates in voltage-mode control with a constant on-time whose value is adjusted depending on operating conditions.

This technique does not require the sensing of the input voltage but needs an auxiliary winding to synchronize the turn-on event with a valley occurrence. As such, the power inductor will require a few additional turns of wire to report the core flux activity to the controller.

A typical application circuit is proposed in Fig. 5. You can see the NCP1680 is supported by two half-bridge drivers: a high-speed driver, the NCP51820, controls the actuation of the fast-leg GaN transistors while a more general-purpose driver, the NCP51530, takes care of the low-frequency half-bridge. Both drivers implement a classic bootstrap technique to support high-side switch operation.

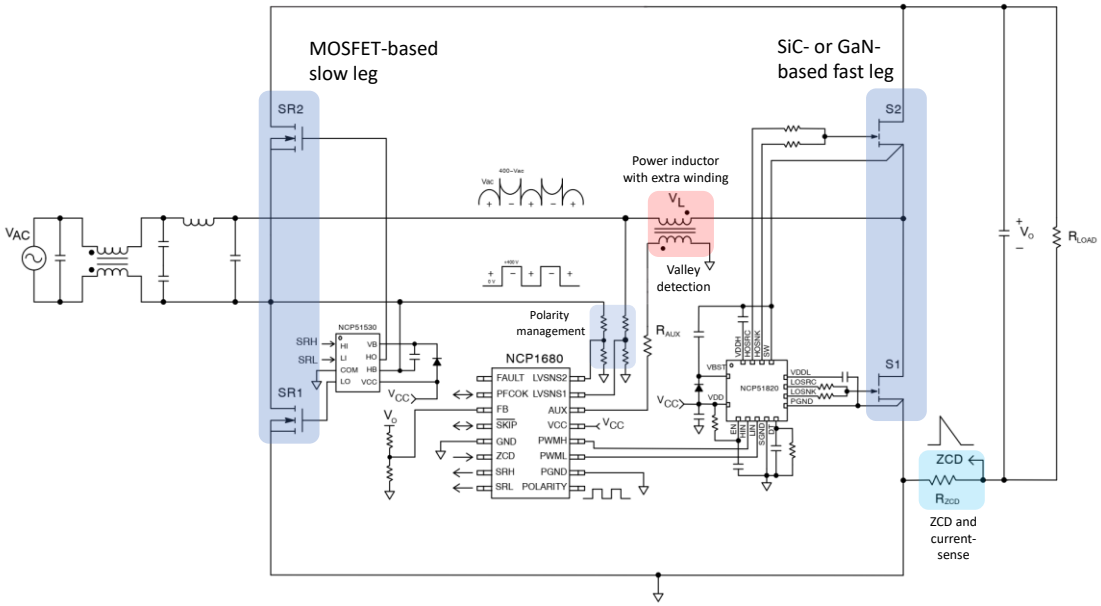

Fig. 5. The NCP1680 TTPFC controller uses a simple sense resistor for managing the instantaneous off-time current.

The NCP1680 monitors the input line voltage by implementing a differential-sensing arrangement around four resistors directly connected to the input mains. The controller knows what the active polarity is and activates the transistors accordingly: two SiC or GaN transistors in the fast leg and two MOSFETs in the slow leg (or two diodes in case you want to reduce the overall cost). Through these sensing inputs, the NCP1680 also controls other parameters pertinent to the grid operation.

For example, there's brown-out and line-sag protection. If the mains amplitude momentarily drops for a duration larger than 25 ms, the controller enters a soft-stop management scheme and auto-recovers when the line goes back to normal. If the line disappears for more than 650 ms, the controller considers it an on-going brown-out event and stops all switching pulses via a general reset. It remains turned off until the mains returns to normal and the part resumes operation through a fresh start-up sequence.

Besides input line amplitude monitoring, the controller circuit permanently verifies that the mains frequency remains within the expected range of 42 Hz to 72 Hz. If the grid frequency deviates from this range, the NCP1680 latches a fault and auto-recovers when the frequency returns within the range limits window for four consecutive correct transitions.

The NCP1680 also internally adjusts the compensation. When deriving the small-signal model of a PFC circuit operated in constant on-time, we can see that the control-to-output transfer function magnitude depends on the RMS amplitude of the input voltage. As such, considering a ratio of roughly 3 between both input extremes (85 to 265 V rms), the crossover frequency of the compensated loop gain can vary by up to a factor of 9 between low- and high-line conditions. By dynamically changing the mid-band gain in the internal compensator with respect to the line magnitude, the NCP1680 maintains a quasi-constant crossover frequency in step with the input range.

Finally, the controller adjusts settings to properly detect the state of the power inductor's core flux. The core flux activity is monitored by the classic method of using an auxiliary winding added to the power inductor. However, depending on the active line polarity, the waveform delivered by the auxiliary winding changes. The voltage swings around –Vin or (Vout–Vin) when observed with respect to the NCP1680 ground. To cope with this unique challenge, the controller internally toggles the various thresholds to detect the demagnetization state in relation to the mains polarity. By adding a small delay in the detection path, the part supports near-zero-voltage switching operation, significantly improving overall efficiency.

Beyond controlling parameters relating to grid operation, a PFC controller must implement a current limit to protect the transistors against damaging current levels. The first limit is given by the maximum on-time which sets the maximum power the PFC can transmit at low-line. There are two options here, 10.2 µs with the NCP1680AB and 17.2 µs with the NCP1680AA.

However, some overpower protection or OPP is needed to alter this maximum value as the mains input increases. The NCP1680 implements a novel sensing scheme observing the current circulating in a shunt resistor during the off time. This resistor is conveniently located in the return path of the output capacitor and the load. Using this method, the voltage developed across the resistor is always positive regardless of the mains polarity and consistently provides an indication of the power level delivered to the load.

TPPFC Small-Signal Response

The compensation strategy of any converter starts with its control-to-output transfer function: if a stimulus is applied to its control pin—for instance the feedback input of the controller—how does the modulation signal propagate in the power stage to generate the response observed at the output? The relationship linking the response to the stimulus represents the transfer function we want (Fig. 6).

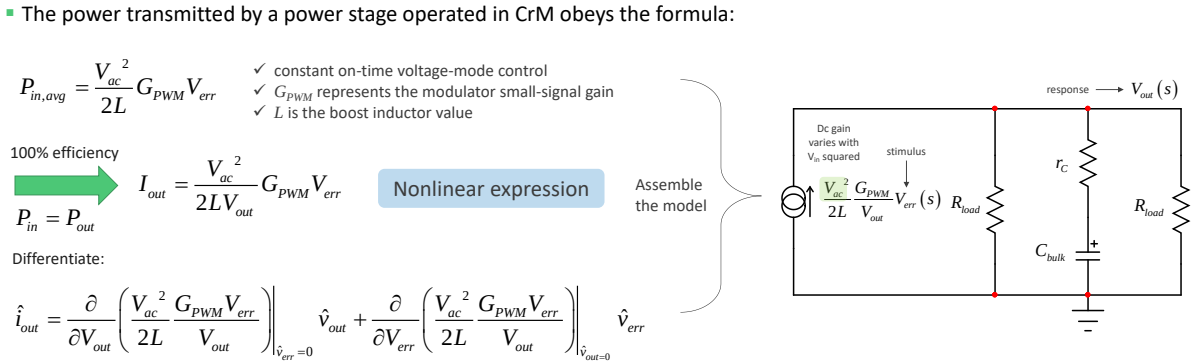

Fig. 6. The transfer function of the PFC stage is obtained by assembling a small-signal model.

From this transfer function and, depending on the closed-loop goals—crossover frequency and margins—a designer can infer a compensation strategy.

The easiest way to analytically obtain the transfer function characterizing a PFC power stage is to express the average power delivered to the load and then run a partial differentiation of the nonlinear equation. From the obtained coefficients, you build a small-signal model which quickly leads you to the transfer function you want.

It is then easy to check the response and see how the gain varies based on the nature of the load. Indeed, for a resistive load, the response is that of a first-order system featuring a low-frequency pole and a dc gain. If we neglect the output capacitor equivalent series resistance (ESR) which contributes a zero well beyond the low-frequency crossover point, then the transfer function as detailed in reference 6 is given by

$$H(s) = H_0 \frac{1+\frac{s}{\omega_z}}{1+\frac{s}{\omega_p}} \approx H_0 \frac{1}{1+\frac{s}{\omega_p}} \qquad (3)$$

If the load is a classic high-voltage dc-dc converter operated in closed-loop conditions, then the PFC sees a negative incremental resistance equal to $-R_{load}$ which cancels the small-signal resistance internal to the model. In this case, the above transfer function becomes that of a pure integrator

$$H(s) \approx \frac{1}{\frac{s}{\omega_{po}}} \qquad (4)$$

Fig. 7 illustrates the two typical frequency responses at the lowest input voltage and maximum power.

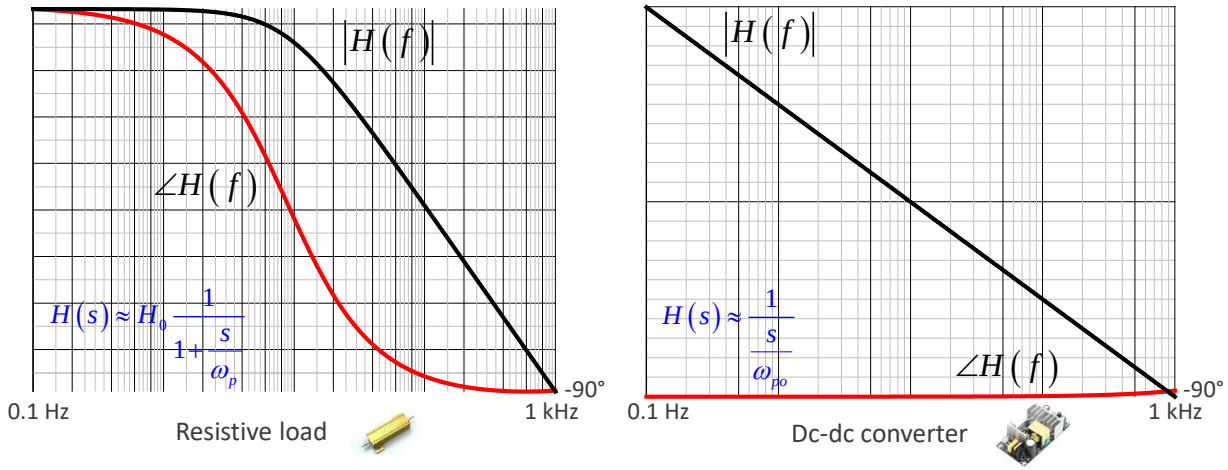

Fig. 7. The transfer function of the PFC stage changes depending on the nature of the load.

Compensation Strategy Of The TPPFC

From the above frequency responses, you can infer a compensation strategy for crossing over at a low frequency, well below the 100- or 120-Hz output ripple. For this particular application, onsemi has selected a type 2 compensator (a pole at the origin and a pole-zero pair) to boost the phase at 10 Hz while adjusting the mid-band gain as a function of the input voltage. This trick helps achieving a quasi-constant crossover frequency in low- or high-line conditions.

The filter is internal and digitally implemented with fixed coefficients. As a result, the user cannot change the values and it is important to verify the converter remains stable in various operating conditions. The filter is shown in Fig. 8 with its corresponding biquad structure.

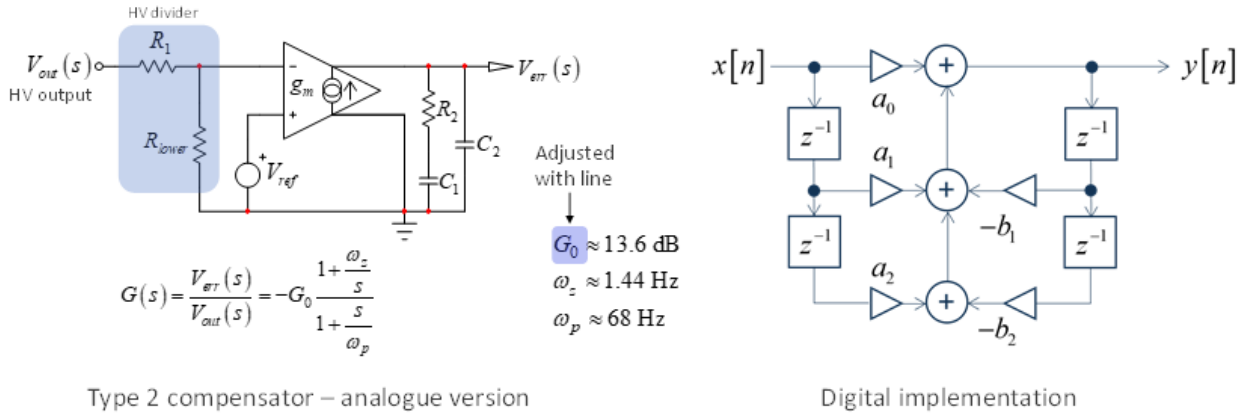

Fig. 8. The NCP1680 is internally compensated with the digital-equivalent of a type 2 compensator.

The typical response is given below and shows how the phase is boosted at the 10-Hz point. You can also see the mid-band gain changed from around 1 dB in high line and up to 13.6 dB in low line conditions, bringing a quasi-constant crossover frequency, independent of the input voltage.

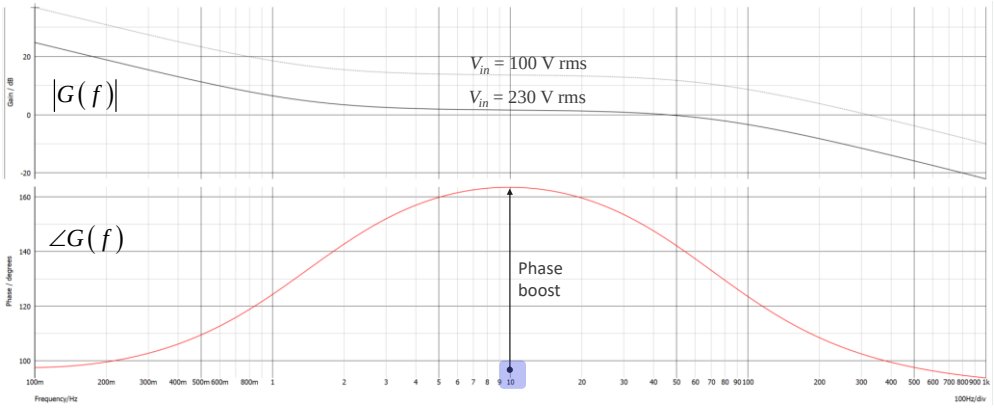

Fig. 9. The typical response of the internal type 2 compensator shows a phase boost centered at 10 Hz.

To efficiently reduce the ripple contribution to the error signal, a low-pass finite impulse response (FIR) filter is inserted in series with the output of the type 2 compensator. The frequency response of this filter depends on the sampling frequency which is set here at four times the mains frequency. The low-frequency pole is then placed at 50 Hz and a notch appears at exactly 100 Hz for a 50-Hz input frequency. For a U.S. mains frequency, the pole adjusts to 60 Hz while the notch now appears at 120 Hz. The response of this filter is given in Fig. 10 for a 200-Hz sampling frequency and confirms the notch precisely set at 100 Hz.

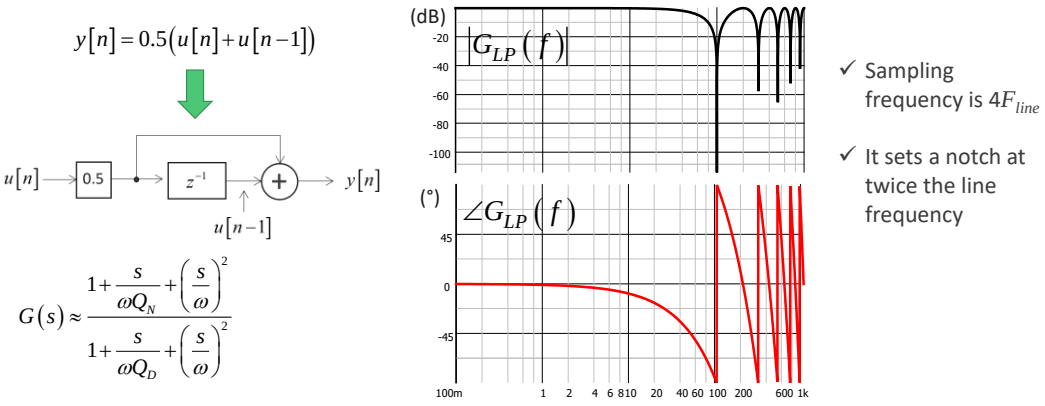

Fig. 10. A low-pass digital filter is added to reduce the output ripple contribution to the error voltage.

Testing The Loop Gain Transfer Function

Now that we have the exact transfer function implemented in the NCP1680, it is important to verify that it suits your design requirements and ensures stable operation in various load/line conditions. The best way to do this is to model the transfer function of the PFC stage via a Laplace equation, then feed the ac response from this stage to a digital filter.

While SIMPLIS can easily extract the ac response from a switching circuit, it requires a specific setup for a switching PFC converter fed by an ac source. For the sake of simplicity, I have used a simple automated SIMetrix template which uses delay lines for modeling z^{-1}. The digital filter receives a stimulus coming out from an equation in the Laplace-domain. The entire setup appears in Fig. 11 and you see the ac source applied to the left side of the circuit.

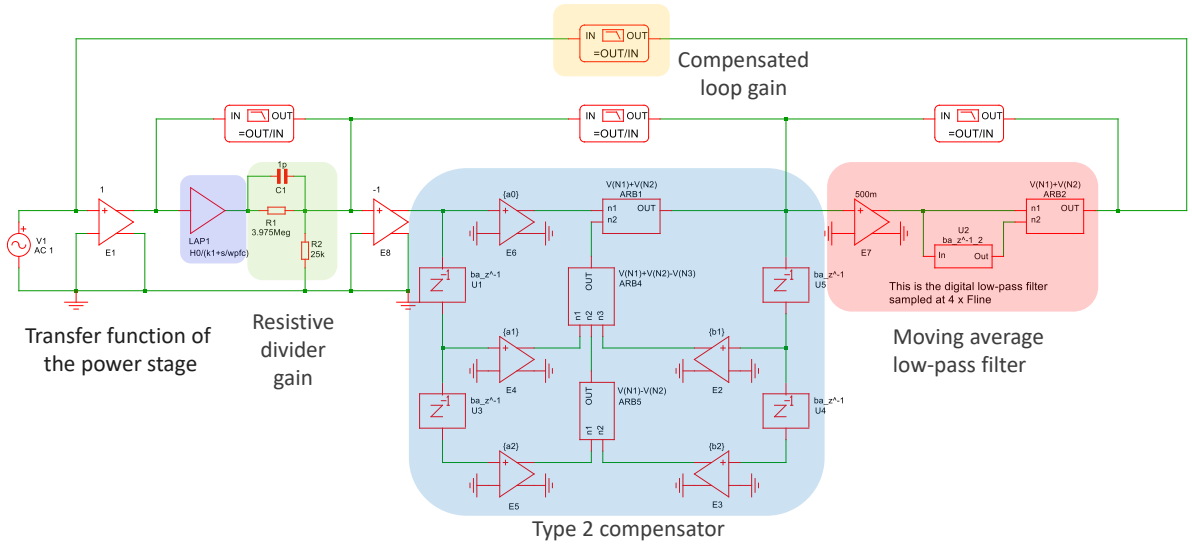

Fig. 11. SIMetrix offers an easy means to test the stability of the compensated TPPFC stage.

In this configuration, the coefficients of the power stage transfer function are automatically computed by a set of instructions as illustrated below in Fig. 12. In the left-side part, you set the variable *load* to either 0 or 1.

When set to 0, the macro assumes a dc-dc converter loads the PFC stage and the Laplace-domain transfer function is changed to reflect the integrator-type response. The biquad coefficients are also automatically calculated and lead to the expected type 2 transfer function.

Once the simulation is run, the loop gain should exhibit an adequate crossover frequency with an acceptable phase margin. Fig. 13 confirms a 13-Hz crossover with a 64° of phase margin at low line while it slightly decreases to 10 Hz in low-line conditions with a 60° phase margin. This is a robust design and you can notice how crossover remains independent of the input line level. This guarantees a stable design and limits the distortion at high line by reducing the amount of ripple polluting the control voltage.

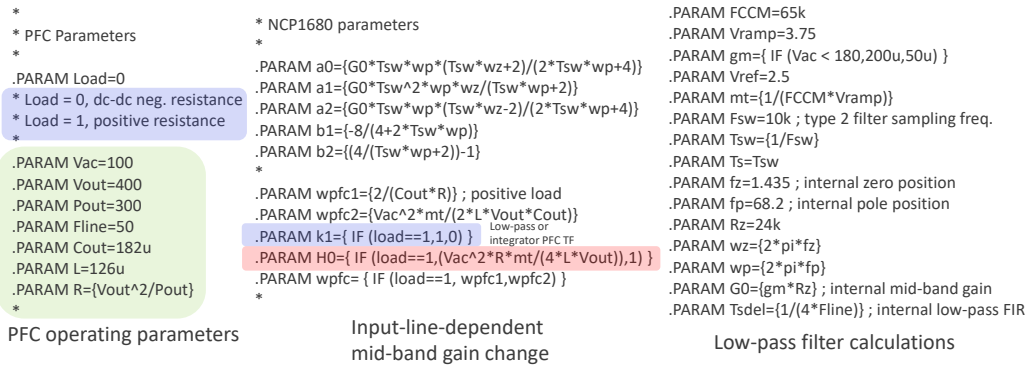

Fig. 12. A set of instructions automates generation of the component values and coefficients for the filters.

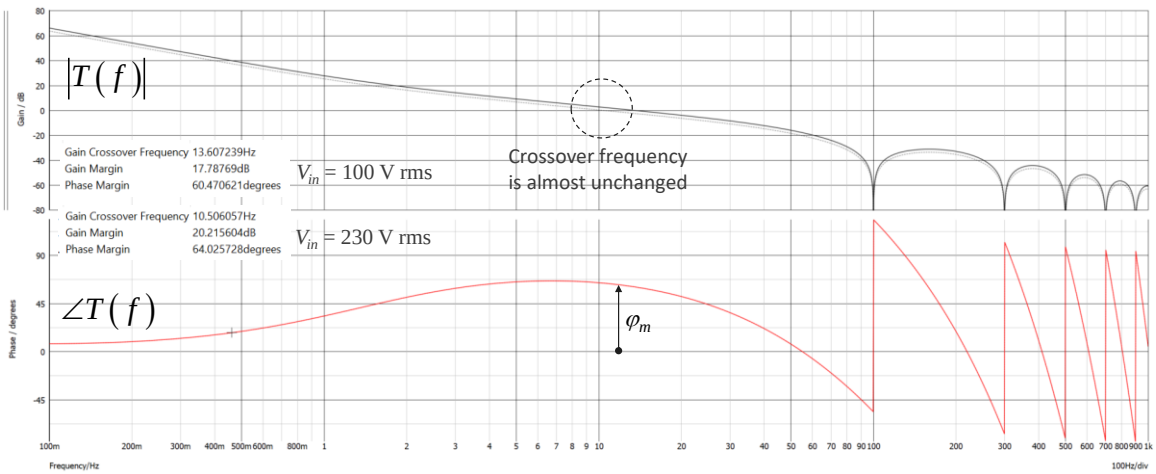

Fig. 13. The loop gain of this 300-W PFC is stable with a comfortable phase margin of 60°.

If you now chose to reduce the output capacitance for different reasons like cost or available volume in the enclosure, the fixed compensation parameters might not lead to the expected margin. An example of this effect is shown in Fig. 14.

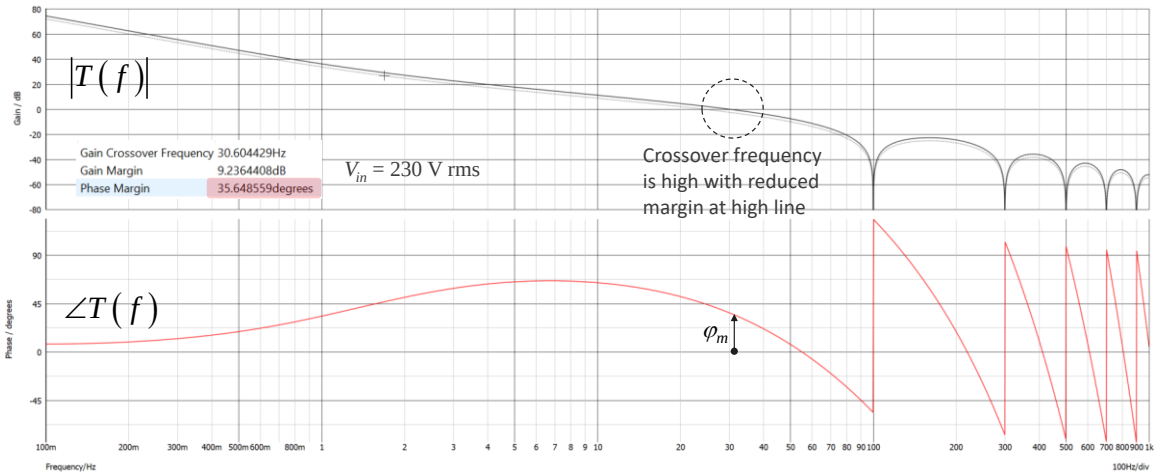

Fig. 14. Reduce the output capacitance from 182 µF to 68 µF and stability can become marginal.

This is because the power stage gain increases with the lower capacitance and brings a higher crossover frequency. However, as the phase boost is fixed and located at 10 Hz by design, the part cannot bring adequate compensation with this component selection.

In this case, you may want to add a small capacitance across the upper sense resistor to form an extra zero. This will certainly improve the phase margin but keep the high crossover and its detrimental effects on input current distortion. As a conclusion, make sure enough output capacitance is selected with this part so that loop gain always offers enough phase margin in any operating condition.

Conclusion

This article shows how the NCP1680 from onsemi can be used to power a totem-pole PFC without resorting to a microcontroller implementation, which requires writing software code and adds cost in the implementation of current sensing. The component mixes analog and digital circuitries for orchestrating the many variables that need to be monitored in such a pre-converter. For your applications below 500 W, the borderline conduction mode implemented in the NCP1680 lends itself well to building an efficient and reliable TPPFC pre-converter.

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Christophe Basso is a business development manager with Future Electronics, a member of the power team and covering EMEA. Previously, he was a technical fellow with ON Semiconductor for 24 years where he originated numerous integrated circuits. SPICE simulation is also one of his favorite subjects and he has authored two books on the subject. Christophe's latest work is "Transfer Functions of Switching Converters: Fast Analytical Techniques at Work with Small-Signal Analysis". Christophe received a BSEE-equivalent from the Montpellier University, France and an MSEE from the Institut National Polytechnique de Toulouse, France. He holds 25 patents on power conversion and often publishes papers in conferences and trade magazines.

For further reading on designing PFC boost converters, see the How2Power Design Guide, locate the Popular Topics category and select Power Factor Correction.