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Stepdown Voltage Regulator With Reduced Input Current Ripple

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Due to their simplicity, their low cost, and the wide variety of controller ICs available to implement them, stepdown (buck) voltage regulators are extremely popular in multiple applications, including computer and server motherboards, PDNs, and cell phones. However, the usage of stepdown converters operating at high switching frequencies represents a certain challenge for electronic equipment or system designers. If the current ripple produced by the voltage regulator (VR) is not properly filtered, it can interfere with other devices powered from the same source—PSU or PDN.

To address this challenge, buck regulator suppliers provide detailed recommendations on ripple and noise suppression.[1-3] They typically suggest using a series inductor in the input current flow path which forms a low pass filter with the VR input decoupling cap. This approach is considered the most common for confining ripple currents to the VR local input bypass caps.

However, this solution has some shortcomings associated with the usage of an additional magnetic component whose parameters often need to be determined through experimentation. That's because the power distribution network configuration and regulation performance of the host supply are usually unknown at the design stage.

In the early days when switched-mode techniques were first being adopted, a noteworthy buck converter topology was introduced by Alfred Leifer in the form of a class D modulator of a high-frequency transmitter.[4] The topology used in this application has several advantages over the conventional buck regulator that is so common nowadays. One of the most valuable benefits of the mentioned technique is that it provides continuous current at the converter input. This feature enables minimization of the filtering cap value and eliminating the filtering inductor without affecting the converter's transient performance.

This article examines the operation of this converter in more detail and studies an opportunity for adopting such a regulator technique if a suitable controller IC were to be made available.

We begin by reviewing the operation of a standard buck converter and the drawbacks of its input LC filter. We then see how the placement of the inductor on the input, as found in other regulator topologies with continuous input current, can be extended to the buck converter with some modifications of the inductor and other circuit details.

The switching operation of this modified buck converter is then explained, as well as the design of the modified inductor. An analysis of inductor winding size for the modified converter enables designers to evaluate the tradeoffs in using the proposed converter design versus a standard buck. Equations for determining the input capacitor ratings are also given, and current ratings for the proposed design are compared with the standard buck converter.

Problem Statement

Let's consider a conventional stepdown VR (Fig. 1) operating in continuous-conduction mode. In this circuit, MOSFET Q1 switches on and off, and output inductor L1's current consequently flows through the switching MOSFET Q1 and freewheeling diode D1. Assuming power losses in this converter are negligible as compared to the power delivered to the load, for continuous-conduction mode, the voltage conversion relationship depends only on the input voltage V_{in} and a duty ratio D of the pulses generated at the filter input:

$$V_o = V_{in}D$$

The low $R_{DS(ON)}$ of modern transistors made it more common to implement synchronous rectification where a more-efficient FET replaces the traditional freewheeling diode D1. But to make it easier to follow the circuit transformations and analysis, we will be considering the fundamental topology with the freewheeling diode.

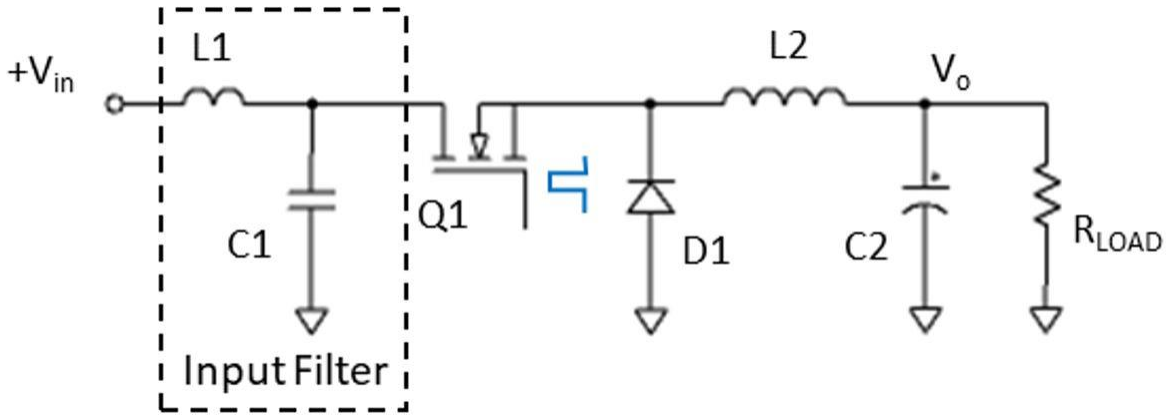

Fig. 1. Basic stepdown voltage regulator. Input LC filter components reduce voltage spikes on Q1 and D1 and smooth the current drawn by the converter to keep the host supply voltage within the required range.

In this regulator, while the output inductor L2 current can have a very low ripple (especially when the inductance value significantly exceeds the critical value) the current drawn from the host supply represents a sequence of rectangular shape pulses with a magnitude approximately equal to the load current. Input inductor L1 and input filter cap C1 smooth the current drawn by the switching stage to keep the host supply voltage within the required range.

However, during a transient, filter inductor L1 slows the current slew rate that can be provided by the host supply, so the use of such an inductor also places more demands on the input filter capacitors since more of the initial current demand must come from the bulk caps rather than the host supply.

The goal of this study is to eliminate shortcomings associated with VR compatibility with the host power supply and examine a design concept that is capable of smoothing the current drawn from the input and suppressing noise emissions from a switching regulator without using the additional magnetic component.

Current Sink Buck Stage

For a better understanding of the introduced design concept let's consider a sequence of modifications to the basic topology that could eliminate rapid input current changes and enable a current-fed converter operation. All continuous input current converter topologies, including the most basic, such as boost, SEPIC, or Cuk converters, have one feature in common—the filter inductor in these converters is placed in the input current path. Interposing the high instantaneous impedance of the inductor between the primary source and the switching stage by definition prevents any rapid input current variations.

So, to create a condition for continuous input current flow in a buck regulator the output inductor can be placed at the input i.e., the positions of the output inductor and the switch in Fig. 1 can be swapped. To form a current path for the time interval when the switch is off, input cap C1 coupled to the anode of the freewheeling diode D1 needs to be disconnected from the ground plane (Fig. 2). To provide a current flow through the cap in both directions, a second identical grounded inductor (or a grounded winding w2 placed on the same inductor core) needs to be used.

The resulting circuit topology implementing the listed modifications and using an identical inductor winding placed on the core is shown in Fig. 2. In this topology, current of each inductor winding can pass through the cap and sequentially flow either through the closed switch Q1 or the conducting diode D1.

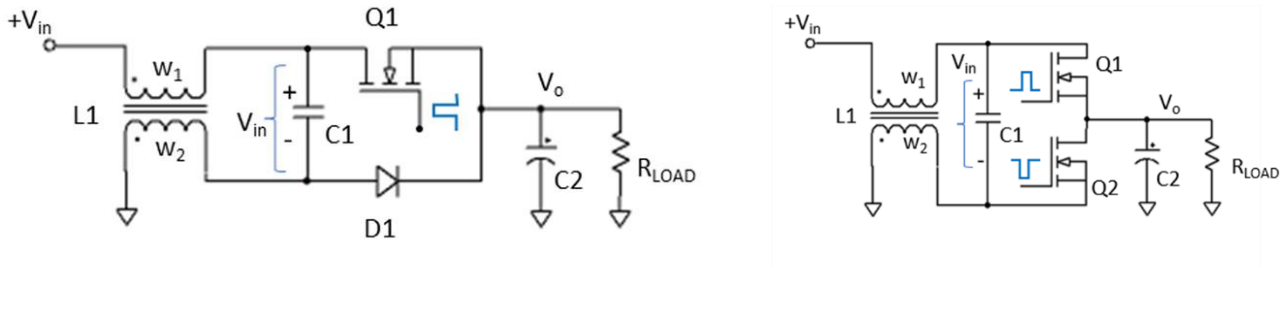

Fig. 2. Enhanced buck converter topology with continuous input current (a). The current of each inductor winding can pass through the cap and sequentially flow either through closed switch Q1 or conducting diode D1. The same topology can also be implemented with a synchronous FET in place of the freewheeling diode (b).

The circuit equivalent schematics for the switch on and off time intervals are shown in Fig. 3a and Fig.3b, respectively. In these schematics, components in conducting (on) and non-conducting (off) states are represented by short and open circuits, respectively. The output network in Fig. 3 is replaced with a voltage source V_o capable of absorbing energy. This was done under the assumption that the output voltage ripple and the energy associated with it is much smaller than the dc component, which is valid for all practical cases.

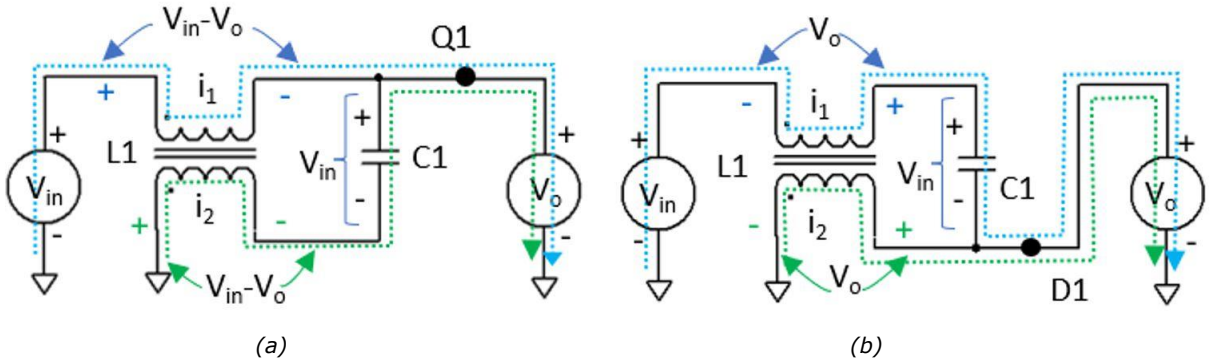

Fig. 3. Continuous input current VR equivalent schematics for switch-on (a) and switch-off (b) time intervals.

When the VR is first turned on, the cap C1 is charged from the input source V_{in} through the two inductor windings without generating any magnetic flux in the inductor core, because fluxes created by each of the windings cancel each other out. Similar to the conventional topology, when the switch (Q1) is on, voltages applied to each of the inductor windings are equal to V_{in}- V_o, the inductor gets charged and currents of both windings ramp up flowing through the closed switch (Fig. 3a).

When the switch is off, the inductor releases a portion of the stored energy to the load, and the winding currents ramp down flowing through the freewheeling diode D1 (Fig. 3b). Blue and green dotted lines in Fig. 3 show the current paths of primary w1 and secondary w2 windings. As it can be seen from the diagrams in Fig. 3 the switch and diode voltages in their non-conducting states are equal to the voltage across C1, so the active components' maximum voltage ($V_{DS.max}$ = $V_{D1.max}$ = $V_{in.max}$) and current (I_{Q1max} = $I_{D1.max}$ = $I_{o.max}$) ratings in this arrangement are identical to the basic version.

Voltage spikes caused by leakage inductance between the windings can be stiffly clamped at the V_{in} level by the freewheeling and Q1 body diodes. Unlike in the conventional case, the voltage at the phase node (Q1 source

terminal) remains constant relative to the ground and equal to V_o. If a freewheeling diode is replaced with a synchronous FET, its source voltage relative to the ground will be varying from negative level: $-(V_{in} - V_o)$ to positive: $+V_o$. This topology is shown in Fig. 2b.

The set of waveforms illustrating the converter operation is shown in Fig. 4.

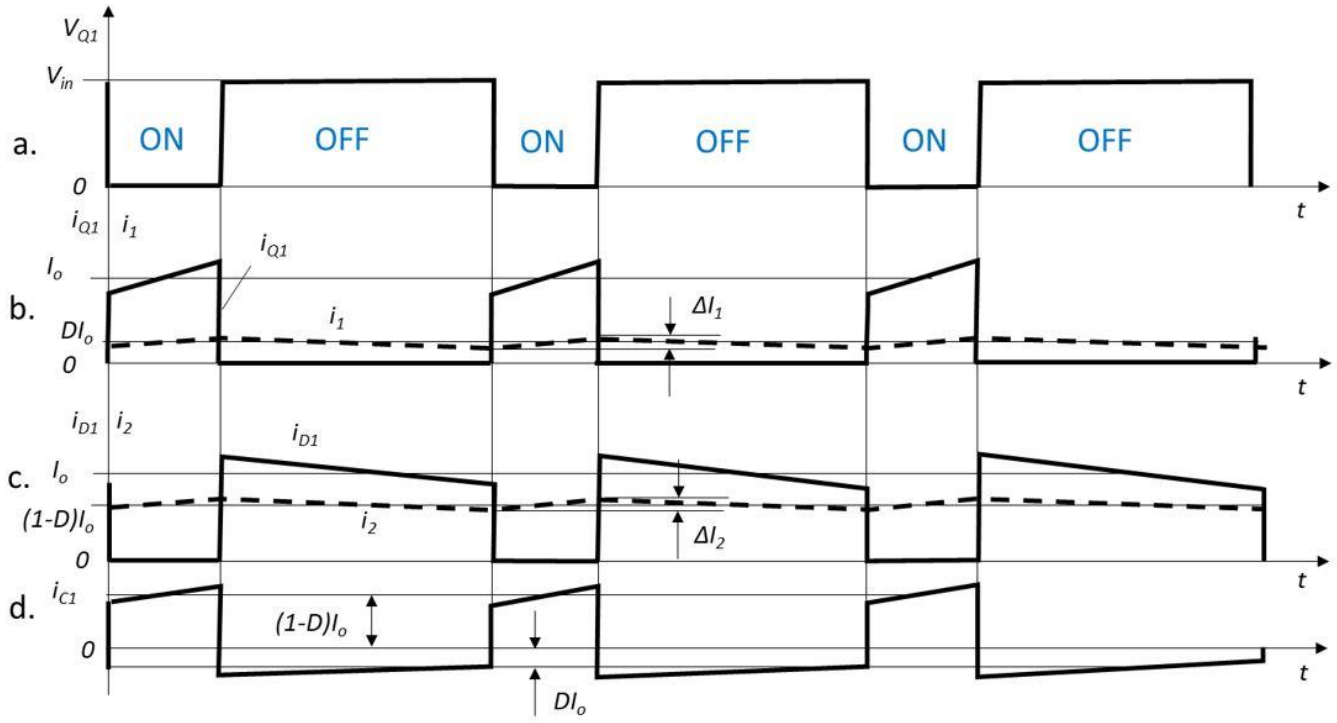

Fig. 4. Voltage and current waveforms in the continuous-input current regulator shown in Fig. 2. Input current (i1) waveform (dashed line in diagram b.) is distinctly different from the conventional case and represents a continuous function of time.

As can be seen from these diagrams, the input current (i1) waveform is distinctly different from the conventional case which essentially matches the switch waveform i_{Q1} in Fig. 4. In the modified VR stage, input current (i_1) appears to be flowing continuously either through Q1, or C1 and D1.

Thus, moving the VR output inductor to the input and providing a path for current flow for the primary inductor winding in the on and off switch states enables the transformation of the conventional VR circuit into a simple switch-mode current-sinking stage with basic characteristics identical to the classic buck regulator. To make a more detailed comparison of the introduced and basic converter topologies, let's take a closer look at the waveforms and characterize the currents flowing through each of the inductor windings and weigh the repositioned cap RMS current against the conventional case. Comparing the RMS current levels under the same conditions (identical inductance value and equal input and output voltages, and load current) will allow us to characterize the introduced VR application specifics.

VR Application Considerations

Inductor Winding Size Impact

As shown in Fig. 3, inductor winding currents i_1 and i_2 subsequently flow through C1, while the sum of these currents forms the load current I_O. Based on this condition and a stipulation that the cap current cannot have a dc component, we can determine the winding currents from the following equations:

$$I_2 \cdot t_{ON} = I_1 \cdot (T_{SW} - t_{ON})$$

$$I_1 + I_2 = I_o = P_o/V_o$$

where t_{ON} is the switch on-time interval, T_{SW} is the switching cycle, and P_O is the output power level.

In the first equation, the output cap ripple current is neglected for clarity purposes without any impact on amp-second product values. The solution of this system of equations is

$$I_1 = P_o D/V_o$$

$$I_2 = P_o(1 - D)/V_o$$

where $D = t_{ON}/T_{SW}$ is the on duty ratio, which for a stepdown lossless VR can be determined as $D = V_o/V_{in}$.

The total cross-sectional area of the inductor winding is proportional to the maximum load current. In the conventional case, this area is defined by the maximum load current $I_{o.max}$, allowed current density J_L and the number of turns w:

$$A_{TC} = wI_{o.max}/J_L \qquad (1)$$

Assuming the same inductance value and the same number of turns in each of the windings total cross-sectional area A_{TT} of the introduced VR inductor windings must be computed for the worst case, i.e. maximum current level in each of the windings:

$$A_{TT} = \frac{w}{J_L}(I_{1.max} + I_{2.max})$$

where $I_{2.max}$ and $I_{2.max}$ can be expressed via maximum output power $P_{o.max}$ and the maximum and minimum input voltage levels:

$$A_{TT} = \frac{w}{J_L}\left[\frac{P_{o.max}D_{max}}{V_o} + \frac{P_{o.max}(1-D_{min})}{V_o}\right] = \frac{w}{J_L}\frac{P_{o.max}}{V_o}\left[\frac{V_o}{V_{in.min}} + \left(1 - \frac{V_o}{V_{in.max}}\right)\right] \qquad (2)$$

Equations (1) and (2) can be used to determine the winding cross-section increase factor k, as compared to the conventional case:

$$k = \frac{A_{TT}}{A_{TC}} - 1 = \left[\frac{V_o}{V_{in.min}} + \left(1 - \frac{V_o}{V_{in.max}}\right)\right] - 1 \qquad (3)$$

Expressing the max and minimum input voltages as $V_{in.min} = V_{in.nom}$-ΔV and $V_{in.max} = V_{in.nom}$+ΔV, where ΔV is input voltage deviation from nominal, equation (3) can be rewritten as follows:

$$k = \frac{V_o/V_{in.nom}}{(1-\widehat{\Delta V})} - \frac{V_o/V_{in.nom}}{(1+\widehat{\Delta V})} \qquad (4)$$

where $\widehat{\Delta V} = \Delta V/V_{in.nom}$ is the input voltage variation normalized over the nominal input voltage level. This equation shows that if VR operates from a tightly regulated voltage source (ΔV =0), then k = 0 and there is no difference in inductor sizes between the conventional and introduced VR topology options. But as the input voltage variation range increases, the difference can become noticeable, especially for the cases with higher $V_o/V_{in.nom}$ ratios. The set of graphs representing this increase as a function of normalized input voltage variation $\widehat{\Delta V} = \Delta V/V_{in.nom}$ and relative output level $V_o/V_{in.nom}$ is given in Fig. 5.

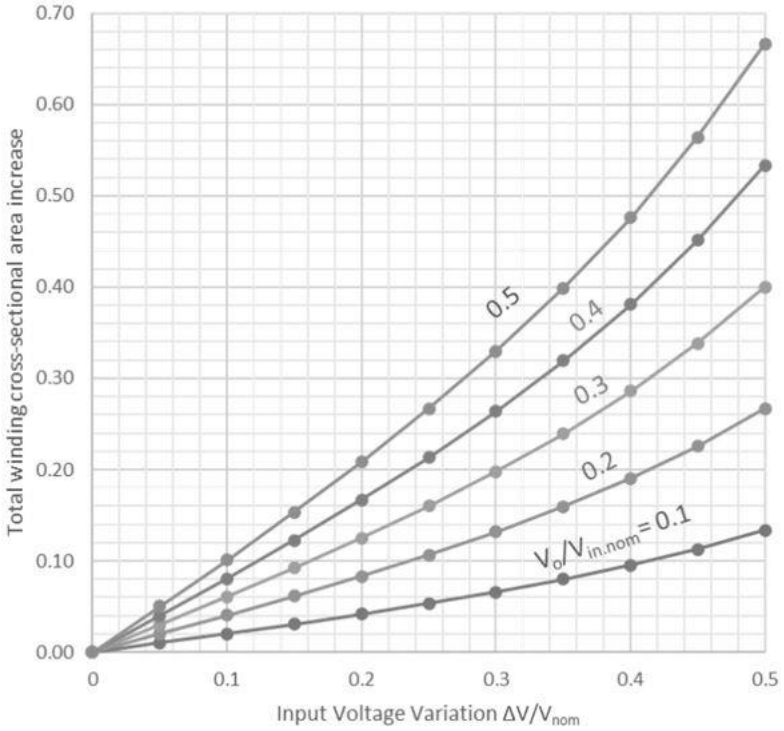

Fig. 5 Inductor winding cross-sectional area increase (k) in the modified VR vs. input voltage variation and output-to-input voltage ratio.

The graphs in Fig. 5 can help to make tradeoffs between the use of the additional magnetic component in the conventional buck design and the inductor winding size increase in the proposed buck design. They show that in many cases when output voltage does not exceed 25% of input and input voltage variation does not exceed 20%, the winding increase factor won't exceed 10% and in practice won't be noticeable. This makes the introduced topology attractive for many low-voltage applications such as CPU and memory VRs.

Winding Ripple Currents And Output Voltage Ripple

Based on the equivalent circuit diagrams in Fig. 3, voltage magnitudes applied to each of the inductor windings during on and off time intervals, regardless of sign, are

$$V_{w1(ON)} = V_{w2(ON)} = V_{in} - V_o$$

$$V_{w1(OFF)} = V_{w2(OFF)} = V_o$$

and the current pk-pk ripple in each of the magnetically coupled windings are

$$\Delta I_{1(2)} = \frac{(V_{in} - V_o)DT_{SW}}{L_{w1(2)} \pm M}$$

where M is the mutual inductance such that $M = k_C\sqrt{L_{w1}L_{w2}}$, L_{w1} *and* L_{w2} are inductance values of L1 windings, and k_C is the coupling coefficient. Since the two currents i_1 and i_2 enter the dotted ends of the coupled windings (Fig. 3), the sign of the mutual inductance is positive, and the current pk-pk ripple in each of the windings can be determined as

$$\Delta I_1 = \frac{(V_{in}-V_o)DT_{SW}}{L_{w1}+k_C\sqrt{L_{w1}L_{w2}}} = \frac{V_o(1-D)T_{SW}}{L_{w1}+k_C\sqrt{L_{w1}L_{w2}}} \qquad (5)$$

$$\Delta I_2 = \frac{(V_{in}-V_o)DT_{SW}}{L_{w2}+k_C\sqrt{L_{w1}L_{w2}}} = \frac{V_o(1-D)T_{SW}}{L_{w2}+k_C\sqrt{L_{w1}L_{w2}}} \qquad (6)$$

Since the windings have an equal number of turns, their inductances can be considered identical and set equal to the inductance value L of the conventional buck regulator $L_{w1} = L_{w2} = L$. Assuming $k_C \cong 1$ we can express the current ripple in each of the windings as

$$\Delta I_1 = \Delta I_2 = \frac{(V_{in} - V_o)DT_{SW}}{2L} = \frac{V_o(1-D)T_{SW}}{2L}$$

This represents 50% of the pk-pk ripple of the conventional buck topology having the same inductance value and illustrated with dashed line waveforms in Fig. 4b,c. Since the two windings currents get summed at the load node (Fig. 2) the resultant output cap ripple current will be identical to the conventional case.

This means that with the same L and C values, output voltage ripple will be also identical to the conventional case. At the same time, providing small input current ripple and confining large ripple currents to the VR's "internal" circuitry greatly simplifies regulator electric compatibility with the host supply and other devices connected to the same source.

It is important to note that if separate inductors are used in the circuit in Fig. 2, the coupling coefficient in equations (5) and (6) needs to be set to zero. Substituting this k_C value into these equations will result in the current ripple level increase by a factor of two as compared to the magnetically coupled case.

In other words, providing the same output ripple level with separate inductors in this circuit will require doubling the inductance or capacitance value and a considerable converter size increase. That is why for practical applications the coupled inductor version shown in Fig. 2 has significant advantages.

Input Capacitor Voltage Ripple And RMS Current

Capacitor RMS current and voltage ripple typically represent the key parameters used in the cap selection procedure. Cap pk-pk voltage ripple can be determined based on any current polarity amp-second area and pk-pk current step size. For example, for the i_1 flow-time-interval, cap voltage ripple can be expressed as

$$V_{C1pk-pk} = \frac{1}{C_1}\int_0^{t_{ON}} I_1 dt + \frac{P_o}{V_o}.ESR = \frac{P_o}{V_o}\left(\frac{DT_{SW}}{C_1} + ESR\right) \qquad (7)$$

where *ESR* is the equivalent series resistance of the cap.

Cap RMS current needs to be determined by both positive and negative portions of the cap current waveform:

$$I_{C.RMS} = \sqrt{\frac{1}{T_{SW}}\int_{t_{ON}}^{T_{SW}} I_1^2 dt + \frac{1}{T_{SW}}\int_0^{t_{ON}} I_2^2 dt} = \frac{P_o}{V_o}\sqrt{D-D^2} \qquad (8)$$

The graph of the input cap RMS current normalized over the load current $I_o = P_o/V_o$ is given in Fig. 6.

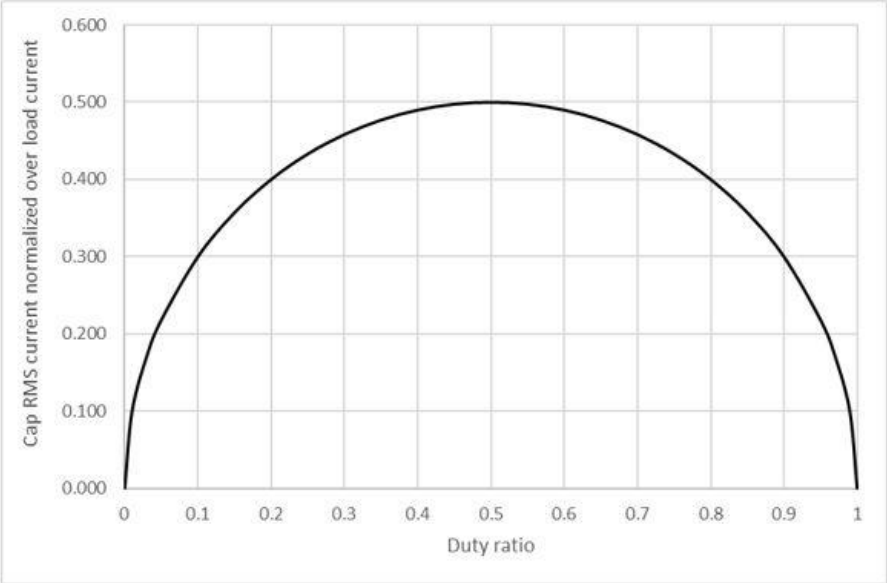

Fig. 6. Normalized input cap RMS current vs. duty ratio.

This graph exactly matches the conventional case[3] in which the cap is placed at the VR input, and equations (7) and (8) can be used for this component selection.

Conclusions

A stepdown voltage regulator with a constant input current has been presented. It is characterized by a much lower ripple generated in the host supply PDN achieved without using an additional input current smoothing magnetic component as would be required with a conventional buck design needing lower ripple.

The introduced converter topology can be considered the most efficient for confining ripple currents to the VR local circuitry and simplifies regulator electric compatibility with the host supply and other devices connected to the same source.

The presented solution can be recommended for many low-voltage applications such as CPU and memory VRs, having relatively low output-to-input voltage ratios (or relatively high input-to-output voltage ratios) and relatively small input-voltage variations.

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About The Author

Viktor Vogman currently works at Power Conversion Consulting as an analog design engineer, specializing in the design of various power test tools for ac and dc power delivery applications. Prior to this, he spent over 20 years at Intel, focused on hardware engineering and power delivery architectures. Viktor obtained an MS degree in Radio Communication, Television and Multimedia Technology and a PhD in Power Electronics from the Saint Petersburg University of Telecommunications, Russia. Vogman holds over 50 U.S. and foreign patents and has authored over 20 articles on various aspects of power delivery and analog design.

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