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Silicon Capacitors Shrink Footprint And Component Count For High-Frequency Decoupling

Empower Semiconductor has expanded its E-CAP family of silicon capacitors with new technologies that offer further breakthroughs in density and performance. Integrating multiple discrete capacitances into a custom, single solid-state device, E-CAP is described as the world's thinnest, most compact and most flexible capacitor solution. According to the company, the technology brings together a capacitor density that is over five times that of leading multilayer ceramic capacitors (MLCCs) with improved equivalent series inductance (ESL) and equivalent series resistance (ESR) characteristics that dramatically reduce parasitics (Fig. 1).

Designed using the most advanced trench capacitor technology, the latest E-CAP solutions offer densities of 1.1 $\mu F/mm^2$, which is over twice the density of alternative silicon capacitor technologies, says the vendor. In addition to the density, thickness levels can be achieved below 50 µm in overall height.

These new E-CAP solutions represent the second generation of Empower's silicon trench capacitor technology. The previous generation, which was announced last year, had a minimum thickness of 75 µm. It was also based on a 4-V technology versus 2 V for this new generation.

The company initially applied this technology for the I/O caps used in its integrated voltage regulators (IVRs). However, the silicon capacitor technology itself predates Empower's use and is well established, having been applied in mobile phones for about 10 years, according to the company.

Multiple, matched capacitance values from 75 pF to 5 µF at 2 V can be integrated into a single die to create custom integrated capacitor arrays, while form factors can be customized for the space and height limitations of a particular application. Packaging options based on bumps, pads and pillars allow designers to choose the best solution based on specific system constraints (see the Table).

"E-CAP provides a superior high-frequency de-coupling solution with a much smaller footprint and component count than traditional MLCC-based solutions," says Steve Shultis, Empower's SVP of Sales and Marketing (see Fig. 2). "Our technology provides new options for demanding applications in IoT, wearables, mobile, and processors where size, performance, and flexibility are essential. The latest improvements in density and performance make E-CAP ideal for next-generation, data-intensive systems that demand high-frequency operation and maximum efficiency from the smallest possible form factors."

Using E-CAP, designers can combine all non-bulk, high-frequency decoupling capacitors into a single die to dramatically reduce component count, BoM cost and potential points of failure. Although the E-CAPs have lower nominal capacitance, their superior frequency response and ESL over MLCCs results in lower impedance at high frequencies.

And unlike MLCCs where multiple devices are needed to account for derating from voltage, temperature and age, E-CAP requires no ac or dc bias derating while all other derating requirements are negligible. This eliminates the need to overspecify capacitance requirements to account for derating (Fig. 3).

The company adds that E-CAP is also optimal for in-package filtering and bypass in system-on-chip devices (SoCs), offering >2x higher capacitance density compared to the closest competitor and requiring one-third the capacitance compared to standard MLCCs. In this usage, E-CAP's ESL is as low as 15 pH versus ~200 pH for MLCCs.

Meanwhile, the E-CAPS for filtering and bypass can be as thin as 75 µm, are not susceptible to low-frequency audible noise found in MLCCs, and contain no materials sensitive to magnetic fields. This latest characteristic proves valuable in applications such as MRIs and particle accelerators. In addition, matched capacitors can be integrated in a single die and custom arrays can be created as with E-CAP solutions for decoupling.

For more information, see the website or email info@empowersemi.com.

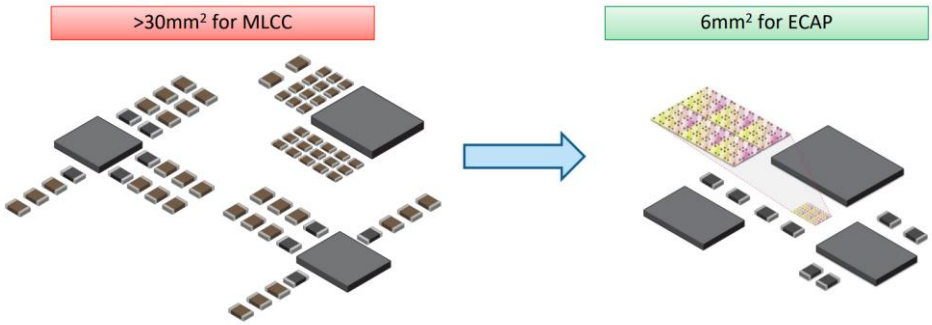
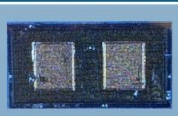
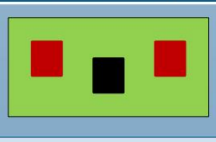
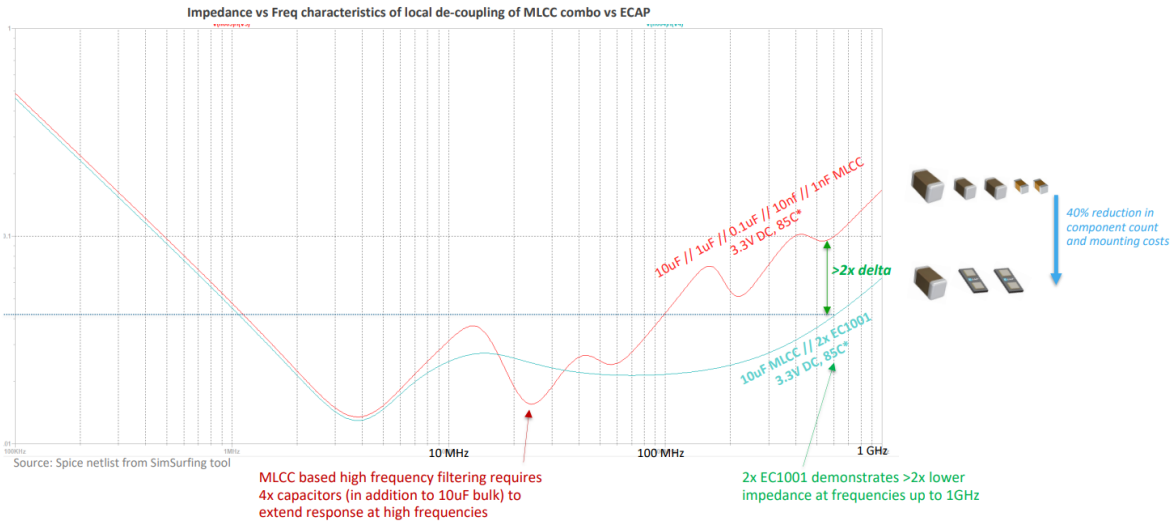


Fig. 1. An E-CAP-based decoupling solution is said to provide >5x density compared to a solution using standard MLCCs.

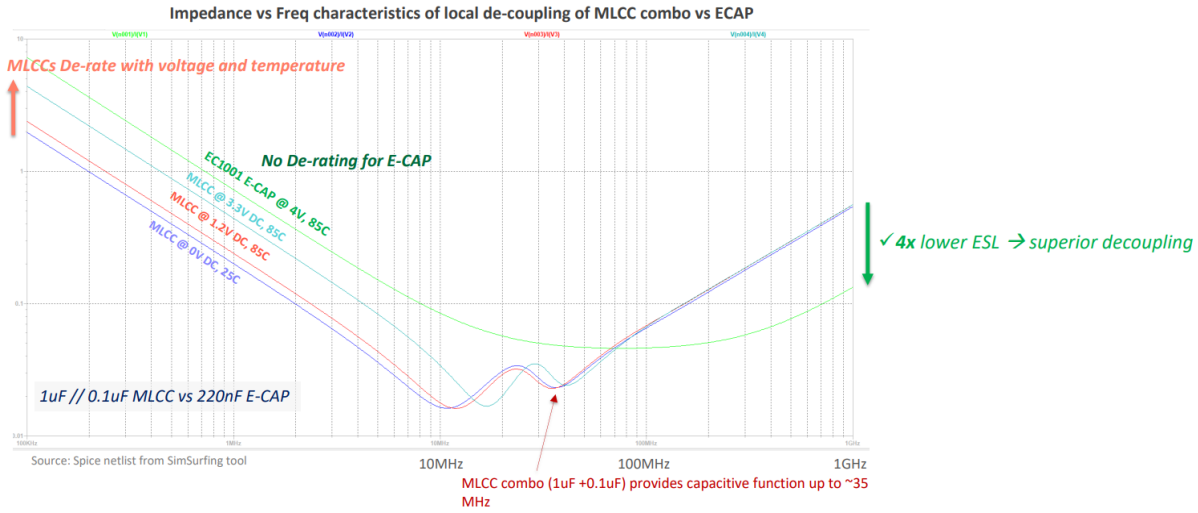
Table. E-CAP design examples demonstrate a range of combinations and package options for the silicon capacitors.

Gen1 Single-Cap	Gen1 Multi-Cap	Gen2 Multi-Cap	Gen2 Double-Cap
			
1 capacitor	5 capacitors integrated	18 capacitors integrated	2 capacitors integrated
220 nF	670 nF total	4,800 nF total	2 x 1 nF
4V V_{Op}^{max}	4V V_{Op}^{max}	2V V_{Op}^{max}	4V V_{Op}^{max}
1 mm x 0.5 mm	2.5 mm x 0.6 mm	2.2 mm x 2 mm	0.5 mm x 0.25 mm
Rectangular copper pads 450um pitch	Rectangular copper pads 150um pitch	Circular CuP bumps For PCB assembly	Rectangular CuP flat bumps for substrate assembly
Die thickness: 100+ µm			
Pad pitch: 150 - 450 µm			
Pad height: 15 - 50 µm			



(a)

(3.3-Vdc and 85°C derating sourced from Murata simulation data.)*



(b)

Fig. 2. Impedance versus frequency characteristics of local decoupling of MLCC combo vs E-CAP. E-CAP's superior high-frequency response and low ESL results in fewer components and lower mounting cost (b) as well as better high-frequency decoupling due to the lower ESL (b).

MLCCs require multiples to account for de-rating from voltage, temperature and age

ECAP does not require over-design due to negligible de-rating from voltage, temperature and age

Parameter	Standard MLCC	ECAP
DC bias de-rating	*44% @ 3 V*	*None*
Temp de-rating	*-11% up to 85 °C*	*Negligible - ~0.3% (measured in ppm / K) – equivalent to C0G*
Aging	*~5-10% / 10k hrs*	*<0.001% / 10k hrs*
ESL	*>100pH (100nF)*	*<10pH (100nF)*

Fig. 3. Relative to MLCCs, the negligible derating of E-CAP devices simplifies system design.