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Give Your Battery A Rest With A Supercapacitor-based Power Subsystem

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Today's mobile handsets are becoming more feature rich and power hungry. The basic VGA imager that was popular two to three years ago is now being replaced by imagers with 3.2 megapixels (MP) or higher (some over 8 MP) with higher-current LED flashes. Lower-power monaural audio drivers are being replaced with higher-power stereo drivers for use in multimedia playback. With the spread of 3G networks, the transfer of wireless data has increased exponentially requiring multiple RF power amplifiers (RF PAs) to be placed into the handset to handle both voice calls and data streams.

Unfortunately, each of these functions can draw large pulses of battery current (1 A or more) when in use. If allowed to operate at the same time, these features can often cause a battery current fault or prematurely shut down the device.

Solutions for handling peak battery current are possible through careful pulse timing management and reduction of overall performance requirements such as limiting the flash current or audio volume. Both solutions limit the phone's capabilities and are not always welcome. One alternative approach is to create a power subsystem based on a supercapacitor and a supercapacitor management IC. This approach can help restore the application to its full potential.

Today's System Issues

With lithium-ion (Li-ion) battery current limits where they are now (around 2-A to 3-A per cell), the designer must carefully manage the timing of the current demand by the different loads in the system to avoid an overcurrent situation. Additionally, when the battery voltage is low and close to the system shutoff voltage, large current pulses in conjunction with the battery ESR can cause the system to shut down prematurely. For example, if a GSM transmit occurs at the same time as an LED flash event, the total pulsed current demand could easily exceed 3 A (2 A for transmit event and 1.5 A for flash).

To help prevent these overcurrent situations many handset designs use one of two approaches to hold input current to a manageable level. Either they derate the flash current or issue a transmit interrupt. The latter is supported by the transmit interrupt pin provided on many flash LED driver ICs.

A transmit interrupt provides a synchronization mechanism between the RF PA and the flash driver. When the RF PA begins to transmit during a flash event, the flash interrupt should fire, causing the flash current to either reduce to a lower level or turn off completely.

This feature prevents the battery from being overloaded. However, if a rolling shutter is used, the result will be a picture that has either dark lines or a dark section on the image. Derated flash current and transmit interrupt are both performance compromises that can yield poorer picture quality.

Fig. 1 shows the effect of numerous pulsed loads on a battery, highlighting the issues of the battery's ESR voltage drop as well as the magnitude of the total pulsed battery current. Assuming a 100-mΩ battery ESR and loads consisting of a 1.2-A LED flash pulse, a 2-A GSM transmit pulse and a stereo Class-D amplifier, the peak pulse current could exceed 4 A and cause a momentary drop of 400 mV in the battery line voltage.

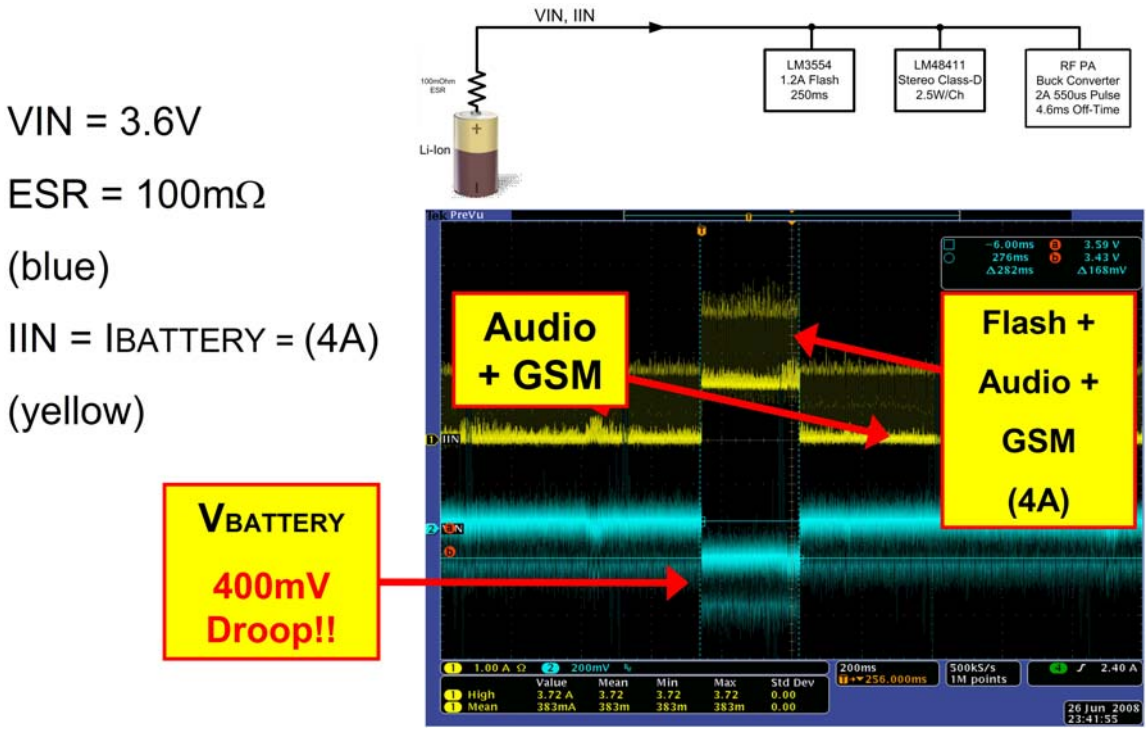

***Fig. 1**. When multiple pulsed loads in a handset fire at once, the battery voltage can drop dramatically.*

To avoid this drop, a, concession must be made in terms of decreasing the flash current and audio power to lower peak-currents levels that can be tolerated in the system. Alternatively, the battery capacity must be increased. The addition of a supercapacitor, however, would effectively increase the battery's pulse current handling capacity without increasing the battery capacity. This allows the full system performance to be realized.

What Is A Supercapacitor?

The proper name for a supercapacitor is an electrochemical or electric (depending on the manufacturer) dual layer capacitor, or EDLC for short. Supercapacitors behave like traditional capacitors (MLCC, tantalum, electrolytic etc.) except they have a much higher energy density. This increased energy density is achieved through the combination of porous carbon-based electrodes that create a very large charge storing surface area and a very thin plate-separation layer provided by specialized electrolytes.

EDLCs can have capacitance values that could never reasonably be placed in a thin portable system using other capacitor styles. Typical EDLC thickness is around 2-mm to 3-mm compared to an electrolytic capacitor used for Xenon flash applications, which has typically has a thickness greater than 6 mm.

EDLC capacitance values can range from 180 mF up to 1.8 F for single-cell capacitors with maximum voltage ratings around 2.75 V to 2.85 V. In this article, the focus will be on the dual-cell variety EDLC (two single-cell EDLCs in series). Dual-cell EDLCs feature a voltage rating of 5.5 V to 5.7 V and a capacitance value between 425 mF and 550 mF.

Supercapacitor Placement

Having a very large capacitance available in a portable system can provide many advantages. Where the supercapacitor is placed can have dramatic effects on the battery supply current.

If placed in parallel with the system battery, a supercapacitor can help lower the peak current from the battery when a large current is drawn by an LED flash driver or RF transmission. The amount of current supplied by the supercapacitor and the battery will be inversely proportional to the electrical series resistance (ESR) of the battery and the ESR of the supercapacitor. The supply (in this case the battery and supercapacitor combo) with the lowest ESR, will deliver the most current.

A supercapacitor can have ESR values as low as 50 mΩ, while a typical Li-ion battery has 200 mΩ to 300 mΩ of ESR. An example illustrates how the initial current drawn from the battery compares to the current drawn from the supercapacitor.

In this example, $I_{LOAD} = I_{CAP} + I_{BAT} = 2$ A; $R_{CAP} = 50$ mΩ and $R_{BAT} = 300$ mΩ; and initially, $V_{BAT} = V_{CAP}$. Given these conditions, the initial I_{BAT} and I_{CAP} can be determined as follows:

$V_{BAT} - (I_{BAT} \times R_{BAT}) = V_{CAP} - (I_{CAP} \times R_{CAP})$

$I_{CAP} = I_{BAT} \times R_{BAT} / R_{CAP}$

$I_{CAP} = 6 \times I_{BAT}$

$I_{BAT} = 2\text{ A} / 7 = 285\text{ mA}$

$I_{CAP} = 1.715$ A

As the load pulse continues, the current from the supercapacitor will decrease and the current from the battery will increase due to the discharging of the supercapacitor (Fig. 2). Sharing the load helps minimize the battery's ESR drop due to the pulsed loads, potentially extending the usable battery range.

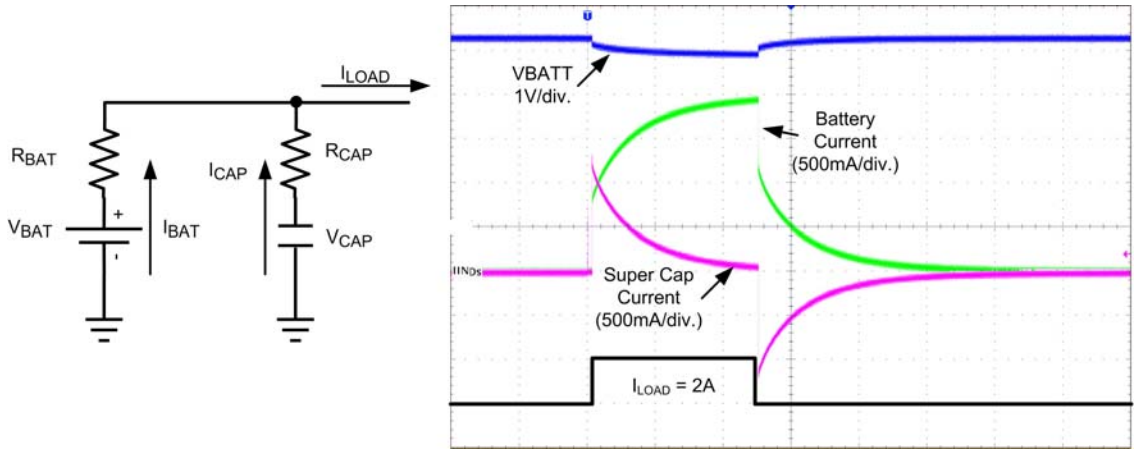

Fig. 2. *When a load pulse occurs, the current supplied by the supercapacitor decreases over the interval of the pulse.*

Having a supercapacitor in parallel with the battery does help prevent early shutdown conditions. Nevertheless, there are some problems with this configuration. To prevent damage to the battery, some form of current-limiting circuit should be placed between the battery and the supercapacitor. When a supercapacitor is fully discharged, it will look like a short to ground and will draw as much current as it can from the battery. The maximum battery current is determined by the following equation:

$I_{PEAK} = V_{BAT} / (R_{BAT}+R_{CAP}+R_{ROUTE})$.

A current limiting circuit can be as simple as resistor placed in series with the capacitor. However, a series-connected current-limiting resistor will lower the overall system efficiency and will impact the capacitor recharge time due to the very large RC time-constant.

Another limiting circuit places a current-limiting linear voltage regulator (LDO) between the supercapacitor and the battery to help charge the supercapacitor and manage peak battery currents. When using an LDO, the target supercapacitor voltage must always be lower than the battery voltage because LDOs do not have the ability to boost the battery voltage.

A third option, which will be the focus of the remainder of this article, uses a boost converter between the battery and the supercapacitor to create a fixed voltage rail capable of recharging the supercapacitor and supplying the average current requirement of the supercapacitor system.

The Supercapacitor System

Using the same load profiles and load controllers highlighted in Fig. 1, Fig. 3 utilizes a supercapacitor charger/controller that can help limit the peak battery current to manageable levels (around 500 mA) and keep the voltage drop due to the battery ESR to around 50 mV. In this example, the supercapacitor and the controller help decrease the peak current and ESR voltage drop by more than 85% without having to decrease the performance of the subsystem loads.

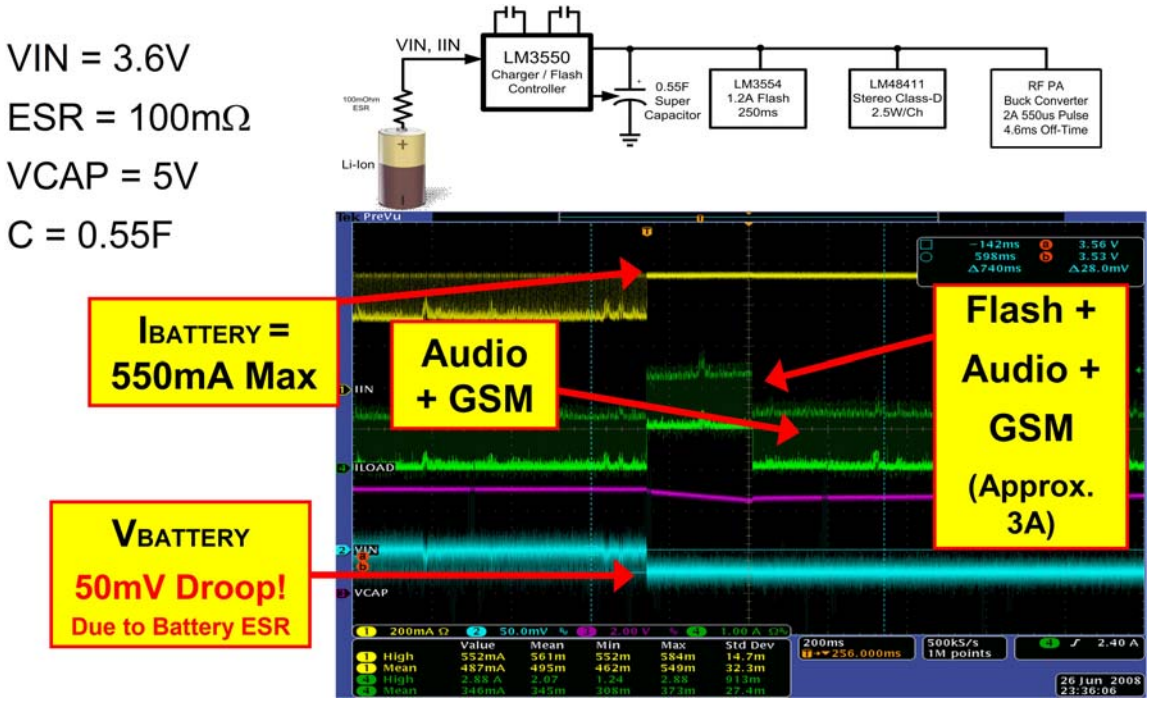

Fig. 3. *The LM3550 supercapacitor charger/controller limits the peak battery current to 550 mA, which restricts the battery's voltage drop due to battery ESR to 50 mV.*

Supercapacitor Management Requirements

With the dual-cell supercapacitor architecture there are some special requirements that are typically not encountered when dealing with other type of capacitors. The EDLC management IC must be able to handle these requirements to properly protect the EDLC and manage the supercapacitor power subsystem.

Input-current limiting. The supercapacitor subsystem management IC must have an input-current limit that is compatible with the battery and other systems being used in the mobile device. A supercapacitor subsystem should support high-current pulsed loads while not interrupting normal system functions. The product designer must first come up with a power budget for the different power domains (i.e. baseband processor, display, etc) present in the design.

Consider an example in which the battery has a 2-A current limit and the functions not associated with the supercapacitor can draw up to 1.4 A at any given time. In this case, picking a supercapacitor management IC with a 600-mA input current limit should prevent the design from triggering the battery overcurrent protection.

Switched-capacitor-boost and synchronous-inductive-boost converters are better suited to supercapacitor charging than an asynchronous-inductive-boost converter. Asynchronous converters cannot actively disconnect the output from the input. If the supercapacitor is discharged to some value below the battery voltage and the battery is connected to the system, there will be no way of limiting the charge current because the schottky diode will start to conduct and the current will flow in an uncontrolled manner. Synchronous- and switch-capacitor-based boost converters both have internally controlled FETs that can be used to limit the current that flows to the supercapacitor.

Start-up into a short. A supercapacitor management IC must be able to handle starting into an output short at the IC's rated input-current limit. When a supercapacitor with a capacitance of 0.5 F is fully discharged, it will look like a short to ground during the beginning of the charge cycle. Most power management ICs based on a boost architecture (whether it be inductive or switched capacitor) will run at the input current limit until the capacitor is close to reaching its target output voltage. At start-up, this condition requires that the management IC dissipate significant amounts of power across the device.

For example, if the battery voltage is 4.0 V and the management IC has an input current limit equal to 500 mA, assuming the supercapacitor is fully discharged (V_{CAP} = ground or 0 V), the IC must be able to initially dissipate 2 W across the part and still continue the charging process. As the supercapacitor voltage increases, the power dissipated across the IC will decrease.

High-impedance output mode. The subsystem management IC should be able to place the output of the boost converter into a high-impedance state when the subsystem goes into a shutdown state. This requirement prevents the EDLC from being discharged when not in use.

Cell-balancing. Dual-cell supercapacitors require a cell-voltage balancing scheme to prevent an overvoltage condition on either EDLC cell. Simple resistors can be used to balance the individual cell voltages, but these resistors will continually draw current away from the supercapacitor.

An active balancing scheme using an amplifier to drive the balance terminal is the preferred method to maintain EDLC cell balance. An effective active balance scheme must be able to source and sink current away from a given cell to ensure the voltage on each cell is equal to the total output voltage divided by two (see Figure 4).

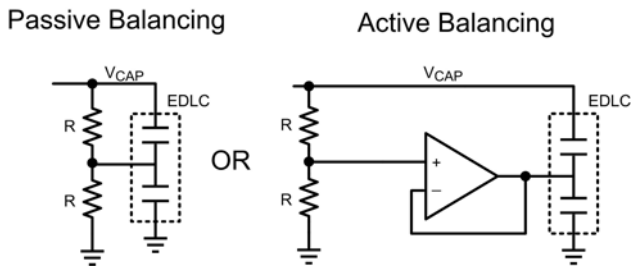

Fig. 4. *When dual-cell supercapacitors are employed to support the battery, resistors (circuit on left) or an amplifier (circuit on right) may be used to balance the individual cell voltages.*

A 3-A+ LED Flash

Besides the advantages already mentioned, the use of a supercapacitor subsystem allows LED flash arrays to be driven at current levels much higher than those allowed when a flash driver is connected to the battery alone. Depending on the capacitance value and the number of LEDs used, flash currents in excess of 5 A lasting for 33 ms are possible. At these current levels, the LED array can generate light exposure values (lux x seconds) comparable to that of a xenon flash, but with a much-thinner solution size. In addition, the LEDs can operate in a continuous movie mode—something the xenon cannot do. A further advantage of the LED solution is that it can be driven continuously at a lower current to support a movie mode "light" (i.e. a lower-performance movie mode.)

Drawbacks

For all of the supercapacitor subsystem advantages, there are a few design considerations that may prove less than ideal. The first is the physical size of the capacitor itself. While still thinner than a xenon-based solution, a typical supercapacitor capable of handling the 5.5-V operating rating can have an average height of 2 to 3 mm with a footprint measuring between 360 mm^2 and 400 mm^2. Accommodating a component of this size in a mobile device can prove difficult.

Additionally, supercapacitors today are not capable of surviving a standard reflow assembly process and require a secondary assembly step, which adds cost to production. Furthermore, when placed in a high-temperature environment, supercapacitors tend to swell and this swelling can lead to component damage and lifetime issues.

Conclusions

When using supercapacitors in a portable design, the ability to support numerous high-current load pulses simultaneously becomes possible. Supplying RF PA transmit pulses, high-power stereo drivers, and LED camera flashes while keeping battery current to a manageable level can help eliminate numerous design challenges (timing limitations, huge battery ESR drops, etc.)

Properly evaluating a supercapacitor driver/controller using the criteria mentioned in this article will help any design use the supercapacitor subsystem to its fullest potential while minimizing design headaches late in the design cycle. As the performance of the supercapacitors improve, (i.e. voltage rating and capacity increase, ESR and physical size decrease), more high-performance features will be added to the mobile handset, providing a richer user experience.

About the Author

Greg Lubarsky is a senior applications engineer with National Semiconductor's Grass Valley design center and works in the Mobile Devices Power group. He received his Bachelor of Science degree in Electrical Engineering from the University of California, Davis in 2002. Lubarsky has over seven years of experience as an applications engineer working with white LED backlight drivers, LED flash drivers and other power management electronics.

For further reading on supercapacitors, see the How2Power Design Guide and search the Component category and Capacitors subcategory.