Scoping Out the Best DC-DC Converter Design

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With today's proliferation of nonsolated, dc-dc converter solutions, there are a wide variety of options for fulfilling a power supply requirement. Designers have a choice of functionally complete, dc-dc converter modules and embedded solutions based on power supply ICs, each of which are offered by multiple vendors. Because of cost and other reasons, embedded solutions have become an increasingly popular approach. But finding the optimum embedded dc-dc solution is not a simple matter.

Even if the designer narrows the search to a single power IC vendor, the designer still needs to select the best combination of power supply IC and supporting components. For a given set of power supply input and output requirements, there may be 50 or more possible designs. To determine which design works best in the application, designers need to establish goals for their power supply such as low cost, small footprint or high efficiency.

Unfortunately, these goals are frequently in conflict with each other, adding to the complexity of finding the right solution. To address these challenges, semiconductor vendors are developing more-sophisticated product selection tools, which go beyond simple parametric searches and look-up tables, crossing into the realm of power supply design. An example is National Semiconductor's WEBENCH Visualizer, which allows real-time comparison between a large number of power supply design options. By presenting the design possibilities graphically, WEBENCH Visualizer enables designers to quickly grasp the possible design tradeoffs among many different solutions. A dc-dc converter design example presented here demonstrates this powerful capability.

Limitations of IC Selection Tools

To begin the power supply design, an engineer must first set specifications for input-voltage range, output voltage and load current (V_{IN} min, V_{IN} max, V_{OUT} and I_{OUT}). Then, the designer needs to determine which voltage regulator to use. This may be done through the use of a parametric catalog. A good catalog on a manufacturer's website allows filtering of results based on the previously mentioned parameters and others such as the switching frequency, package type and feature set. However, the user may still be left with a large number of choices. In addition, the hard-coded parametric values do not tell the whole story since they tend to be specific to the regulator, not the entire power supply design.

For example, for a stepdown (buck) application, if the output voltage is very close to the input voltage, the voltage drop across the power supply may be too great to maintain the output voltage within the maximum duty cycle specification for the switching regulator. This dropout voltage needs to be calculated for each supply in the list. For a boost application, the peak switch current is a function of the minimum input voltage, the output voltage and the efficiency of the regulator. This too must be calculated for each supply in the list.

For controllers, designers must find a suitable FET, which meets the application's voltage and current specifications, and which can be driven by the controller while maintaining a reasonable efficiency. This again, needs to be calculated for each possible option. Lastly, the user would like to look at key design values such as the total bill-of-materials (BOM) footprint, the efficiency and the price for each option.

Determining these values is very time consuming. It requires actually choosing a BOM, and doing calculations for currents and power dissipation for all possible candidates. The bottom line is that a lot of work needs to be done to get a good side-by-side comparison between options for the meaningful design values. National Semiconductor's WEBENCH Visualizer automates the process of calculating those design values needed to perform side-by-side comparisons. The WEBENCH Visualizer uses optimized algorithms to calculate the BOM and operating values, which allows the data to be generated in seconds, allowing real-time comparison of many power supply design options.

Using WEBENCH Visualizer

As an example, consider an application requiring a stepdown converter with a 14-V to 22-V input range and a 3.3-V output at 2 A. Figure 1 shows a graph of the calculated component footprint, efficiency and BOM cost for 48 different power supply options that satisfy these input and output criteria.

The y axis of the graph shows component footprint, the x axis shows efficiency and the bubble size shows the BOM cost. The variation in the results is significant with the footprint ranging from 286 mm^2 to 752 mm^2, the efficiency from 77% to 91% and the BOM cost from $2.46 to $5.52.

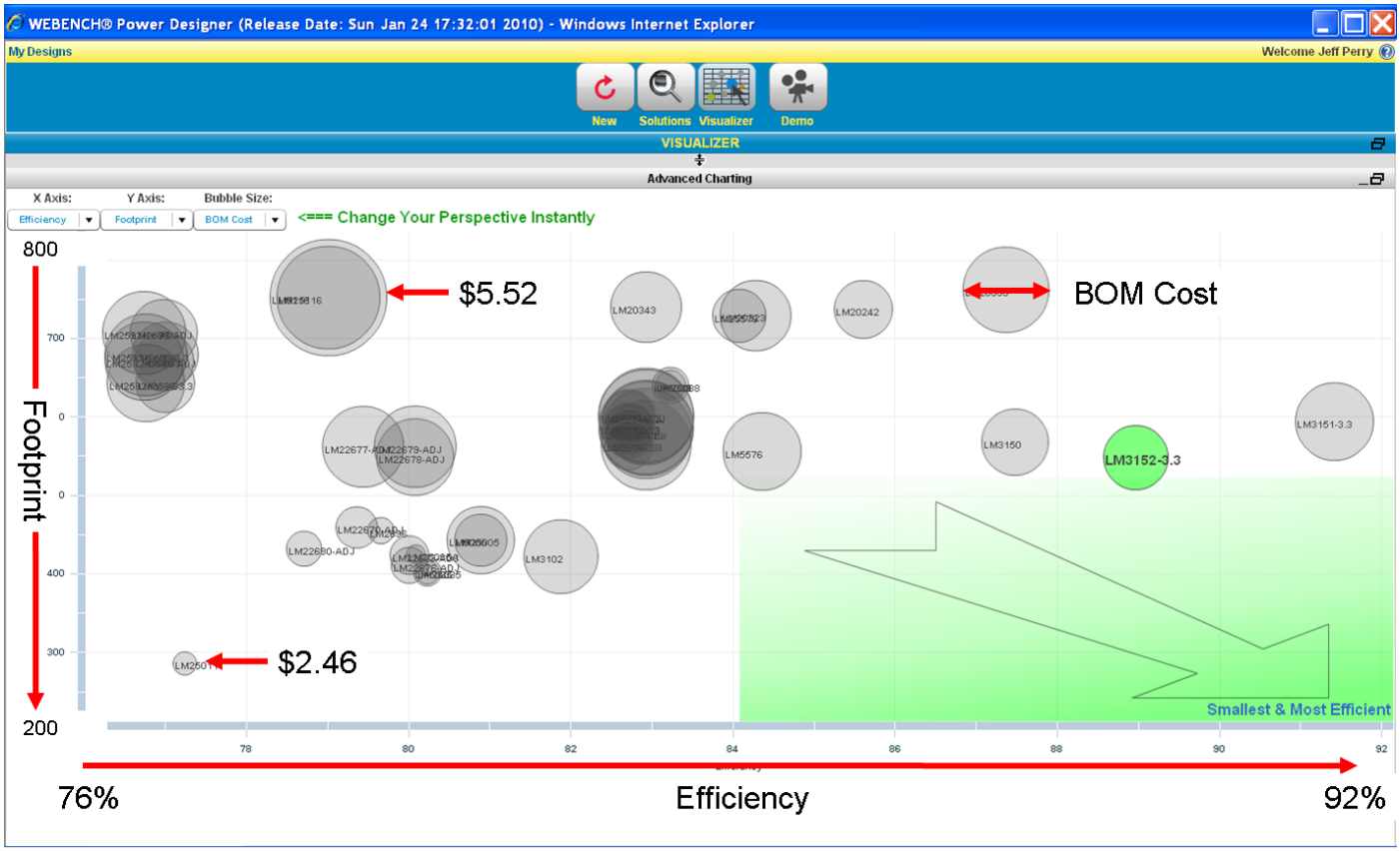

Figure 1. Graph of efficiency, footprint and BOM cost for 48 power supply options. The y axis of the graph shows footprint, the x axis shows efficiency and the bubble size shows the BOM cost.

The general trend of results is from the lower left portion of the graph to the upper right. This is because designs which have small footprint generally have low efficiency and designs with high efficiency generally have large footprint. The primary cause of this difference is the switching frequency. If we change the bubble size to represent frequency, we see the results in Figure 2.

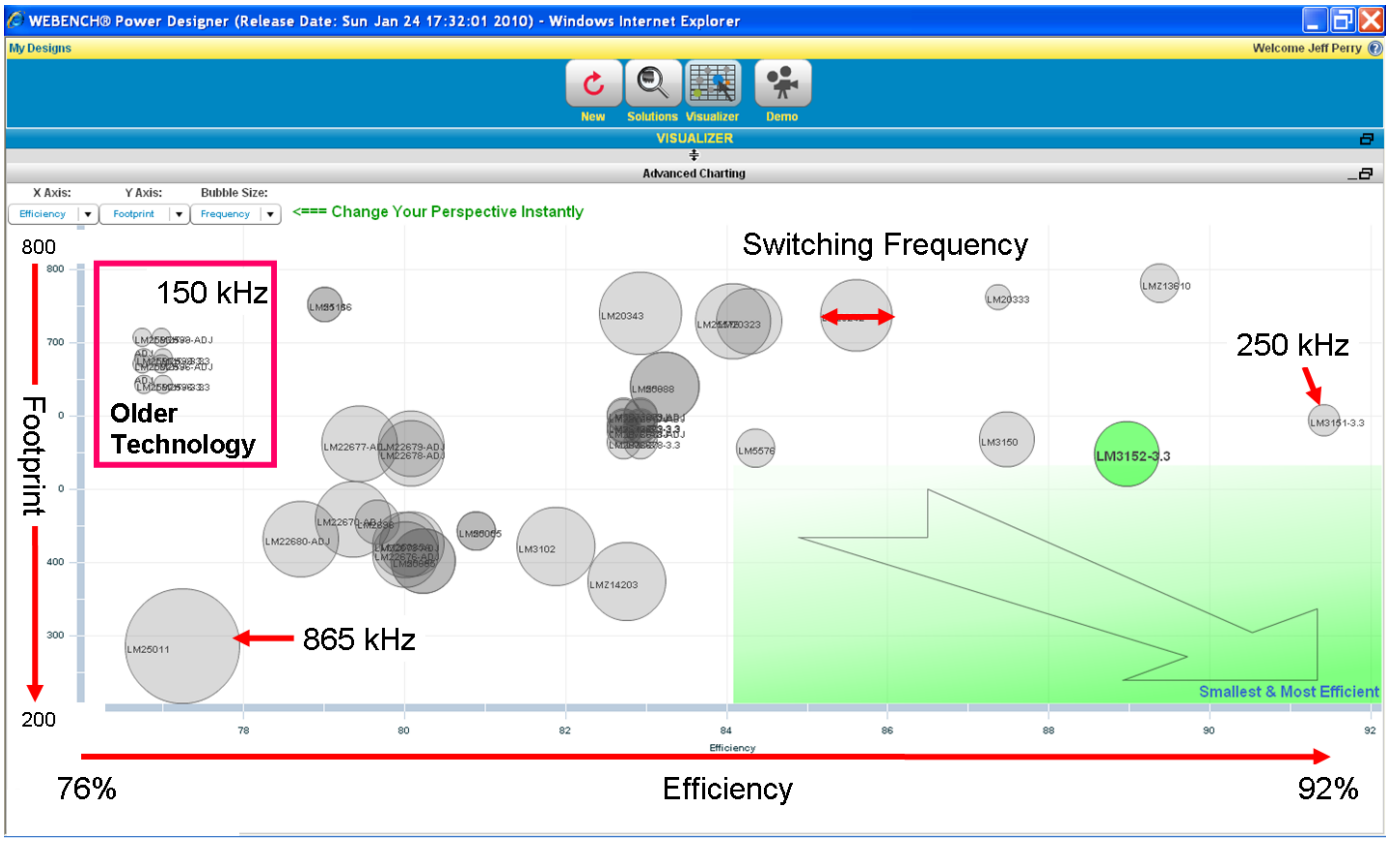

Figure 2. Graph of efficiency, footprint and switching frequency for 48 stepdown converter options. The y axis of the graph shows footprint, the x axis shows efficiency and the bubble size shows the frequency.

We see that for the most part, the designs with higher switching frequency (large bubble size) are in the lower left portion of the graph indicating smaller footprint, but lower efficiency. As we go to the upper right of the graph, signifying higher efficiency but larger footprint, the switching frequency tends to be lower as indicated by the smaller bubble size. These results make sense from the standpoint of ac switching losses.

Figure 3 shows a representation of voltage and current in a FET during a switching period in a typical buck switching regulator. During the rise and fall times when the switch is turning on and off, both voltage and current in the switch are non zero, and power is dissipated as voltage times current as shown by the orange areas in the figure. These rise and fall times are not fundamentally dependent on the switching frequency and tend to be fixed. So as the frequency is increased and the switching time period is decreased, the rise and fall times become a larger percentage of the switching time period and the efficiency drops. Conversely, with lower switching frequency and longer switching time period, the rise and fall times are a lower percentage of the switching time period and the efficiency improves.

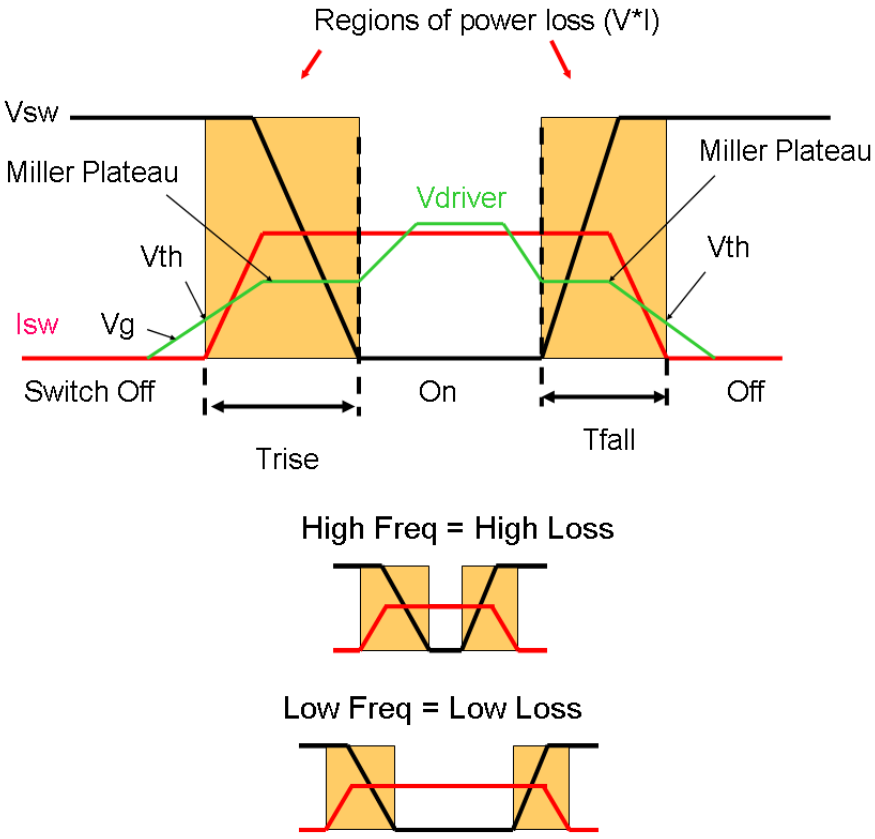

Figure 3. Diagram of switching losses as a function of the switch rise and fall time. Orange areas show regions of power loss where voltage and current are non zero. These areas decrease as a percentage of the switching period as the frequency decreases.

The tradeoff to be made at lower switching frequency is the component footprint. This is driven primarily by the inductor size. As shown in Figure 4, the inductor ripple current and thus peak switch current are proportional to the on time and inversely proportional to the inductance by the fundamental inductor equation:

$dI = (1/L) \times V \times dt$

where dI is the inductor ripple current, L is the inductance, V is the voltage applied to the inductor and t is the on time of the switch. As the frequency is lowered, the on time increases and the peak switch current goes up if the same inductance is used. To maintain the desired peak switch current, the inductance must be increased and this increases the footprint of the inductor.

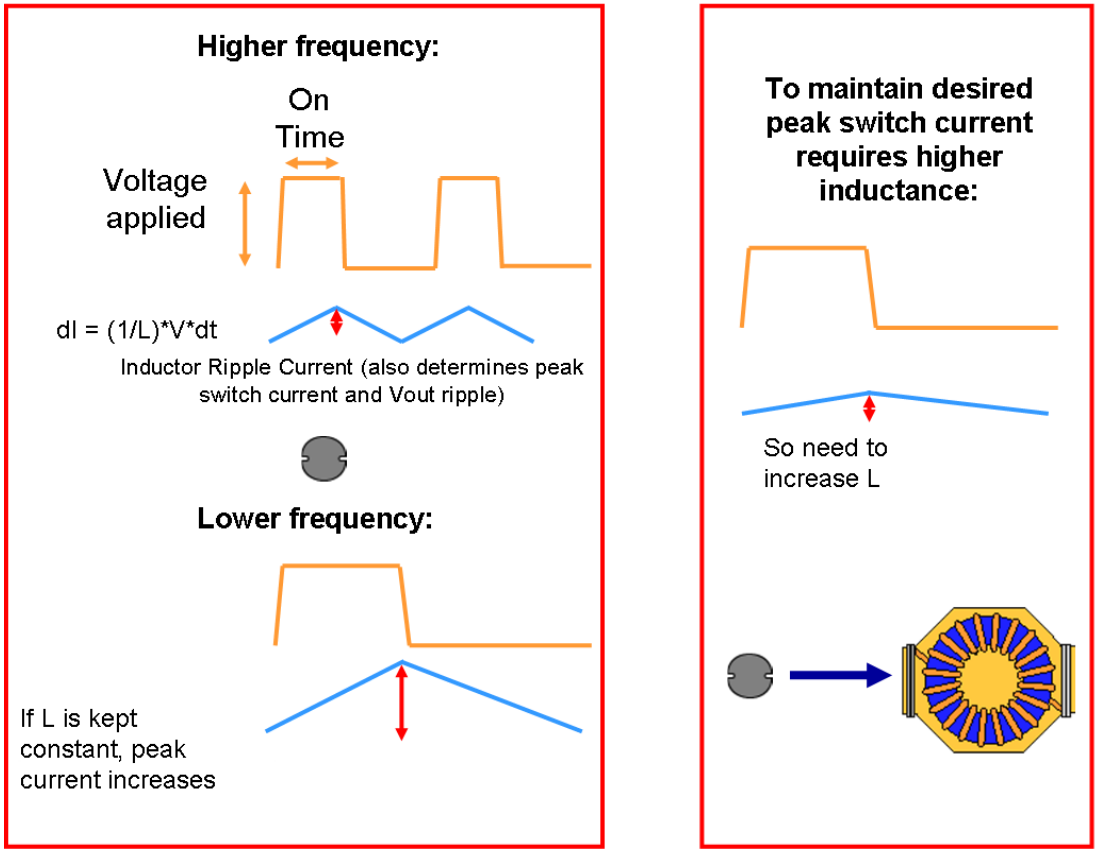

Figure 4. To keep the peak current constant, the inductance must increase as the switching frequency is lowered.This results in larger inductor footprints.

Returning to Figure 2, the most desirable designs would be those in the lower right corner, which have both high efficiency and small-footprint. But as previously explained, this is difficult to achieve due to fundamental tradeoffs. Another notable trend is that as we go to the lower left of the plot with smaller footprint, the price tends to go down. This is largely because smaller passive components tend to be cheaper.

Since many voltage regulators have adjustable frequency, we can optimize the designs to have high efficiency by setting the frequency lower and choosing passive components with lower power dissipation. In tools such as WEBENCH Designer, this can be done using a simple knob control to specify high-efficiency optimization.

Figure 5 shows an array of designs which target high efficiency. We see that there are now a number of designs with efficiency above 90% with a high of 93%. At the same time, the range of component footprints has increased and now goes as high as 1800 mm^2, which is a fundamental tradeoff made to achieve high efficiency. Several designs to the right side of the plot, with higher efficiency, utilize controllers that have an external FET.

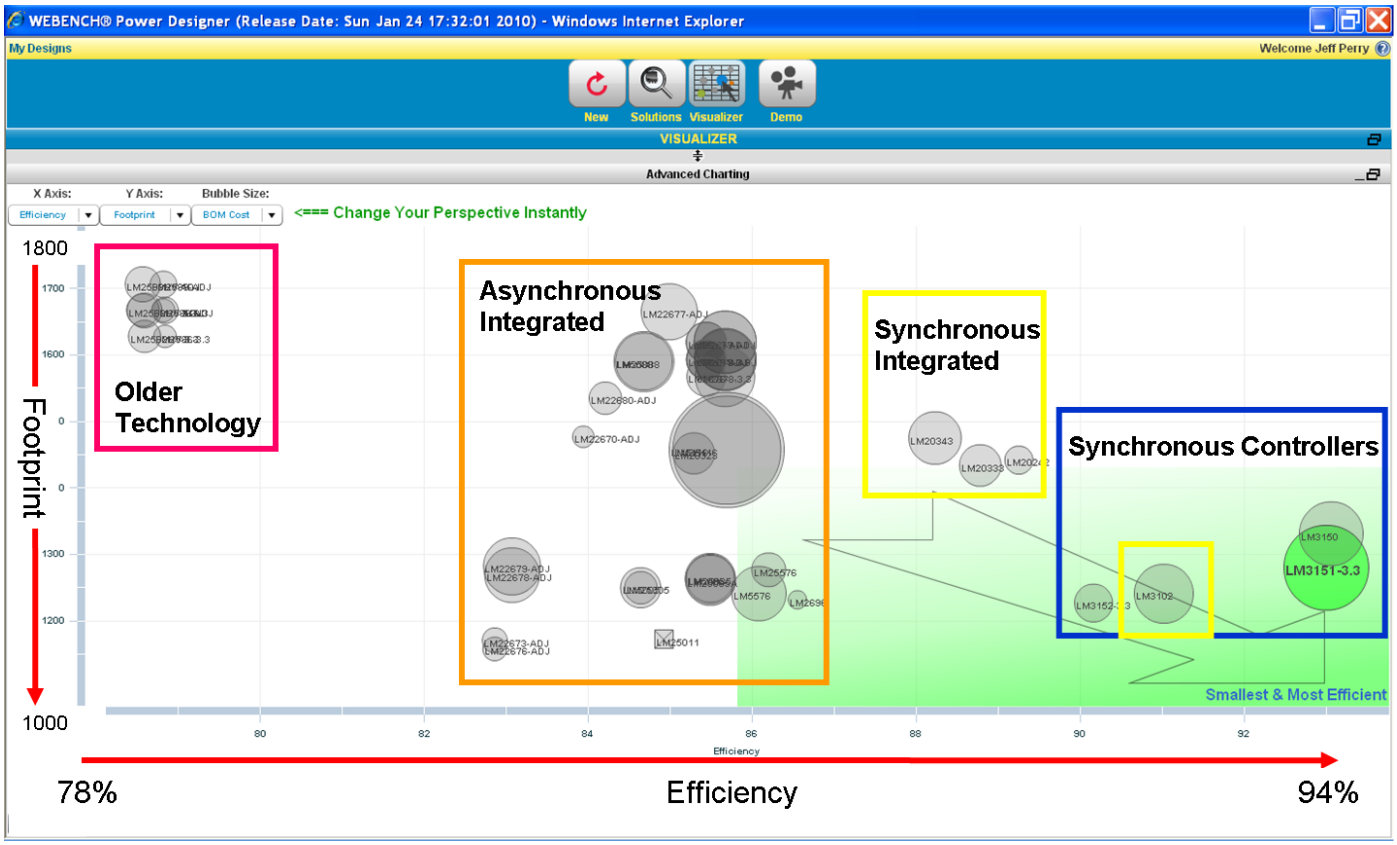

Figure 5. Graph showing power supply designs optimized for high efficiency. The x-axis shows efficiency, the y-axis component footprint and the bubble size shows the BOM cost.

These designs tend to be efficient because the FETs can be selected to have low $R_{DS(ON)}$ to reduce dc losses and the ac losses are kept low due to the low frequency. On the negative side, controllers can be more difficult to design with than integrated switch devices because the FET selection and also the board layout tend to be more complex.

Designs on the right also feature synchronous switching, which uses a FET instead of a catch diode for the low-side switch-node. FETs with low $R_{DS(ON)}$ tend to have lower power dissipation than diodes, which have a high fixed voltage drop of 0.4 V to 0.5 V at the currents and voltages for this design scenario.

As we move to the left side of the plot toward lower efficiency, we see some devices that seem to violate the general trend of lower footprint. This is because some of the designs use a part with a fixed frequency, which is higher than those on the right side of the graph. We also see a group of designs in the upper left which utilize older technology switches and have low efficiency and high footprint. These parts may still be considered viable by some who have used them successfully for a long time. But the sacrifice in efficiency and footprint is obvious.

At the opposite end of the spectrum, we can target the designs for small footprint. Figure 6 shows the results of this type of optimization. This is accomplished by increasing the switching frequency, and choosing components with smaller size. The results of this optimization show that the footprints have indeed been reduced and are as low as 244 mm^2. But at the same time, the efficiency of the smallest design has dropped to approximately 72%.

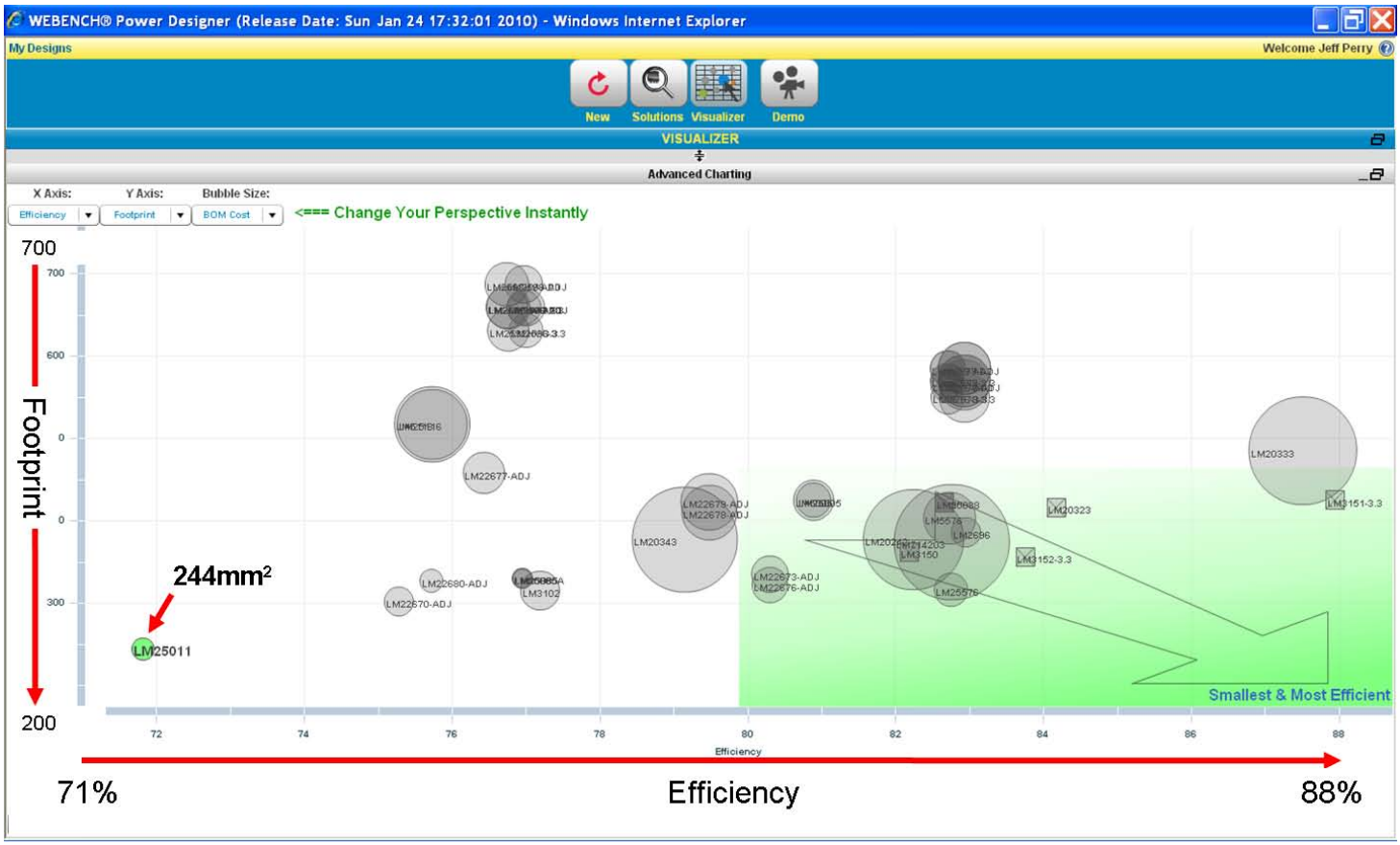

Figure 6. Graph showing power supply designs optimized for small footprint. The x-axis shows efficiency, the y-axis component footprint and the bubble size shows the BOM cost.

After examining all the options for our design example, we can identify the limits on optimization with respect to footprint cost and efficiency. These results are summarized in the table.

Table. Stepdown converter design options with one parameter optimized.

Optimized Design Parameter	Footprint	Efficiency	B.O.M. Cost
Smallest- footprint design	244 mm^2	72%	$2.69
Lowest-cost design	425 mm^2	80%	$2.31
Highest-efficiency design	1246 mm^2	93%	$5.06

As can be seen from these optimized results, the general trends we investigated hold true. The smallest-footprint design has the lowest efficiency, and the highest-efficiency design has the largest footprint. The lowest-cost design is somewhere in between.

It is up to the designer to choose which option is best or perhaps select a compromise between parameters. Thus, it can be seen that using the latest visualization and optimization tools, such as National Semiconductor's WEBENCH Designer, a power supply designer can quickly sift through a large number of design choices to obtain the desired result in a matter of minutes. This is a task that would otherwise take many days of work, if it were possible at all.

About the Author

Jeff Perry is the senior development manager for National Semiconductor's WEBENCH online design environment. He spent the first part of his career in semiconductor process engineering and the latter portion in power supply applications and development. He has been involved with the WEBENCH tool since it's inception in 1999. Jeff graduated from UCLA with a BS in physics and received an MBA from San Jose State University. He holds 10 patents.

For more information on design tools that aid in dc-dc converter design, see Power Around the Web and check out the Design Notes and Tools category with its descriptions of various sites that offer power supply design tools. Also, see the How2Power Design Guide, and search the Design Area category and the Modeling and Simulation subcategory.