## How2 Get The Most Out Of GaN Power Transistors

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Power MOSFETs first started appearing in 1976 as alternatives to bipolar transistors. These majority carrier devices were faster, more rugged, and had higher current gain than their minority-carrier counterparts. As a result, switching power conversion became a commercial reality. Ac-dc switching power supplies for early desktop computers were among the earliest volume consumers of power MOSFETs, followed by variable-speed motor drives, fluorescent lights, dc-dc converters, and thousands of other applications that populate our daily lives.

In June 2009, Efficient Power Conversion Corporation (EPC) introduced the first enhancement-mode GaN (eGaN) on silicon power transistors designed specifically as replacements for power MOSFETs [1]. These products were also designed to be produced in high volume at low cost using standard silicon manufacturing technology and facilities. The eGaN structure is relatively simple as shown in Figure 1.

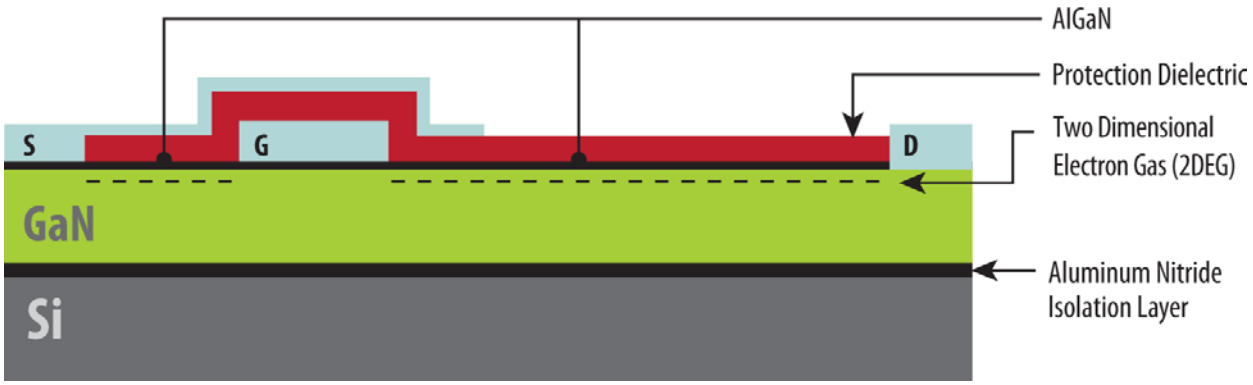


*Figure 1. GaN-on-silicon devices have a very simple structure similar to a lateral DMOS device and can be built in a standard CMOS foundry.*

Thirty years of silicon power-MOSFET development taught us that one of the key variables controlling the adoption rate of a disruptive technology is how easy the new technology is to use. This principle has guided the design of EPC's enhancement-mode GaN transistors. To explain the eGaN devices' ease-of-use, we must first review how they operate and highlight both their similarities and differences versus today's power MOSFETs. With that as background, we'll describe the gate-drive requirements for eGaN transistors, and possible discrete and IC-based gate-driver designs.

### GaN Power Transistor Characteristics

As with silicon power MOSFETs, applying a positive bias to the gate relative to the source of a GaN power transistor causes a field effect, which attracts electrons that complete a bidirectional channel between the drain and the source. When the bias is removed from the gate, the electrons under it are dispersed into the GaN, recreating the depletion region and, once again, giving it the capability to block voltage.

To obtain a higher-voltage device, the distance between the drain and gate is increased. Doing so increases the on-resistance of the transistor. However, as the mobility of electrons in a GaN HEMT (high electron mobility transistor) is very high, increasing its blocking-voltage capability has much less of an impact on the device's on-resistance than would be the case with a silicon power MOSFET.

Figure 2 compares the theoretical resistance-times-die area voltage limits of GaN, silicon carbide (SiC) and silicon (Si) as a function of voltage [2]. EPC's first generation of devices is shown as well. Please note that after 30 years of silicon MOSFET development, silicon has approached its theoretical limits. Progress in silicon has slowed to the point where small gains incur significant development cost. In contrast, GaN is young in its life cycle, and will see significant improvement in the years to come.

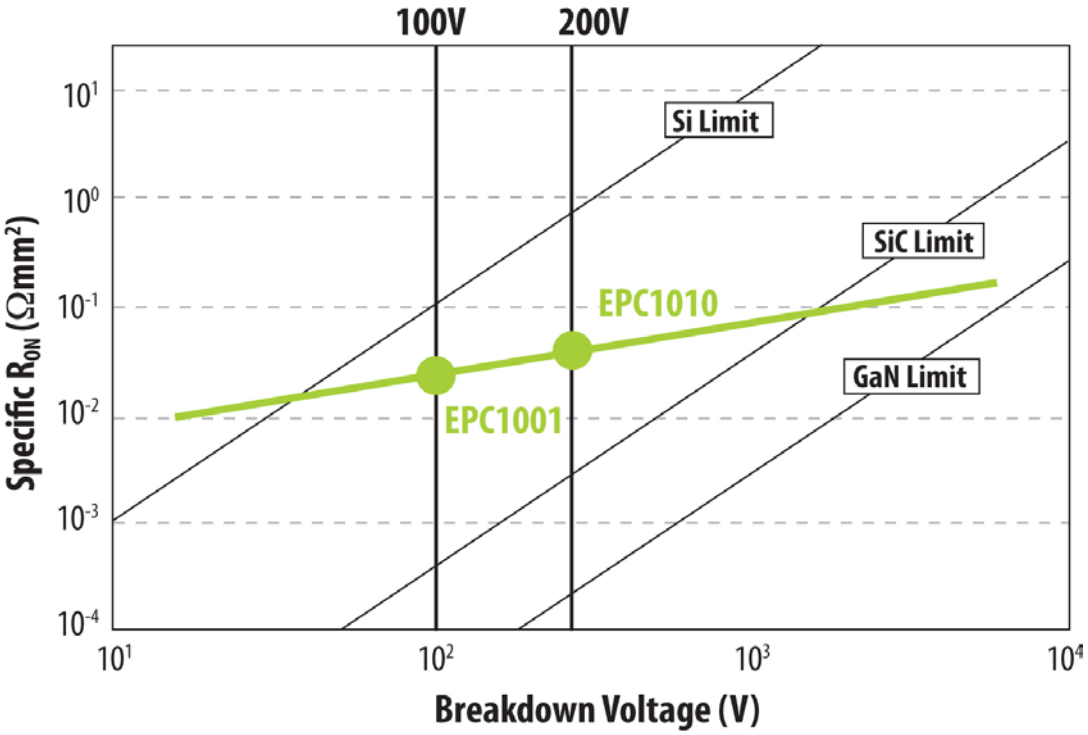


*Figure 2. Theoretical resistance times die area limits of GaN, silicon, and silicon carbide versus voltage.*

### *Gate Threshold And Maximum Gate Voltage*

The threshold of eGaN is generally lower than that of silicon MOSFETs. This poses less of a limitation to the designer because there is an almost flat relationship between threshold and temperature along with the very low gate-to-drain capacitance ($C_{GD}$). Figure 3 shows the transfer characteristics curve for the EPC1001, 100-V, 7-mΩ transistor. Please note the negative relationship between current and temperature. This allows excellent current sharing in the linear region and in diode conduction, which will be explained later. Being that the device starts to conduct significant current at 1.6 V, care must be taken to ensure a low-impedance path from gate to source when the device needs to be held off during dV/dt in a rectifier function.

EPC's eGaN devices have a maximum gate voltage of +6 V/-5 V, which is more than adequate to fully enhance the channel. However, lower gate-to-source voltage limits compared with silicon MOSFETs mean a more accurate gate-drive voltage is required, but this also means total gate-drive losses will be lower.

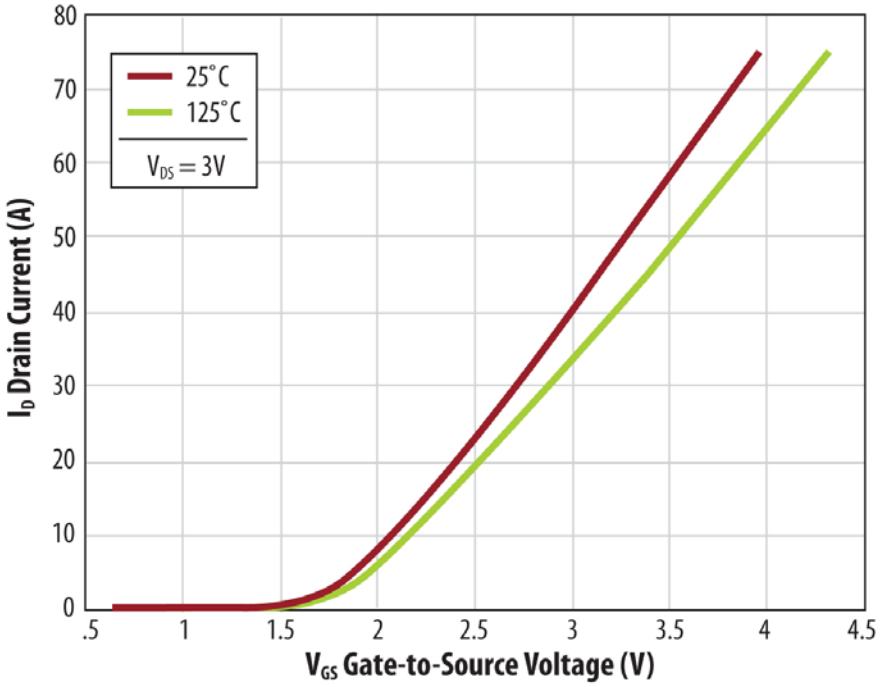


*Figure 3. Transfer characteristics curve for the EPC1001, 100-V, 7-mΩ transistor.*

## Resistance

$R_{DS(ON)}$ versus $V_{GS}$ curves are similar to those of MOSFETs. EPC first-generation eGaN are designed to operate with 5-V drive. Figure 4 shows the set of curves for the EPC1001. The curves show that $R_{DS(ON)}$ continues to decrease as the absolute maximum gate voltage is approached. As there is negligible gate-drive loss penalty, eGaN should be driven with 5 V. The temperature coefficient of $R_{DS(ON)}$ for the eGaN transistor is also similar to that of the silicon MOSFET in that it is positive, but the magnitude is significantly less. At 125°C, the $R_{DS(ON)}$ of the 100-V eGaN is 1.45 times the 25°C value compared to 1.7 times for silicon.

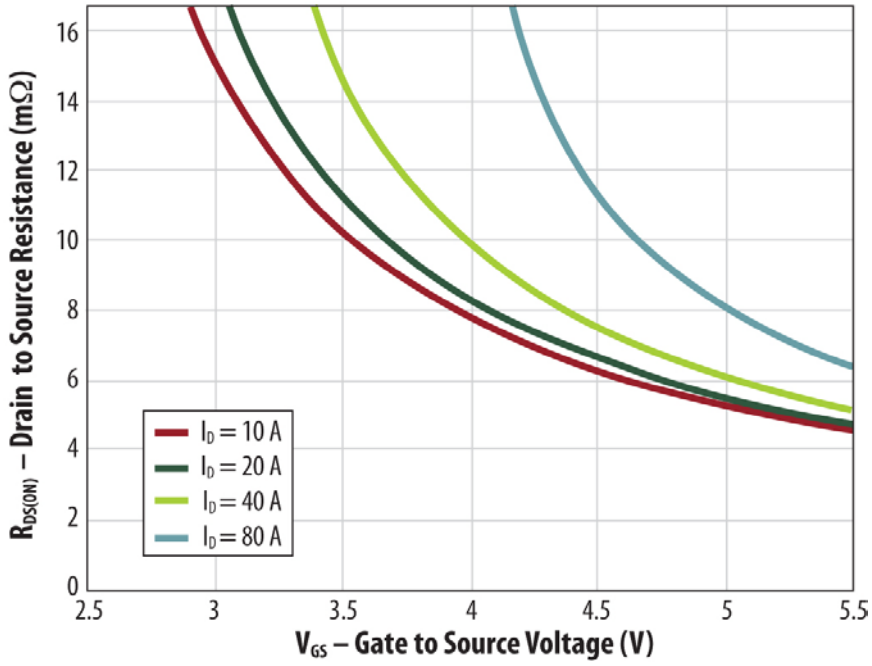


*Figure 4. EPC1001 $R_{DS(ON)}$ versus $V_G$ at various currents.*

### Capacitance

In addition to the low $R_{DS(ON)}$, the lateral structure of the eGaN transistor makes it a very low-charge device. It has the capability of switching hundreds of volts in just a few nanoseconds, enabling multiple-megahertz switching. This capability leads to smaller power converters, and higher-fidelity class D audio amplifiers. Most important for switching performance is $C_{GD}$. With the lateral device structure, $C_{GD}$ comes only from a small corner of the gate. An extremely low $C_{GD}$ leads to eGaN's ability to switch voltage very rapidly.

Capacitance curves for the EPC1001 are shown in Figure 5 [3]. Again, eGaN looks similar to silicon except that, for a similar on-resistance, the capacitances are significantly lower and "flatten out" much sooner. $C_{GS}$ consists of the junction from the gate to the channel, and the capacitance of the dielectric between the gate and the field plate. $C_{GS}$ is large when compared with $C_{GD}$, but since $C_{GD}$ flattens out to a non-negligible value quickly, this cumulative $Q_{GD}$ change does impact dV/dt immunity with increasing drain-to-source voltage.

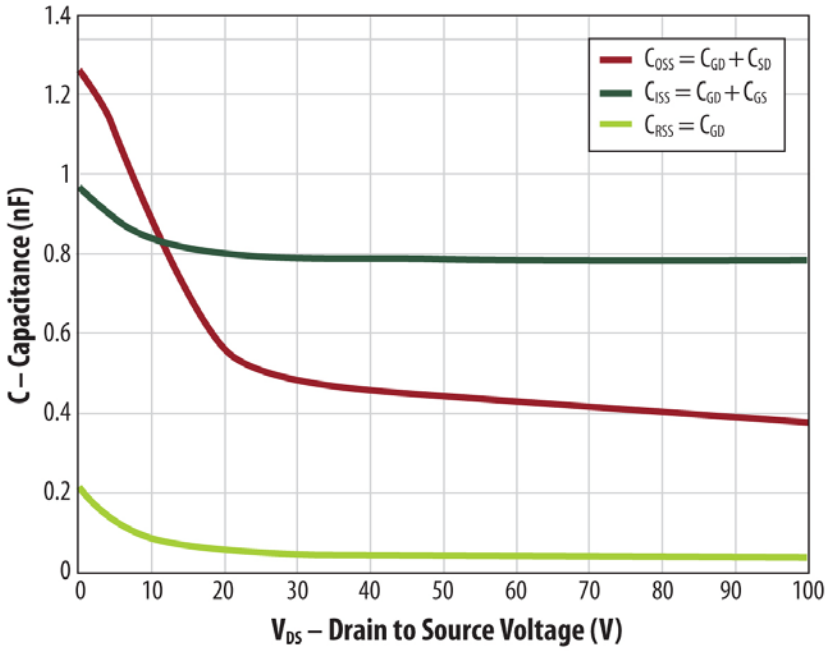


*Figure 5. EPC1001 capacitance curves.*

In short, the 40-V devices (EPC1014 and EPC1015) have excellent Miller ratios ($Q_{GD}/Q_{GS}$ < 0.6), while the 150-V and 200-V devices (EPC1010, EPC1011, EPC1012, and EPC1013) have Miller ratios of >1.9 and therefore require some careful gate-driver design (more on this later). Overall, the value of $C_{GS}$ is still small when compared with silicon MOSFETs, enabling very short delay times and excellent controllability in low duty-cycle applications. $C_{DS}$ is also small, being limited to the capacitance across the dielectric from the field plate to the drain.

### Series Gate Resistance And Leakage

Series gate resistance ($R_G$) limits how quickly the capacitance of any field effect transistor can be charged or discharged. Consistent with the high switching-speed capability of eGaN, EPC transistors have been designed to have gate resistances of a couple tenths of an ohm. This low gate resistance also helps with dV/dt immunity.

The eGaN devices do not use an insulator in the gate. For this reason, the gate leakage current is higher than that of silicon MOSFETs. Designers should expect gate leakage on the order of 1 mA. As these devices have low gate-drive voltage, losses associated with gate leakage are low and therefore this is not an issue in most applications.

### Drain-Source Breakdown

As of the date of this writing, EPC's first-generation eGaN has not been characterized for operation where the device is forced into drain-source breakdown (Since there are no minority carriers in eGaN conduction, devices do not avalanche).

Not having an avalanche rating means switch-node voltage overshoot should be limited through optimum layout, and the correct voltage rating should be used so devices do not experience excursions beyond their maximum drain-source rating.

### *Body Diode*

The last part of the performance picture is that of the so-called "body diode". As seen from Figure 1, EPC's eGaN structure is a purely lateral device, absent of the parasitic bipolar junction common to silicon MOSFETs. As such, reverse bias or "diode" operation has a different mechanism but similar function. With zero bias from gate to source, there is an absence of electrons in the region under the gate. As the drain voltage is decreased, a positive bias on the gate is created relative to the drift region, injecting electrons under the gate. Once the gate threshold is reached, there will be sufficient electrons under the gate to form a conductive channel. The benefit of this mechanism is that there are no minority carriers involved in conduction, and therefore no reverse-recovery losses.

Although $Q_{RR}$ is zero, the output capacitance ($C_{OSS}$) still has to be charged and discharged with every switching cycle. For devices of similar $R_{DS(ON)}$, eGaN transistors have significantly lower $C_{OSS}$ than silicon MOSFETs. As it takes a threshold voltage to turn on eGaN in the reverse direction, the forward voltage of the "diode" is higher than for silicon transistors. As with silicon MOSFETs, to reduce losses, care should be taken to minimize diode conduction.

Table 1 summarizes the similarities and differences between a silicon power MOSFET rated at 100-V $V_{DS}$ and a similarly rated eGaN transistor.

Table 1: A comparison between silicon and GaN characteristics.

| | **Typical 100-V Silicon** | **100-V eGaN** |
|---|---|---|
| Maximum gate-source voltage | ±20 V | +6 V and -5 V |
| Avalanche capable | Yes | Not rated |
| Reverse-direction 'diode' voltage | ~1 V | ~1.5 V to 2.5 V |
| Body-diode reverse-recovery charge | High | None |
| Gate-to-source leakage | A few nanoamps | A few milliamps |
| Gate threshold | 2 V to 4 V | 0.7 V to 2.5 V |
| Internal gate resistance | >1 Ω | <0.6 Ω |
| dV/dt capacitance (Miller) ratio $Q_{GD}/Q_{GS}$ | 0.5 to 0.7 | 1.1 |
| Change in $R_{DS(ON)}$ from 25°C to 125°C | >+70% | <+50% |
| Change in $V_{TH}$ from 25°C to 125°C | -33% | -3% |

### *The "Ideal" eGaN Gate Drive*

To understand the differences between an eGaN-specific gate drive and a generic MOSFET driver, it is necessary to consider what characteristics an "ideal" eGaN gate drive would have.

Such an "ideal" gate-drive solution (IC or discrete) is best considered as two separate functions: (1) the gate driver itself, which converts a high-impedance logic input into a low-impedance source to drive each of the power-device gates directly and (2) the level-shifting, delay-matching and other logic circuitry that assures that the input logic is reproduced correctly and with proper timing at the two power-device gates.

The important gate-driver characteristics are:

- Pull-down resistance as low as 0.5 Ω. With dV/dt slew rates of 20 V/ns to 30 V/ns or more, the risk of Miller turn-on and shoot-through becomes a concern for the higher-voltage devices. The gate-drive pull-down resistance must be minimized for maximum dV/dt immunity.

- An accurate gate-drive supply voltage. There is only 1 V of headroom between the recommended gate-overdrive voltage (5 V) and the absolute maximum rating (6 V). This accuracy requirement is more difficult to achieve for a bootstrapped supply.

- Adjustable pull-up resistance for EMI and voltage-overshoot control. In half-bridge applications of MOSFETs, a resistor with an anti-parallel diode is typically used for this purpose. With eGaN, the need for minimizing pull-down resistance means that this resistor and anti-parallel diode connection is not

recommended. The simplest general solution is to split the gate pull-up and pull-down connections and allow the insertion of a discrete resistor as needed.

- Low gate-drive loop impedance. At these high switching speeds, the impact of the gate-drive interconnection impedance also becomes important, requiring the gate drive to be placed as close as possible to the GaN power device.

The important level-shifting and delay-matching characteristics are:

- A 5-ns ±2-ns deadtime interval to minimize 'body-diode' conduction losses. As with silicon, the effective deadtime increases with load as turn-on time increases. Ideally this could be compensated in the gate drive, but such compensation is not a necessity. For higher-voltage devices, this interval is less critical as power levels and the switching period typically increase.

- A ±2-ns propagation-delay matching. Propagation delays from input to output for both high-side and low-side need to be matched to a much greater accuracy as determined by the deadtime requirement above. This delay matching avoids cross conduction or shoot through. The actual delay itself and its variation with temperature are less important.

- A >50-V/ns dV/dt immunity. Switching dV/dt is typically 30 V/ns or higher. Therefore, high dV/dt immunity is required to avoid 'accidently' turning on (or off) both power devices due to the dV/dt glitch.

For nonsynchronous or 'self-driven' gate drives, level shifting and delay matching are not relevant.

### *Discrete Gate-Drive Solutions*

Although there are no eGaN-specific gate-drive ICs on the commercial market as of the date of this writing, there are a variety of circuits available with adequate drive capability. However, it's relatively straightforward to employ a discrete solution.

Considering just the gate-driver element, a simple discrete solution is shown in Figure 6 and works for both ground-referenced (low-side) and floating (high-side) drivers. This solution requires an accurate external ~5.6-V supply (depending on the effective forward drop of the bootstrap diode) to supply both high-side and low-side drivers through identical "matching" diodes to achieve the 5.0-V gate drive. M2 should be chosen to have 500 mΩ or lower $R_{DS(ON)}$, while R2 can adjust the effective pull-up resistance (to control voltage overshoot and EMI ringing) without impacting the pull-down impedance. During layout, the loop between the EPC eGaN and the discrete (or IC) gate drive should be minimized.

Discrete MOSFETs M1 and M3 should be scaled so they can be driven with a higher impedance (logic-level input) source while still being able to drive M2 and M4. Resistor R1 is added to limit cross conduction between M1 and M3 and eliminate cross conduction in M2 and M4. For applications with only ground-referenced eGaN devices, the diode can be removed and an accurate 5.0-V supply can be used to directly power the discrete driver.

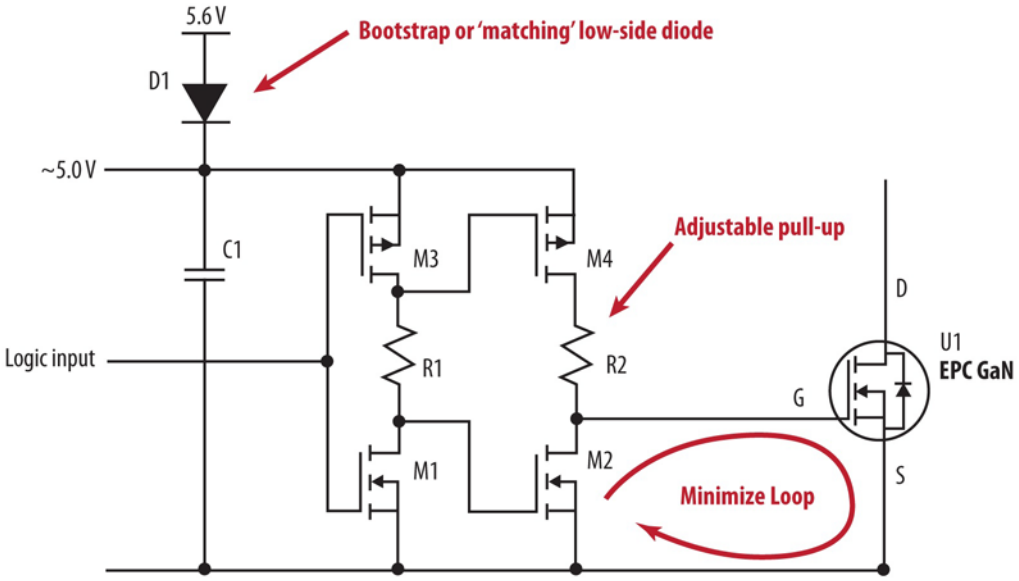


*Figure 6. Discrete eGaN gate-driver solution.*

Apart from being compatible with all 5-V-logic control ICs, this discrete solution can also be combined with higher logic voltage ICs where no 5-V-logic versions exist (e.g. level shifters above 100 V). Figure 7 shows an example of adding a 5.0-V regulator between the level-shifting/gate-drive IC and the discrete-driver solution. By placing the regulator before the discrete MOSFETs, the pre-drive MOSFETs (M1 and M3 in Figure 6) provide logic translation from the higher voltage to 5 V. This also lengthens the gate pulse by only speeding up the gate turn-on, which can be advantageous when the deadtime is already too large. Alternatively, the regulator can be placed between the pre-drive and drive stages, thereby shortening the gate pulse.

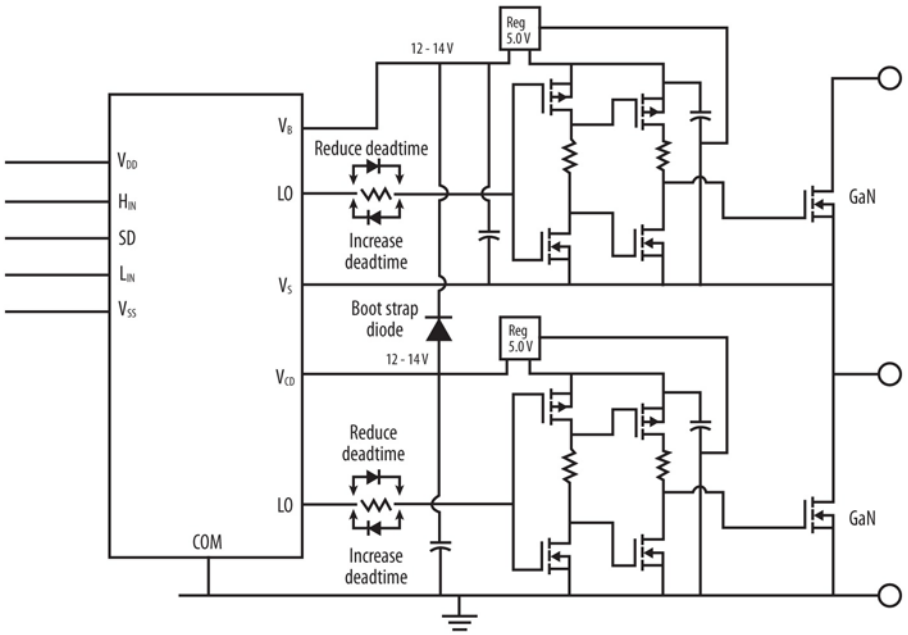


*Figure 7. Discrete gate-drive solution paired with higher logic voltage level-shift IC.*

## Gate-Driver ICs

There are also a number of commercially available gate-driver ICs that are adequate for driving eGaN devices. As low pull-down impedance is required, these ICs tend to be single gate-drive buffer ICs with very high-current drive capability. Please note that for the 40-V EPC devices (EPC1014 and EPC1015), this pull-down resistance requirement can be relaxed. A partial list of these gate-drivers is given in Table 2. It should be noted that some may not meet the 0.5-Ω pull-down requirement, which may not be necessary, depending on the actual dV/dt and the eGaN device used.

Table 2: Some current gate-drive ICs suitable for eGaN transistors.

| Manufacturer | Part number | Typical pull-down resistance |
|---|---|---|
| Fairchild | FAN3121/22 | >9A[a] |
| | FAN3123/24 | >4A[a] |
| Intersil | EL7158 | 0.5 Ω[b] |
| IXYS | IXDE509 | 0.7 Ω |
| Maxim | MAX5048 | <0.5 Ω |
| | MAX15024 | 0.5 Ω |
| National | LM5110/12 | 1.4 Ω[c] |
| Micrel | MIC4421/2 | 0.8 Ω |
| | MIC4451/2 | 0.8 Ω |
| Microchip | TC4421/2A | 0.8 Ω |
| | TC4451/2 | 0.9 Ω |
| Texas Instruments | UCC27321/2 | 1.1 Ω |
| | TPS28225/6 | >1 Ω |

Notes:
a Resistance not given
b Used on EPC9001/2 development boards
c Negative pull-down supply possible on LM5112

## Level Shifters And Logic Circuitry

Whether a discrete or IC solution is used to drive the eGaN device, the requirement for minimizing deadtime and controlling propagation delay is still a concern. In general, MOSFET-friendly level-shifter ICs have at least 20-ns deadtime, and this value tends to increase with the level-shifter voltage rating. As these ICs have some drive capability, a simple RCD circuit (see Figure 8) can be placed on the output to slow down turn-off and decrease deadtime. Care should be taken not to reduce the deadtime too much to cause cross conduction as the variation in deadtime of the driver from part-to-part or over temperature can be significant. Such modifications will also affect maximum and minimum pulse widths.

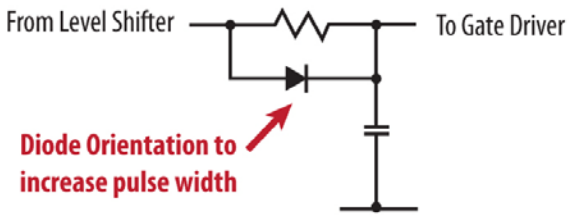


*Figure 8. Simple RCD circuit to adjust gate-drive pulse width.*

Apart from level-shifter ICs, the transfer of gate-pulse information across a high dV/dt barrier can also be achieved through a pulse transformer, optocoupler or by other means (e.g. iCoupler) and these may be realistic options for higher-voltage and higher-power applications.

## Switching Results

An experiment was conducted in which the generalized discrete gate-drive circuit from Figure 6 was used to drive a half-bridge consisting of two 200-V EPC1010 devices. The detailed schematic for this circuit is shown in

Figure 9 and the resulting waveforms are shown in Fig. 10. These are the waveforms for a 100-V-to-10-V, 7-A buck circuit operating at 400 kHz. Diode conduction can clearly be seen, while the turn-on time is less than 3 ns and dV/dt slew rates are as high as 40 V/ns. The use of a driver-stage MOSFET with an $R_{DS(ON)}$ less than 0.2 Ω is probably excessive as switching their gate capacitances is responsible for half the total gate-drive losses.

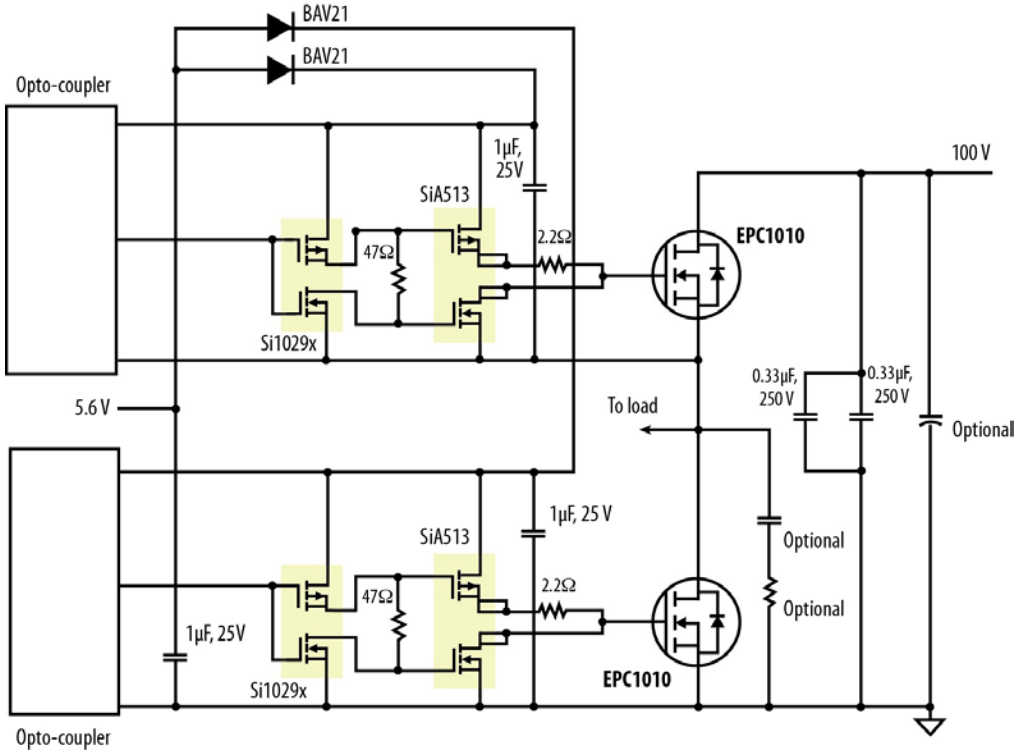


*Figure 9. Schematic of discrete gate-drive circuit.*

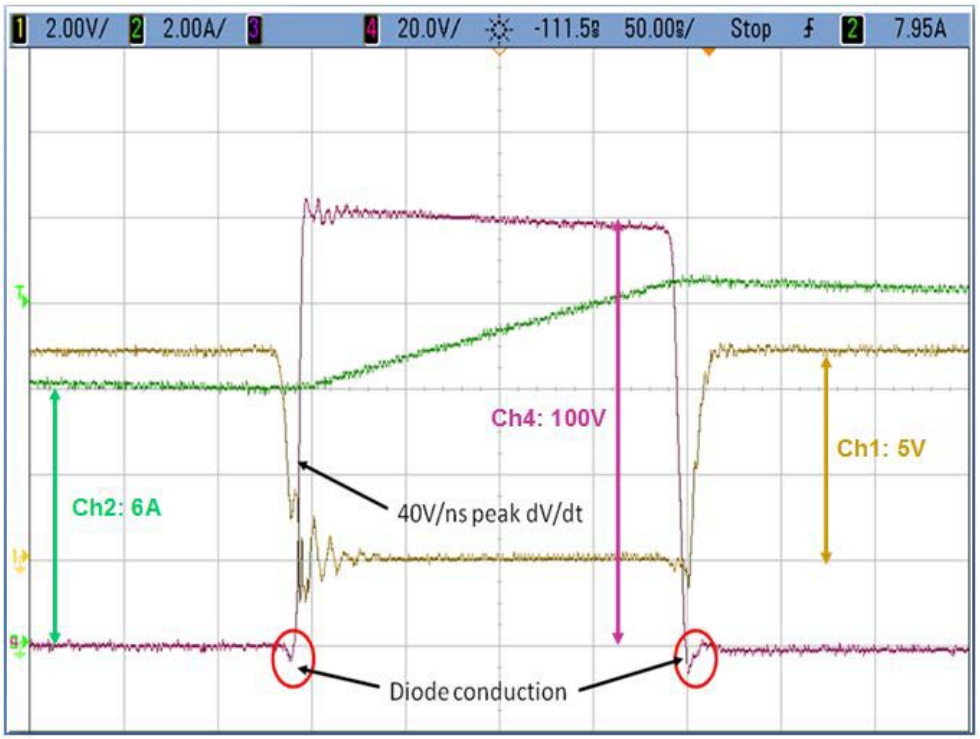


*Figure 10. EPC1010 switching 100 V and 7 A using discrete gate-drive solution. Ch1: low-side G-S voltage (2 V/div), CH2: inductor current (2 A/div), Ch4: low-side D-S (switch-node) voltage (20 V/div). Time scale: 50 ns/div.*

## *Conclusions*

EPC's eGaN transistors give the design engineer a whole new spectrum of performance compared with silicon power MOSFETs. In order to extract full advantage from this new, game-changing technology, designers must understand how to apply the type of simple and cost-effective drive circuitry that has been demonstrated here. Eventually, semiconductor suppliers will develop driver ICs specifically optimized for eGaN technology using specifications like those presented above for the "ideal" drive IC. When such gate-driver chips become commercially available, the task of transitioning from silicon to eGaN technology will become even more simple and cost effective.

### References:

1. http://epc-co.com/epc/Products.aspx

2. B. J. Baliga, Power Semiconductor Devices, 1996, PWS Publishing Company, p. 373

3. http://epc-co.com/epc/documents/datasheets/EPC1001_datasheet_final.pdf

### About The Author

*Johan Strydom is currently the head of Applications Engineering at EPC Corporation. He received his Ph.D from the Rand Afrikaans University, South Africa in 2001. From 1999 to 2002 he was working as a GRA and post-doctoral researcher at the Center for Power Electronics (CPES), Virginia Tech. Prior to joining EPC, he held various application engineering positions at International Rectifier Corporation (IRF) and more recently at Linear Technology Corporation (LLTC), working on a wide range of consumer and industrial applications including motor drives, class-D audio, hybrid power modules and dc-dc converters for VRM and POL.*

For more on GaN power transistors and their applications, see the How2Power Design Guide, select the "Popular Topics" category, and then search the "Silicon Carbide and Gallium Nitride" subcategory.