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Increasing Active-Mode Efficiency And Reducing Standby Power for Energy Star

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As the need to meet green initiatives becomes more pressing, the International Energy Association (IEA) will be mandating that suppliers of electronic equipment reduce the power consumption of their systems below 1 W, 0.5 W or even 0.25 W when operating in the standby mode. To reduce this wasted energy below the desired limits, we need to both improve consumer awareness of the problem and improve the available power supply technologies. This paper focuses on the technology side, discussing the main sources of loss in ac-dc power supplies and techniques for reducing these losses during active and standby modes of operation.

Introduction

When appliances and equipment are switched off or not performing their primary function, the electricity being used is known as standby power. A device can consume around 8600 W of energy for an entire year if it draws 1 W constantly for a year, which corresponds to about $1.00/yr of energy cost. Although this wasted standby power seems very small, when we sum all such devices that are continuously plugged in within the household, the number becomes significant—at around $3 billion in annual energy costs for U.S. households or approximately 7% of total residential electricity consumption in America.

For example, in typical set-top boxes (STBs) shown in the figure below, we can see, there are subcircuits within a complete system. The ac line is used as the input to the ac-dc adaptor, which outputs a dc voltage to power the STB indicated in the red box. The STB also consists of a dc-dc power section, which converts the dc voltage out of the ac-dc supply to a number of lower voltages for powering the digital processor and interfacing with different peripherals.

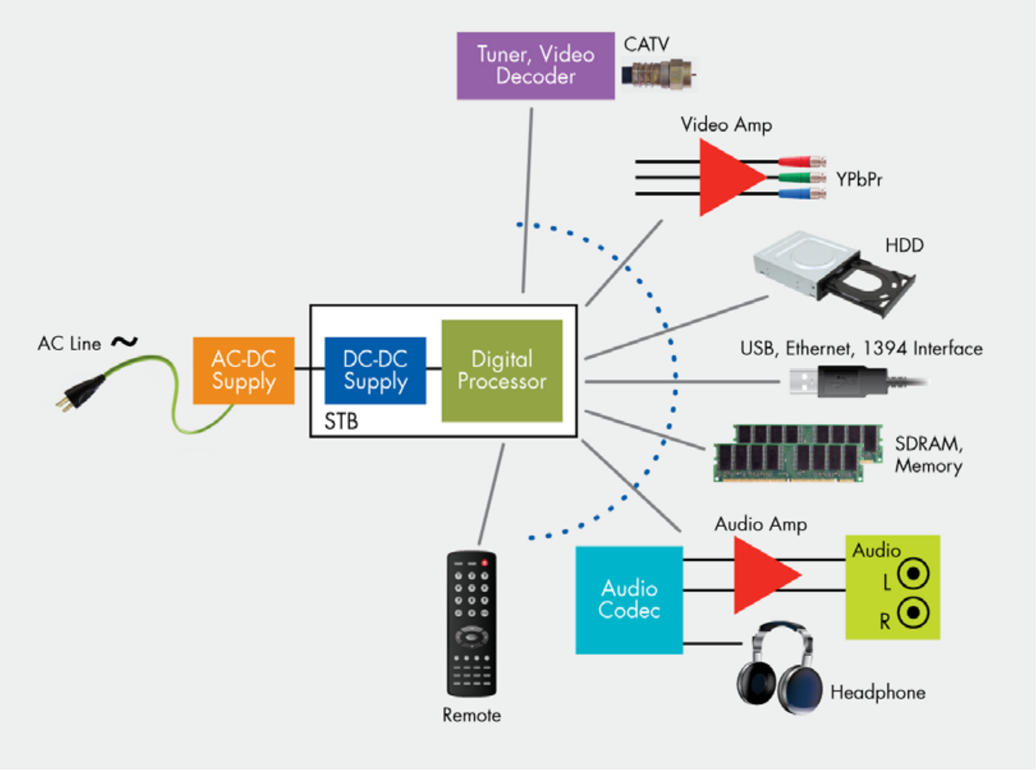

Figure 1. Typical block diagram for a set-top box (STB)

Set-Top Box System

The set-top box system consists of a number of different subcircuits, each of which could be turned off during standby mode to reduce the system's overall power consumption. To obtain the Energy Star certification, the ac-dc adaptor needs to have at least the minimum specified efficiency at full load and to have less than 500 mW of power dissipation under no-load conditions. Energy Star requirements for set-top boxes are given in Tables 1 and 2.

Table 1. Energy Star requirements for set-top boxes: minimum average efficiency in the **active mode.**

Nameplate Output Power (P_{NO})	**Minimum average efficiency in active mode (expressed as a decimal)**
0 to <1 W	$\geq 0.5 \times P_{NO}$
1 to 51 W (24 W)	$\geq [0.09 \times \ln(P_{NO})] + 0.5$*
>51 W	≥ 0.85

*For a 24-W power supply, the required efficiency would be 78%.

Table 2. Energy Star requirements for set-top boxes: proposed energy-efficiency criteria for **no load**.

Nameplate Output Power (P_{NO})	**Minimum power in no-Load**
0 to <15 W	≤0.3 W
15 to <50 W	≤0.5 W
50 to <75 W	≤0.75 W
75 to <180	≤1.0 W

For the STB to obtain an Energy Star certificate it needs to have less than or equal to 1 W of power dissipation in the sleep mode.

The goal is to increase the efficiency in the active mode and reduce the power dissipation in standby mode by doing the following:

- Focus on improvements at the architectural level to sense when a system is in a low-power state and take steps to improve the efficiency.
- Improve the component-level optimization to minimize losses.

Let's start with the ac-dc section followed by the dc-dc and digital processor sections. The table below is an example of loss calculation for a typical flyback design with universal input and 32-V output with a total of 20-W output power. Table 3 below indicates where we need to focus our attention to bring down the losses.

Table 3. Loss calculation for a typical flyback converter design.

Source of Loss	**Power Loss (W)**	**Percentage of total converter loss (%)**
MOSFET (switching loss)	0.64	16
MOSFET (conduction loss)	0.253	6
Output diode	0.98	25
Controller	0.053	1
Sense resistor	0.055	1

Transformer (core loss)	0.212	5
Transformer (copper loss)	0.329	8
Startup resistor	0.054	1
Snubber and miscellaneous	1.4	35
Total	3.976	
Efficiency= P_{OUT} /(P_{OUT} +Total Power Loss), P_{OUT} = 20 W	83.4%	

Transformer Losses

Looking at Table 3 above, one can easily ignore the transformer losses and concentrate on snubber, diode and MOSFETs as the main culprits for high overall losses. Although all those losses are critically important, the snubber loss is caused by a loose coupling between the primary and secondary winding of the transformer. So, to improve the snubber loss we really need to start at the transformer design.

The mutual coupling can be improved by using a better winding-layer arrangement, which increases coupling between the primary and secondary side and, in effect, reduces the leakage energy that would otherwise be dissipated in the snubber circuit.

Magnetic components are the major contributor to the overall power supply losses. Lower loss material for both full pulse width modulation (PWM) and pulse frequency modulation (PFM) modes (in the latter, the frequency is much lower), plus a proper winding arrangement can lower both core and ac losses and increase power supply efficiency.

In any flyback-based, ac-dc adaptor design, the high value of V_{IN} forces the designer to operate at a lower switching frequency to obtain lower switching losses. This imposes a high volt-use on the transformer, necessitating a large number of turns on the transformer primary to keep the flux density at an acceptable level below its saturation point.

In the no-load condition, another source of excessive loss is the transformer magnetizing current. In addition to the current flowing in the primary because of the output load (I_S/n), there is also a magnetizing or exciting current (I_{MAG}) that flows in the primary whether the load is connected or not. The magnetizing current causes a copper loss under light-load or even no-load conditions (Figure 2.)

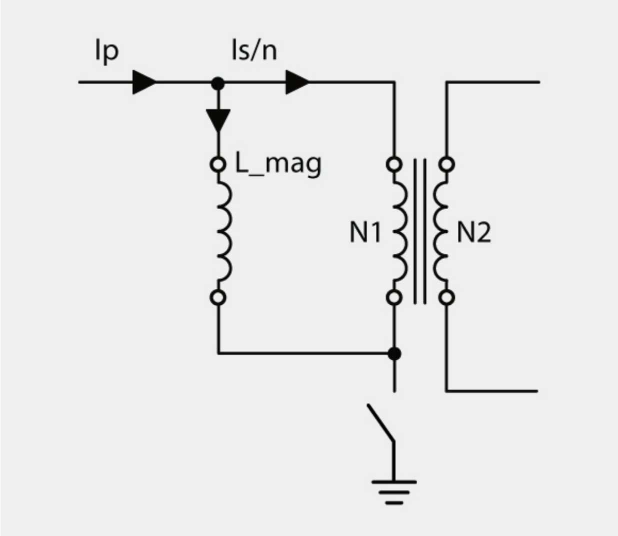

Figure 2. Transformer leakage and winding model.

MOSFET Losses And Packaging

Typically, higher-performance converter designs push the MOSFET's silicon and packaging technologies for smaller and more-efficient products. Low $R_{DS(ON)}$ is a crucial factor in minimizing MOSFET conduction losses at full load. Since the package bond wire and lead resistance can be a considerable portion of the total resistance, MOSFET suppliers are paying special attention to minimizing package resistance in newer packages.

Compared to other package types, a superior thermal performance in a smaller package footprint with optimized electrical performance can be obtained by using enhanced packages like Fairchild's Power 56 and 33 with exposed copper lead-frame technology and aluminum round-wire interconnection (Figure 3.)

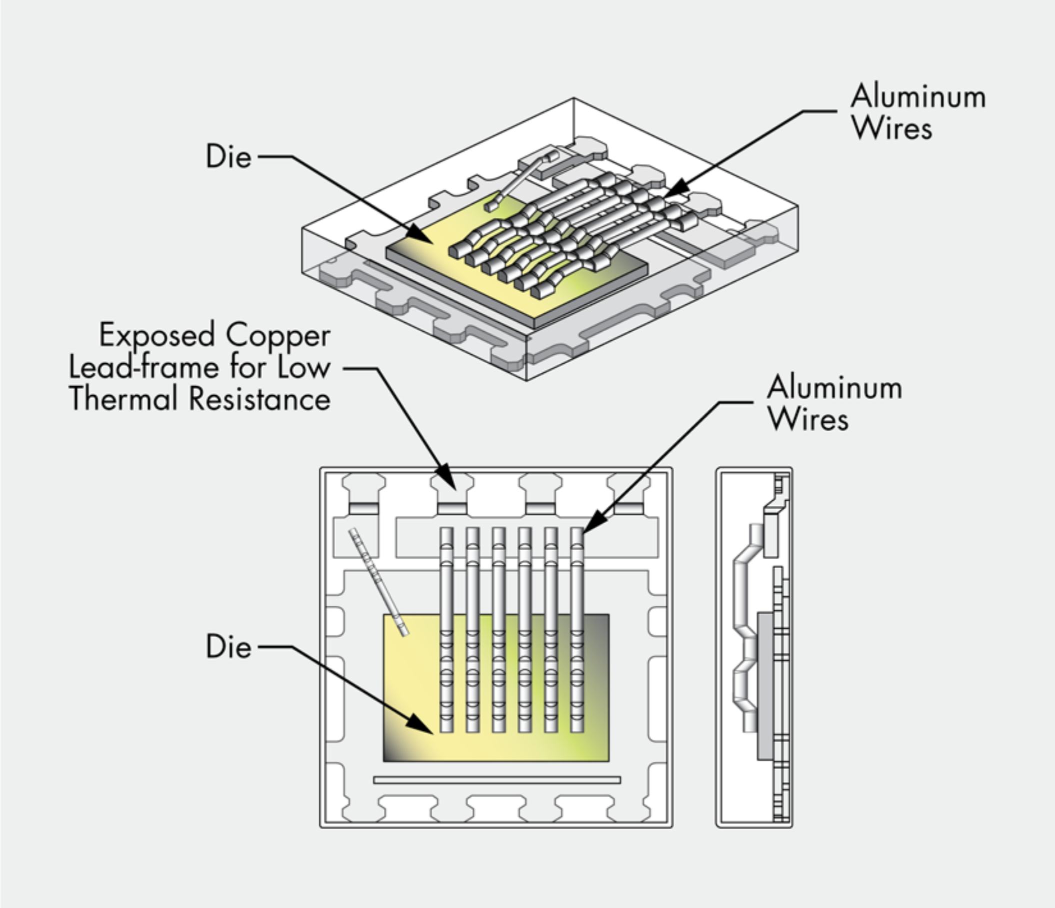

Figure 3. Power 33 and 56 packaging.

The advances in both silicon and packaging technology like the dual cool power 33 package allow superior thermal performance with extremely low on-resistances of less than 2 mΩ at currents as high as 20 A with a 3.3-mm x3.3-mm footprint (Figure 4).

Figure 4. Advanced packages such as the Power 33 allow heat to be extracted from the top and bottom sides of the package.

When evaluating MOSFETs, low $R_{DS(ON)}$ is required for better efficiency at full load. However, it is also very important to look for low a figure of merit (FOM, which is $R_{DS(ON)}$ x Q_G total) to minimize losses at light load. At light load, the $R_{DS(ON)}$ is not as critical, and most of the loss is caused by the gate-drive losses, which are a function of the applied gate voltage (V_{GS}) squared.

It is also essential to optimize the gate voltage to the MOSFET, because as the gate voltage increases, the on-resistance of the MOSFET decreases. However, as the gate voltage increases, the required gate charge Q_G also increases. Gate-drive power $P=Q_G \times V_{GS} \times F$ where Q_G is the gate charge, V_{GS} is the gate voltage, and F is the frequency.

Output-Diode Losses

Conduction loss for a standard schottky conducting 2 A at 500 mV is about 1 W. With 200-mV improvement in forward voltage drop (V_F) the loss could go to 2 A at 300 mv or 600 mW, saving 400 mW of power dissipation. Replacing schottky diodes with synchronous MOSFETs with 10 mΩ of $R_{DS(ON)}$ for higher-current, low-voltage applications is also another option.

Controlling Operating Frequency

There are also different techniques for reducing the controller's switching frequency, which can be applied to reduce power-semiconductor switching losses at standby power. One of these techniques is to lower the frequency of the power supply, causing a reduction in switching losses and improving efficiency in low-power operation.

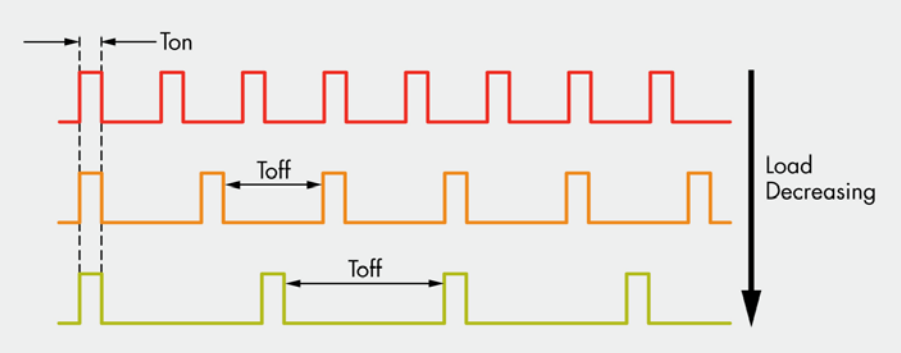

Figure 5. Pulse frequency modulation.

Switch-mode power supplies have two modes of operation: PWM and PFM. In the PWM mode, the switching frequency is fixed. Varying the duty cycle of the power supply regulates the output voltage.

In the PFM mode, the switching frequency varies as the line and load conditions vary, regulating the output voltage. With PFM mode, the switching frequency is proportional to the output power. At low output powers, the switching frequency is reduced, which lowers switching losses and increases the efficiency. The quiescent current consumption of a PFM controller is limited only to the current needed to bias its reference and error comparator. However, PWM controllers always have an active oscillator that continually draws current from the input source even when there is no load.

Many PWM suppliers turn off most or a portion of the PWM functionality to lower the losses during very light load or no-load conditions. With this approach, a few cycles of delay are added before and after the burst mode, which leads to an audible noise problem.

This delay also causes a dip in output voltage when the supply turns back on and goes from light load to full load. To prevent the voltage dip, power supply designers use additional output capacitance in parallel, increasing the cost and size of their systems.

Advanced burst mode minimizes the switching loss under light load with the drawback of increasing the dc output ripple during this mode of operation. Advanced burst mode can be implemented in conjunction with hysteretic control to achieve lower overall losses during light load-operation (Figure 6). When an output voltage is measured at the power supply controller’s feedback pin, and it is below a threshold level, all high-power circuitry within the chip will be turned off to save power loss at light load.

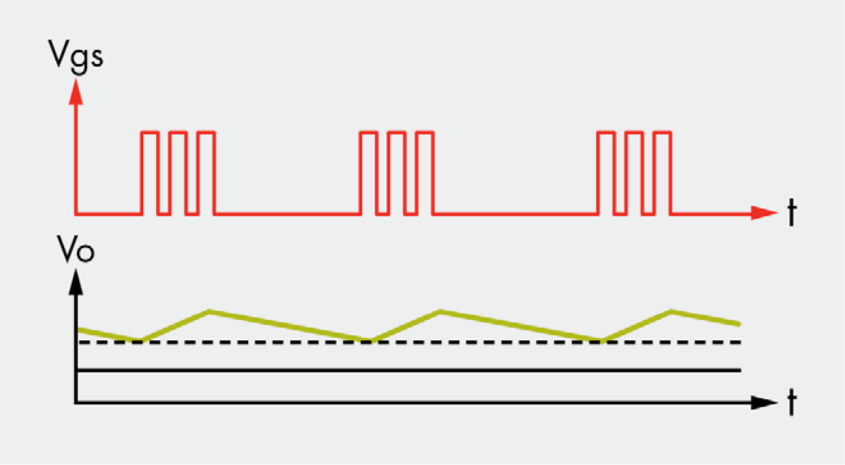

Figure 6. Hysteretic control.

Start-up Resistor Losses

Advances in high-voltage semiconductor IC processes let power-supply ICs start directly from the rectified ac bulk voltage, eliminating the power dissipated in the startup resistors normally used to attenuate the high-voltage bulk to the low-voltage.

In Figure 7, the high-voltage internal current source (I_{CS}) supplies the internal bias and charges the C_{VCC} capacitor and when the V_{CC} reaches a threshold, the internal current source is disabled and the current to bias the PWM comes from the regulated aux winding (Aux Wndg). In this system, both the disconnect of the internal current source (Ics) and low quiescent current are key factors in minimizing start-up losses.

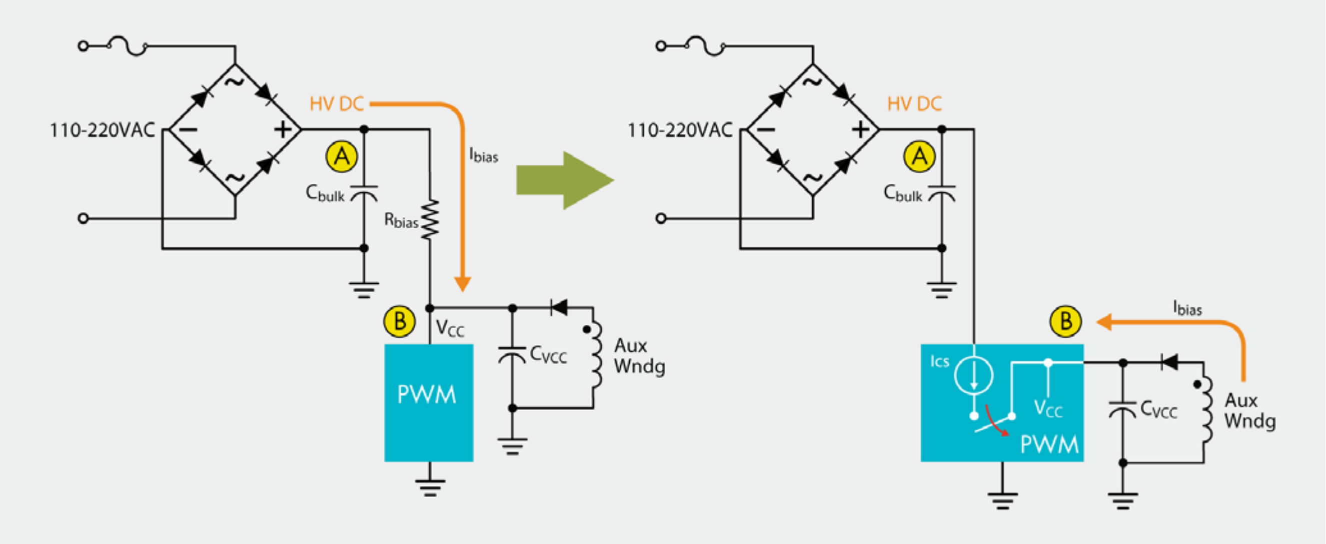

Figure 7.Biasing V_{CC} through R_{BIAS} or with high-voltage IC.

DC-DC Power Section

In the previous section, we discussed PWM, PFM and burst modes. Although, these operating modes also apply when discussing dc-dc converters, in this section we'll move on to the issues of design and component optimization. Besides the usual conduction and switching losses for MOSFETs, there are some other losses that designers might overlook. We will discuss some of these losses and ways to improve efficiency both at full and light load.

Top And Bottom Synchronous MOSFETs

When the duty cycle of the synchronous buck is around 50%, the same devices may be used for the upper and lower MOSFETs. But at lower duty cycles, the choice of each MOSFET should reflect their varying operating conditions. At low duty cycles, the upper FET needs to turn on and off very fast, so a MOSFET with very small gate charge should be selected.

For the lower MOSFET, since it conducts for a much longer portion of the switching cycle, it carries a much higher RMS current. Therefore, the I^2xR losses dominate and the $R_{DS(ON)}$ is a more important factor. Instead of using the same device for both lower and upper MOSFETs, better efficiency can be obtained by selecting a low-gate-charge device for the upper FET (Q1) and low-$R_{DS(ON)}$-device for the lower FET (Q2).

Shoot Thru Losses

When the drain-source voltage of a MOSFET rises quickly, it causes dv/dt-induced turn-on of the MOSFET. This can be a problem for input voltages of 12 V or greater and as the drain-to-source voltage of the MOSFET rises sharply, a dv/dt-induced voltage spike can appear on the corresponding gate signal via the gate-drain capacitance (C_{GD}, Miller Capacitance).

If the dv/dt-induced voltage spike were to exceed the given threshold voltage, the MOSFET may briefly turn on when it should be off and cause a negative impact on overall efficiency. Make sure the chosen controller is using either “fixed dead time” or “adaptive gate drive” or a combination of both techniques.

Deadtime Loss

When a synchronous rectifier turns off, there will be deadtime to make sure that the upper FET waits for the bottom FET to turn off, to avoid cross conduction. During this deadtime the internal body diode of the bottom MOSFET conducts. Because of the body diode’s slow reverse-recovery time, it needs a finite time to turn off, which causes additional power loss during this time.

Using MOSFETs with an integrated schottky diode rather than a regular body diode can help. Since the schottky has zero or very little reverse-recovery time, it reduces the body-diode loss during deadtime.

Parasitic Losses

Parasitic inductance arising from both component packaging and circuit layout is a reality of any circuit. Going to a higher switching frequency can reduce the size of our units and minimize the effect of capacitive and inductance parasitics. Increasing the switching frequency allows a reduction in size of the total power system with smaller components, greater degree of integration and more control over parasitics (Figure 8).

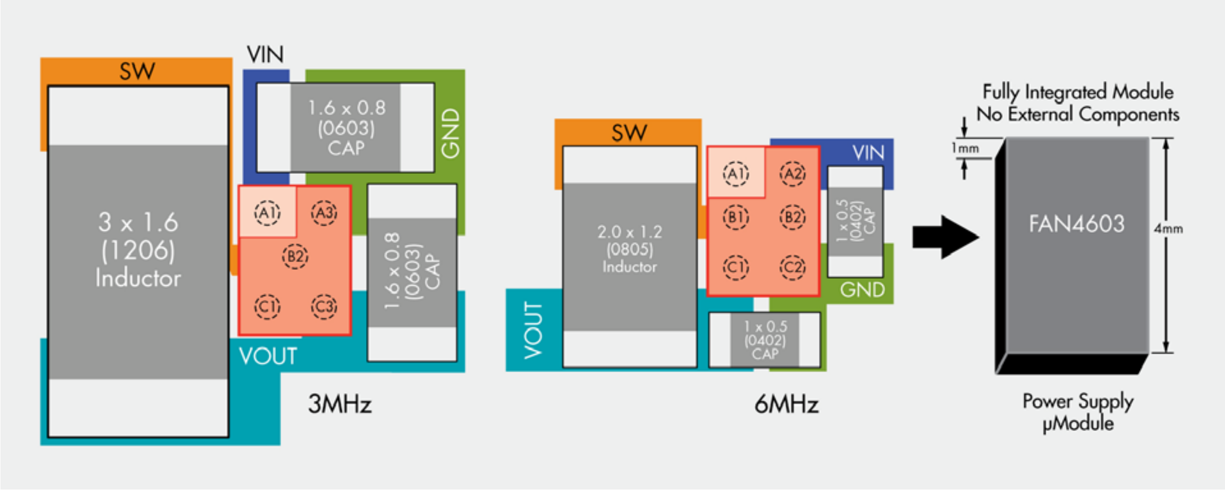

Figure 8. Going to higher switching frequencies reduces component size as well as parasitic inductance and capacitance.

Multiple Load Switches

One solution for reducing standby current involves use of load switches to shut down power to unused subcircuits or functional blocks in the system. Circuitry in the system can be divided into a number of islands or subcircuits, each incorporating a load switch. Using an enable pin or I^2C control, load switches can turn the power off to subcircuits when they in standby mode.

In standby mode, power only needs to be maintained for the subcircuit that is holding the information needed for recovery to the operating state. An example is shown in Figure 9 where subcircuit #1 is kept live, while the other subcircuits may be turned off to save power.

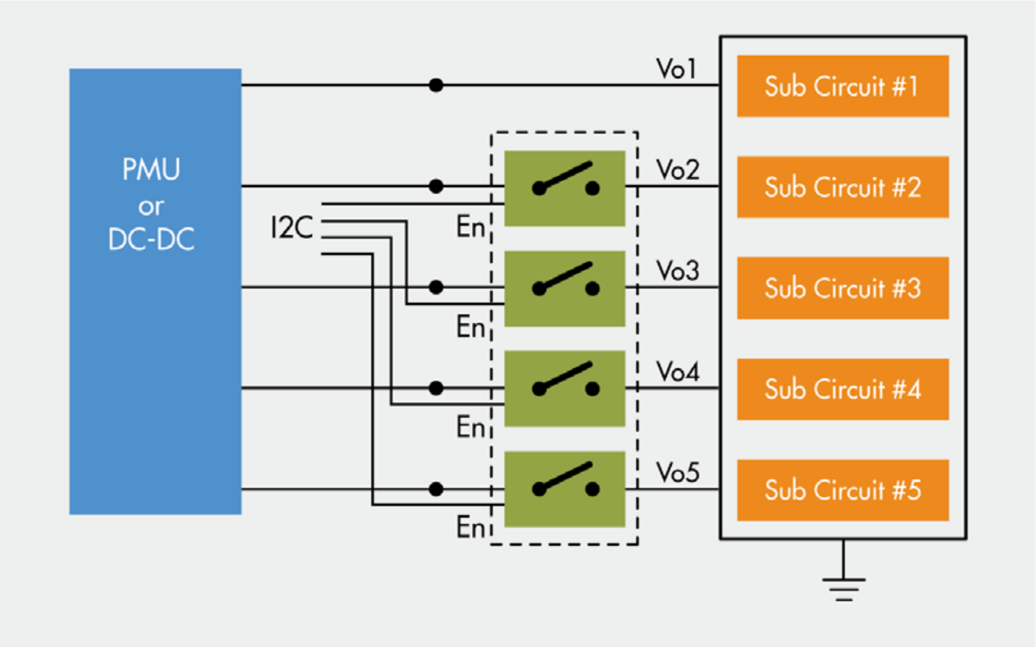

Figure 9. Load switches to turn off subcircuits.

Although with this approach, the standby current is greater than when the power to all subcircuits is cut, keeping one subcircuit live makes it possible to implement a standby mode that allows a quick recovery. However, this approach could introduce an engineering challenge in making sure the functional blocks are turned on and off with the proper timing.

We can put the system in standby mode, by turning on or off different load switches connected to different functional blocks. Once a command is entered from GPIO or I^2C, the low-power DSP exits from standby mode, decodes the signal received and switches on the whole system through the load switches.

Digital Processor

Processor chips are using low–power technologies to reduce power consumption during both active and standby modes. Clock gating is one technique that can be used to reduce the active power dissipation in a system by turning on the clocks (not the power) to specific logic blocks only when there are tasks pending. When there are no pending tasks, the clock to a specific logic block can be turned off, reducing the active power for that block only. But a better alternative to clock gating would be to turn off power to those logic blocks that are not being used.

Since the processor's active-mode power consumption is a function of both supply voltage and frequency (Freq x V^2), we have two parameters we can vary to save power. We can dynamically control the processor's supply voltage (a technique known as dynamic voltage scaling) or modulate its clock frequency as a function of the intensity of the computing task (Figure 10.) When less performance is required, the system can lower both the frequency and the supply voltage of the device.

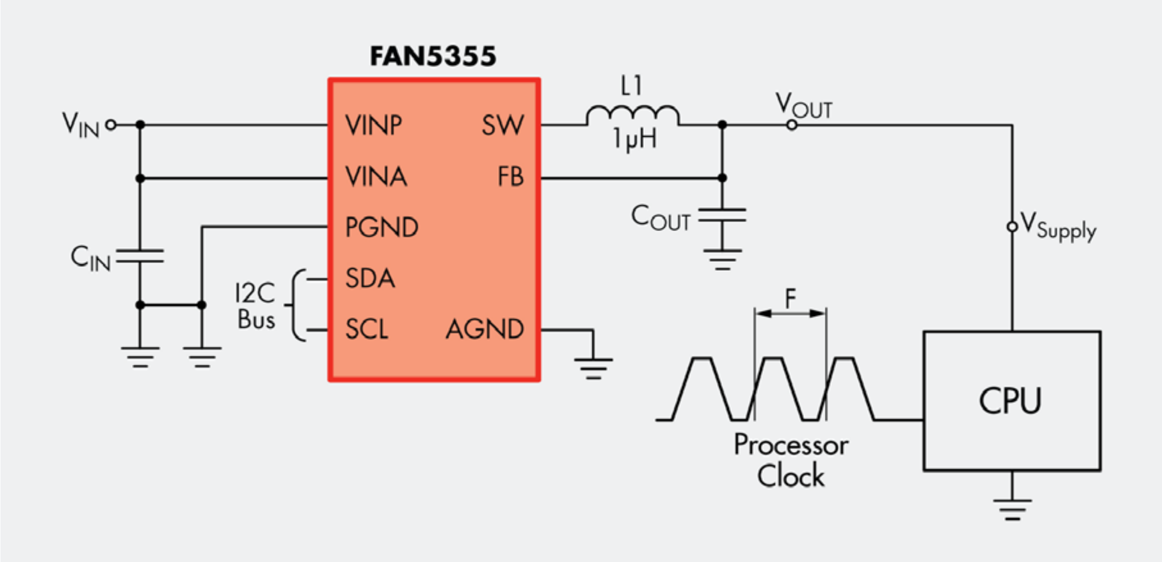

Figure 10. Dynamic voltage scaling of V_{OUT} using I^2C control of the dc-dc converter (FAN5355).

Conclusion

The traditional approach of increasing a system's efficiency only at full load needs to be tuned to accommodate an increase in efficiency under both full- and light-load conditions. System engineers need to focus on improving both architectural-level and component-level optimization of their systems to come up with the most efficient designs and lowest power losses.

With regard to the power supply, special attention needs to be focused on designing transformers with low magnetizing current to boost efficiency by reducing copper losses at light load. A top-level system review is also needed to find out where all the losses within a given system are, and use controllers with PFM or burst mode capabilities to reduce the losses at light loads.

Creating power islands, using load switches to power subcircuits on/off as needed, can also save power consumption during standby modes.

About the Author

Majid Dadafshar is currently working for Fairchild Semiconductor as a field application engineer. He has over 25 years of design engineering experience in power electronics, both in commercial and military applications. He received his engineering degree in 1984 from Northern Arizona University majoring in electronics. He has been employed by ITT Power systems, ITT courier, ITT Aerospace/Defense, Sony Electronics, Eastman Kodak, and Pulse Engineering. He holds four patents and has published a number of technical papers in power supply design, magnetics, EMI, loop stability and conducted numerous domestic and international electronic technical meetings in different symposiums.

For more on increasing efficiency in dc-dc converters, see the How2Power Design Guide, select the "Power Supply Function" category, and then search the "DC-DC Converters" subcategory.