ISSUE: July 2010

How to Control Phase Voltage Ringing in Synchronous Buck Convertors

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Integrated synchronous buck converters are used to meet ever increasing demands for higher power, to increase efficiency and to reduce the size of dc-dc converters. They combine a PWM controller, switching MOSFETs and their drivers within the same package. In order to reduce the overall size of the dc-dc converter, a high operating frequency is required. At the same time, it's necessary that the control FET and the synchronous FET in the buck converter be turned on and off with very fast rise and fall times. Doing this improves converter efficiency and reduces power dissipation.

This fast switching of the MOSFETs can cause higher voltage spikes and ringing at the phase node. These effects are undesirable because they can cause increased power dissipation, higher voltage stress on the switching devices, higher EMI, and higher peak-to-peak output ripple and noise at higher bandwidth.

In this article, the IR3842 integrated buck converter is used to study the undesired voltage spike and ringing at the phase node caused by fast switching. The focus here is mainly on the peak-to-peak output ripple voltage that occurs at higher bandwidth. Experiments are conducted to gauge the impact of different methods used to control this ringing, and the pros and cons of these methods are discussed.

The Test Circuit

By co-packaging a PWM controller, MOSFET switches and drivers, integrated synchronous buck converters can reduce PCB parasitic inductance and capacitance to minimum. With a strong driver, the rise and fall times of the phase voltage can be 10 ns max. and typically, rise and fall times of 5 ns or less can be achieved, which reduces switching losses to a bare minimum.

However, this fast switching action produces voltage spikes and ringing at the phase node of the buck converter. In addition, the fast turn on of the control FET can cause premature turn on of the synchronous MOSFET, though we will not discuss that effect here.

The ringing phenomena at the phase node can produce higher output ripple voltage at higher bandwidth as switching noise gets coupled to the output. If a measurement is performed at a 20-MHz bandwidth, the switching noise coupled to the output cannot be seen very clearly because spikes have high-frequency content that extends well into the megahertz region. But at a higher bandwidth, say 200 MHz or greater, this switching noise gets coupled to the output and increases the peak-to-peak output ripple voltage and noise. This can pose a problem for some applications requiring very low output ripple and noise at full bandwidth.

Fig. 1. shows schematic of a synchronous buck converter based on International Rectifier's IR3842W SupIR Buck IC. This is a synchronous buck converter operating with 12-V input and producing 2.5-V output while switching at 600 kHz. Through careful layout of the PCB, the parasitic inductance and capacitance in the power section can be reduced to a minimum, which helps to prevent the ringing. But even with a very good PCB layout, there can still be some ringing at the phase node.

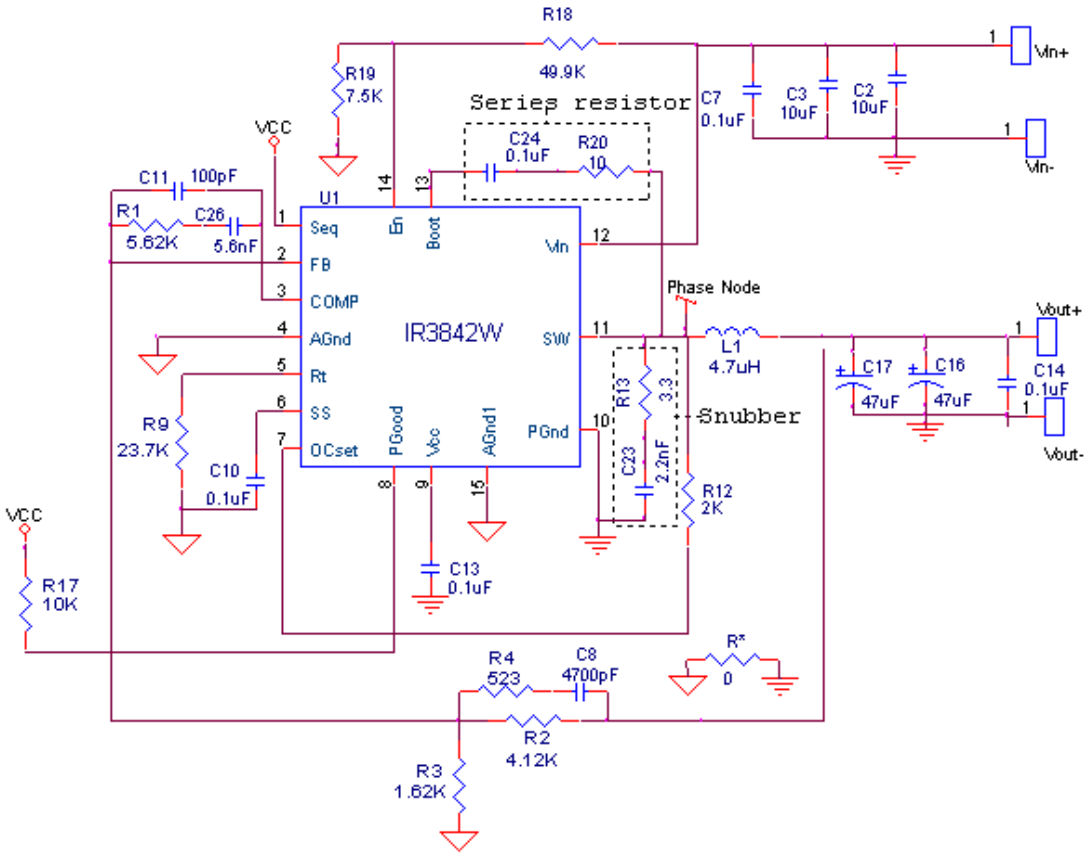
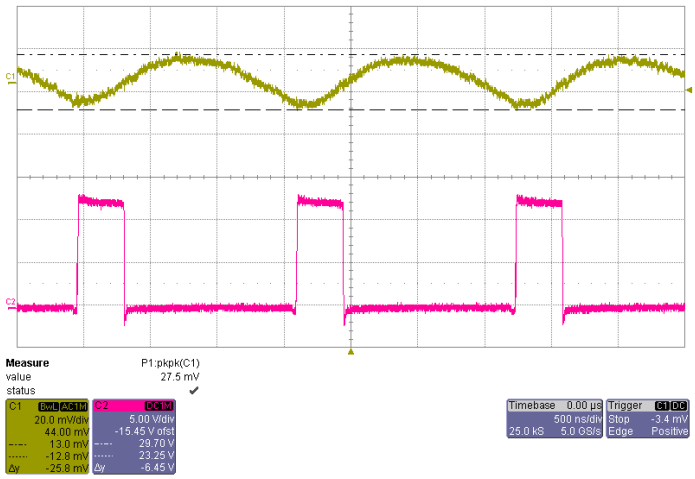


Fig. 1. This synchronous buck converter generates a 2.5-V output from a 12-V input, while operating a 600-kHz switching frequency. Care must be exercised in the layout of the PCB to minimize ringing at the phase node.

To study the behavior of the phase node ringing and its impact on output ripple voltage, and also to evaluate possible solutions, we'll conduct some experiments on the IRDC3842 demo board. We'll measure and capture the waveforms for the converter's phase voltage and output ripple voltage with the converter's original design (i.e. with no added components to suppress phase-node ringing). Then we'll repeat these measurements with two possible solutions. In one case, a resistor (R20) will be placed in series with the bootstrap capacitor (C24). In the other case, an R-C snubber (R13 and C23) will be installed from the phase node to ground.

Test Results

Measurements of the converter's output ripple voltage and phase voltage were taken at a limited bandwidth of 20 MHz and at a full bandwidth of 500 MHz bandwidth. The results of these measurements are shown in Figs. 2 and 3 respectively. In the full bandwidth measurements, the scope is set to its full bandwidth of 600 MHz. However, the scope probe has a bandwidth of 500 MHz, which limits the measurement bandwidth to 500 MHz.



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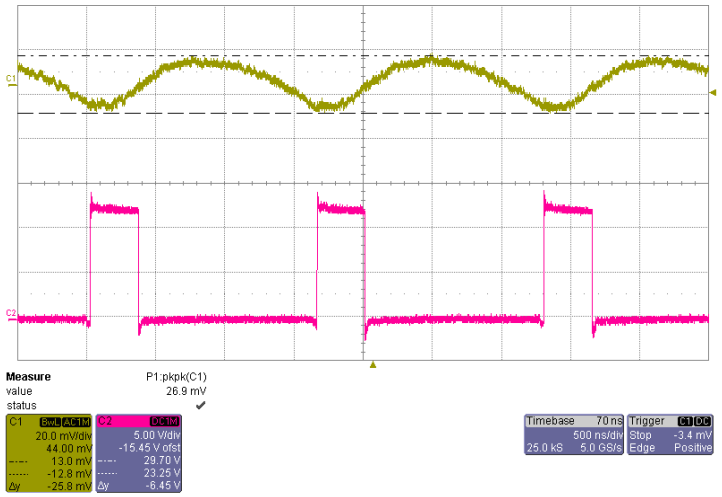

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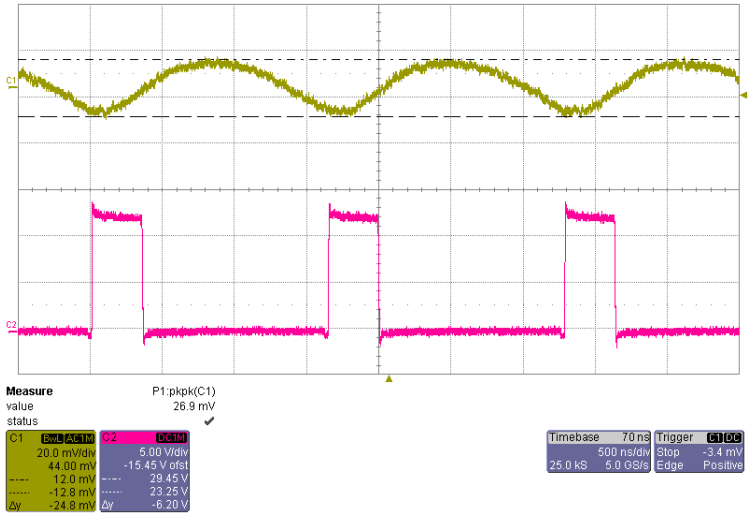

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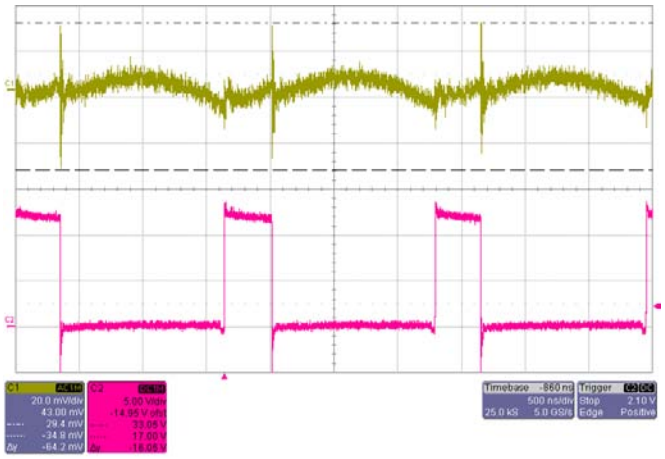
Fig. 2. The buck converter's peak-peak output ripple voltage (Ch 1, green trace) and phase voltage (Ch 2, pink trace) measured at **a 20-MHz bandwidth** with a time scale of 500 ns per division. The ripple voltage is 27.5 mV for the original design (a), 26.9 mV with a 10-Ω resistor in series with the bootstrap capacitor (b), and 26.9 mV with an R-C (3.3 Ω + 2.2 nF) snubber (c). In each case, the value of the bootstrap capacitor is 0.1 µF.



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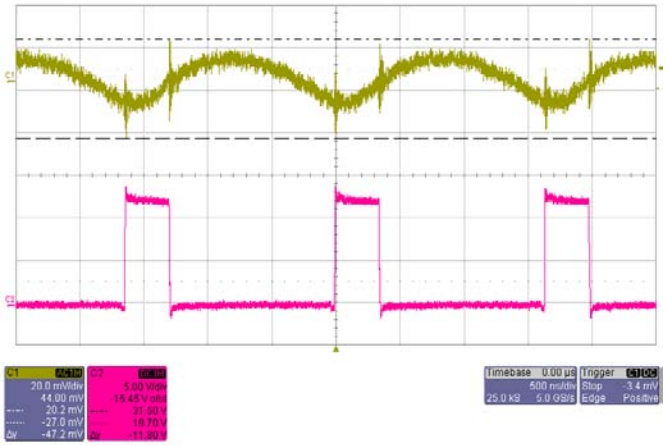

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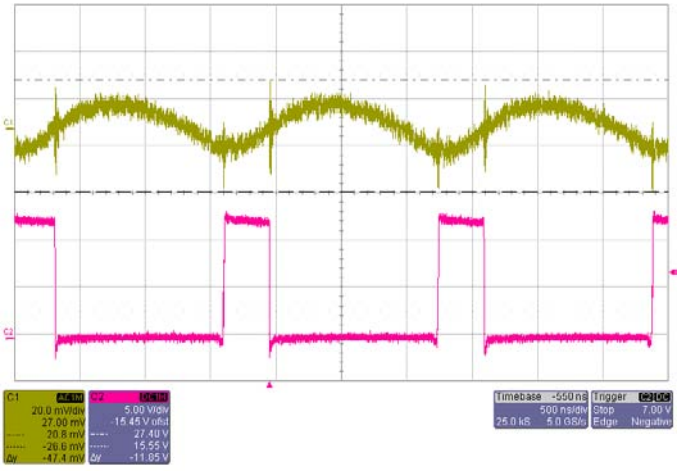

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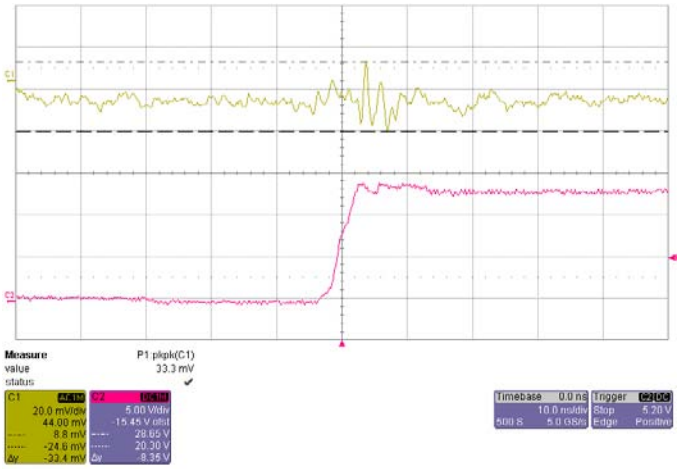
Fig. 3. The buck converter's peak-peak output ripple voltage (Ch 1, green trace) and phase voltage (Ch 2, pink trace) measured at **a 500-MHz bandwidth** with a time scale of 500 ns per division. The ripple voltage is 64.2 mV for the original design (a), 47.2 mV with a 10-Ω resistor in series with the bootstrap capacitor (b), and 47.4 mV with an R-C (3.3 Ω + 2.2 nF) snubber (c). In each case, the value of the bootstrap capacitor is 0.1 µF.

It is found that adding a resistor in series with bootstrap capacitor offers the greatest reduction in peak phase voltage as well as ringing, while having minimum impact on efficiency. Adding a snubber to the converter also produces a similar effect, but results in a higher power loss.

When measurements are conducted with a 20-MHz bandwidth, the peak-to-peak output ripple and noise voltage is found to be the same in all three cases (see Fig. 2, again.). However, when measurements are taken at the full bandwidth, the output ripple voltage increases and does so by different amounts depending on which method was used to control the peak phase voltage and ringing (see Fig. 3, again).

One of these methods can be used to obtain lower output ripple voltage in sensitive applications where the output ripple voltage at full bandwidth is critical. Usually the specification for output ripple voltage at 20-MHz bandwidth will be 1% to 1.5% of Vout and with 200 MHz bandwidth this should not exceed 50 mV to 100 mV. However, there may be some applications with much more stringent requirements than this.

Switching noise during the rising edge of the phase voltage can be well controlled with a good PCB layout and may not require any snubber or series resistor with the bootstrap capacitor in many applications. So switching noise coupled to the output is minimum during the rising edge (Fig. 4). But during the falling edge of the phase voltage, there can be ringing that will require a snubber or a resistor in series with the bootstrap capacitor to control the ringing (Fig. 5). This ringing during the rising time is coming from the reverse recovery of the body diode of the synchronous MOSFET. Either a snubber or a series resistor can be used to control the ringing; this will be effective during both the falling and rising edges.



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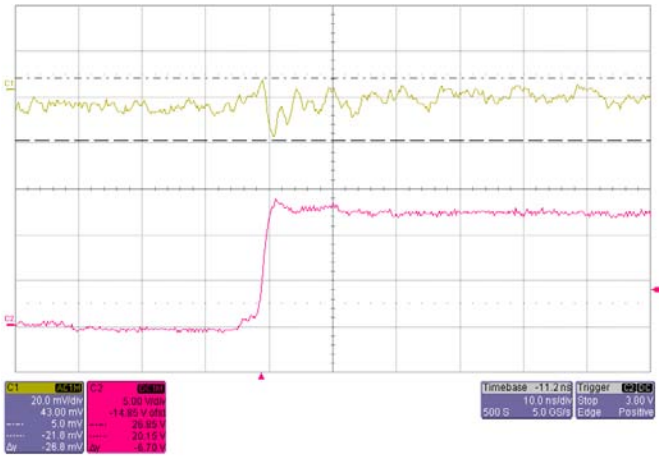

(b)

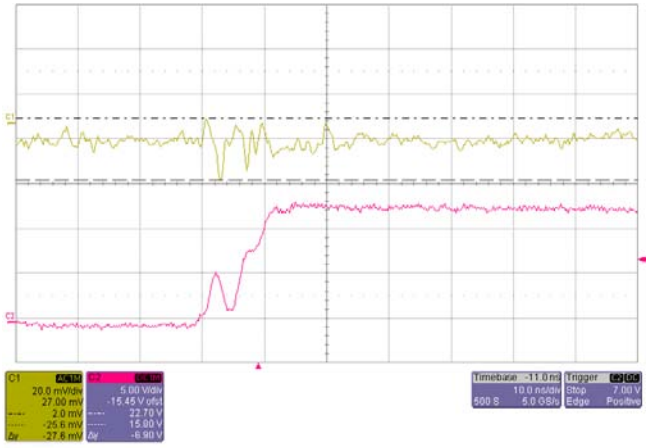

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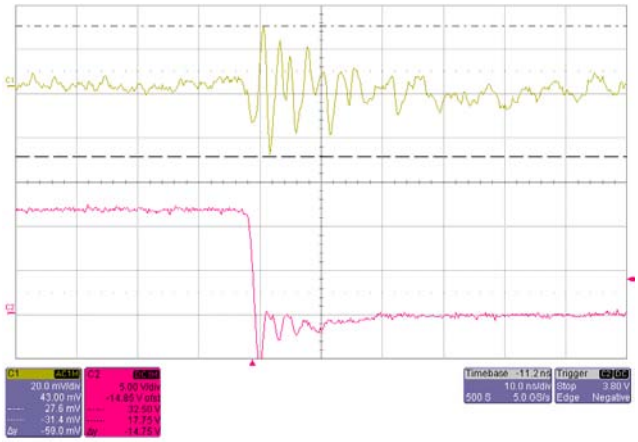
Fig. 4. Switching noise during the rising edge of the phase voltage. The buck converter's peak-peak output ripple voltage (Ch 1, green trace) and phase voltage (Ch 2, pink trace) are measured at a 500-MHz bandwidth with a time scale of 10 ns per division. The ripple voltage is 33.4 mV for the original design (a), 26.8 mV with a 10-Ω resistor in series with the bootstrap capacitor (b), and 27.6 mV with an R-C (3.3 Ω + 2.2 nF) snubber (c). In each case, the value of the bootstrap capacitor is 0.1 µF.



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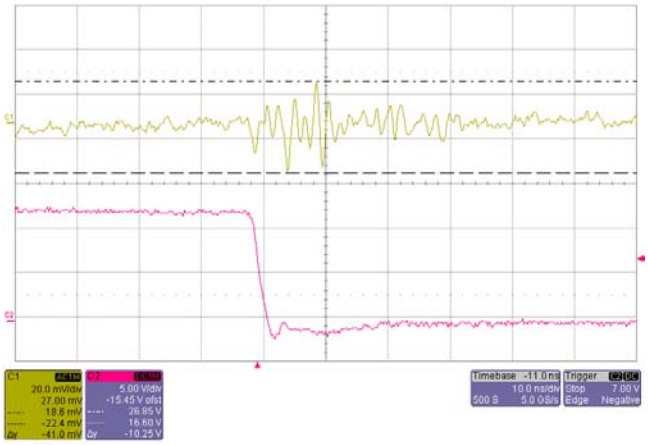

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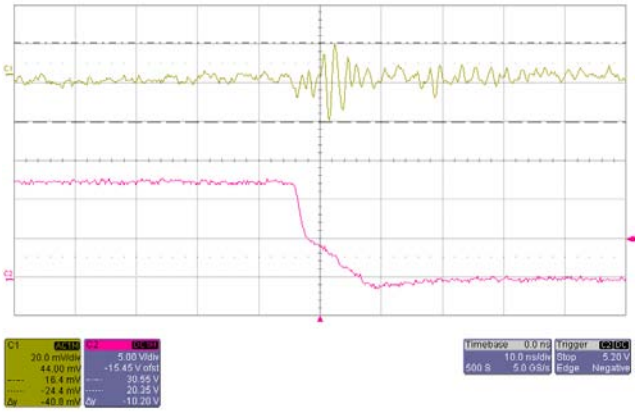

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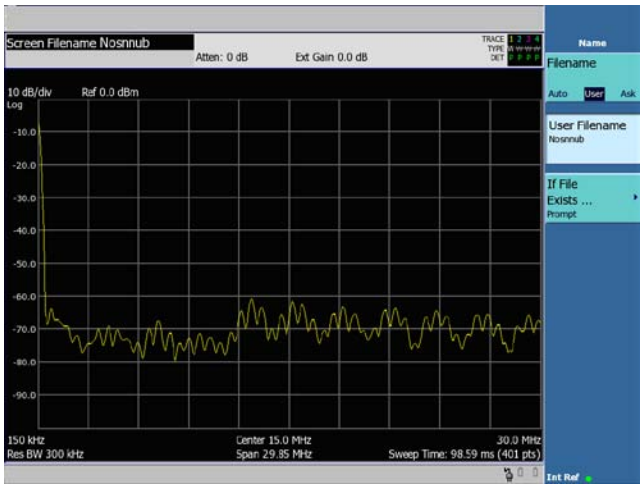
Fig. 5. Switching noise during the falling edge of the phase voltage. The buck converter's peak-peak output ripple voltage (Ch 1, green trace) and phase voltage (Ch 2, pink trace) are measured at a 500-MHz bandwidth with a time scale of 10 ns per division. The ripple voltage is 59.0 mV for the original design (a), 41.0 mV with a 10-Ω resistor in series with the bootstrap capacitor (b), and 40.8 mV with an R-C (3.3 Ω + 2.2 nF) snubber (c). In each case, the value of the bootstrap capacitor is 0.1 µF.

PCB Design Guidelines

Layout is extremely important for high-frequency switching converters. Layout can affect noise pick up and can cause an otherwise good design to perform poorly. Power component connections should be made with wide copper-filled polygons and power planes should be used for power distribution as well as heat dissipation. Input bypass capacitors should be placed close to the IC's input-voltage pins. The inductor and capacitors should be placed as close to the converter IC as possible to reduce EMI radiated by the power traces connecting them as they carry high-frequency switching currents. Loop area should be minimized to reduce parasitic impedance, especially any loop where faster rise and fall of voltage and current is expected.

The feedback and compensation components should be kept away from magnetic components and any other noise sources. In a multilayer PCB, it is preferable to use one power ground plane and another signal ground to connect all control circuit components and connect these two grounds together at a single point. That way the high-current path can be localized so it does not interfere with more-sensitive analog control functions.

Adding a snubber or placing a resistor in series with the boost capacitor can also bring down the EMI noise. EMI noise can be studied with a general-purpose H-field EMI Sniffer probe E101. The probe is placed very close to the IC where EMI noise is maximum and the scan is taken as shown in Fig. 6.



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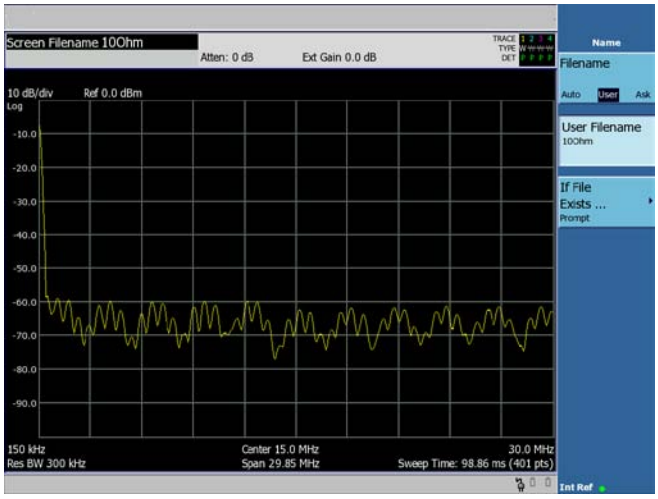

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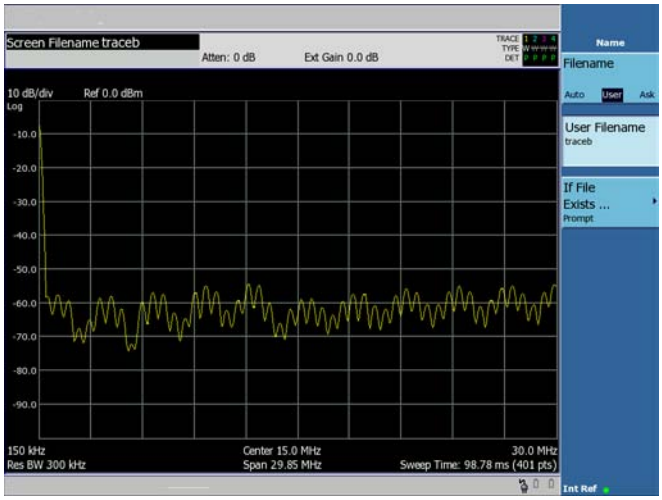

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Fig. 6. An EMI scan of the buck converter is taken with an E101 probe placed close to the IC. Measurements are shown for the original design (a), the modified design with a 10-Ω resistor in series with the bootstrap capacitor (b), and the modified design with an R-C (3.3 Ω + 2.2 nF) snubber installed (c). In each case, the value of the bootstrap capacitor is 0.1 µF.

Selecting Suppression Components

Efficiency is measured in all three cases (Fig. 7.) Adding a resistor in series with the bootstrap capacitor or using a snubber both reduce efficiency. The reduction in efficiency is higher with the snubber. The amount of the efficiency drop depends on the value of series resistor used as well as the snubber component values. Usually the series resistor for the bootstrap capacitor can be below 10 Ω. The recommended value can be somewhere in the 0-Ω to 10-Ω range. A much higher value will cause greater damping, but will also slow down the MOSFET switching speed, cause higher power dissipation, and create a thermal management issue. So using a much higher value resistor is not recommended.

Snubber component design has been discussed previously in many articles. If the ringing frequency is measured without any snubber, then the R-C time constant can be made equal to the time period of the high-frequency oscillation. As a rough starting point for snubber design, R can be chosen as 3.3 Ω. Then, some fine tuning will be required to obtain the desired EMI performance without compromising thermal performance.

Fig. 7. A comparison of buck converter efficiency with 1) the original design, 2) the modified design with a resistor in series with the bootstrap capacitor, and 3) the modified design with an R-C snubber installed.

Having a resistor in series with the bootstrap capacitor reduces the rise and fall times of the control FET. For the same amount of reduction in output ripple voltage this method is preferred over the snubber as the reduction in efficiency is less. A smaller resistor in the snubber reduces ringing, but will have higher power dissipation than the case with the series resistor.

Conclusion

Using either a snubber or a resistor placed in series with a bootstrap capacitor can reduce ringing and peak voltage at the phase node. But the latter approach (the series resistor) is preferred because it results in lower power dissipation. Once the ringing is reduced, peak-to-peak output ripple and noise voltage is also reduced. The value of the series resistor or snubber components will depend upon how much ringing is to be suppressed and the desired peak-to-peak output ripple and noise voltage required at full bandwidth.

About The Author

Suresh Kariyadan joined International Rectifier in June 2009 as senior staff engineer for POL Applications, Enterprise Power Business Unit (EPBU) where he is responsible for all point-of-load customer support for the EPBU. The role involves understanding customer's power supply requirements, providing reference designs, layout of PCBs, design verification tests, troubleshooting customer application boards and evaluating new product performance in application circuits. Prior to joining International Rectifier, Suresh held senior engineering positions with Maxim Integrated Products and Cherokee International. He holds a bachelor degree in Electronics and Telecommunication from Kerala University, India.

For further reading on buck converter design, see the How2Power Design Guide, search the Popular Topics category and select the Buck Converters subcategory.