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Embed Your Planar Magnetics To Maximize DC-DC Converter Performance (Part 1)

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The use of standalone planar magnetics has been in use for some time now. As a result, it is possible to obtain a wide variety of planar magnetic components that cover a wide range of power levels and suit a range of topologies. Many of these discrete planar components are used in embedded dc-dc converter designs, where they take the place of traditional, wire-based transformers and inductors. Compared with these older-style magnetic devices, planar magnetics offer advantages such as low profile, improved efficiency, and easier thermal management.

However, the time is now for many design engineers to contemplate the switch from the discrete planar magnetic devices to embedded magnetics structures. With embedded planar magnetics, the copper windings for inductors or transformers are formed directly on the user's PCB and magnetic cores are then assembled over these windings. This approach enables a higher level of design optimization than the discrete planar approach.

Nevertheless, to create a "real-world" leading-edge embedded magnetics design requires the skills and manufacturing expertise of a company specializing in multi-layer PCB, surface-mount assembly and embedded magnetics design and implementation. Expertise in all these areas makes it possible to develop advanced planar devices such as those combine several magnetic components on the same core (i.e integrated planar magnetics.)

In this article, we demonstrate how embedded planar magnetics can be applied to achieve enhanced performance in a digitally controlled dc-dc converter design. The magnetics design described here was originally developed as part of Microchip Technology's reference design for a dc-dc converter based on the dsPIC33F digital signal controller [1].

For this application, Champs Technologies developed the main transformer (TX1), the output inductor [L2], two gate-drive transformers (DT1 and DT2), and the bias supply flyback transformer (TX3). All of these devices were implemented as embedded planar magnetics with their windings embedded in the same multi-layer PCB. This application also includes a current transformer (TX2), but for this component, a conventional wound device was used. The Fig. 1 block diagram shows the magnetic devices in this application.

Here in part 1 of this multi-part article, we'll describe the procedures used to perform the necessary calculations for designing TX1. In a subsequent Part 2, we'll complete the design of TX1 showing the stackup and layering. And finally in part 3, we'll describe the design of other magnetic components in this application. (Additional background on this application is provided in the Appendix that follows this article.)

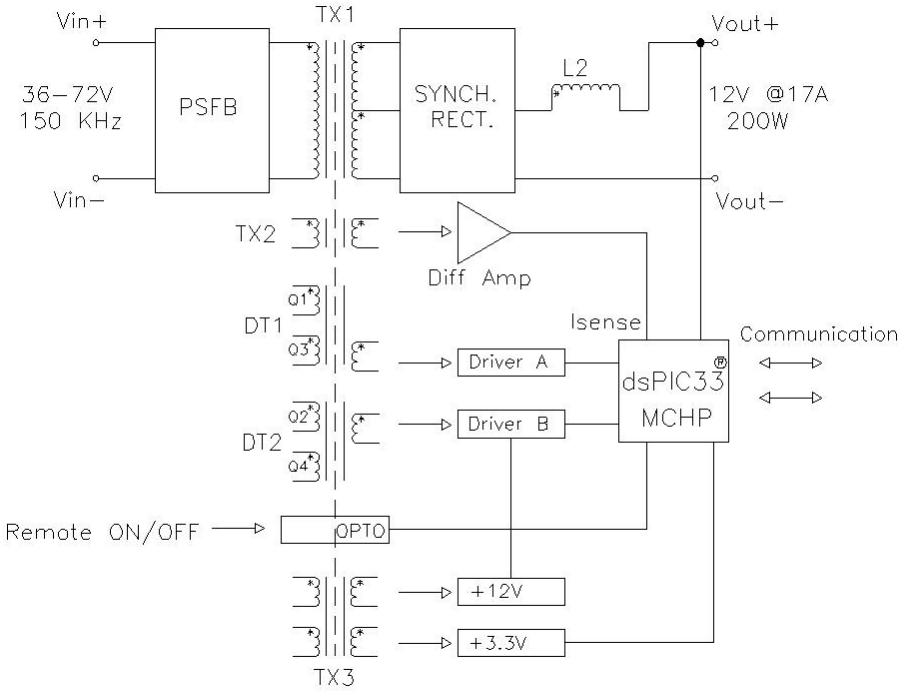


Fig. 1. Embedded planar magnetic devices TX1, L2, DT1, DT2, and TX3 were developed to enhance the performance of this digitally controlled dc-dc converter design. Current transformer TX2 is a traditional, wire-wound device.

Planar Magnetics Design Process

Perhaps not surprisingly, the procedure or method for designing embedded magnetics is the same as in other magnetics designs, namely:

1. Choose optimum core cross section.
2. Choose optimum core window height.
3. Iterate turns vs duty cycle.
4. Iterate core loss.
5. Iterate copper (Cu) loss.
6. Evaluate thermal methods.
7. Estimate temperature rise.
8. Tradeoff cost vs number of PCB layers.
9. Determine mechanical design fit envelope and pad layout.
10. Fit within core window height.
11. Size sufficiently to dissipate power loss and achieve acceptable temperature rise.

Size Sufficiently For Power loss And Thermal Solution

One goal is to offer a broad operating frequency from 125 kHz to 200 kHz in order to give wide latitude for customers to optimize efficiency. The input voltage (V_{in}) range was 36 V to 72 V dc nominal with extended Vin min of 32.5 Vdc. Our analysis of the transformer design thus begins with:

$$V_{in} := 36$$

$$Tp := 6.667 \cdot 10^{-6} \qquad freq := \frac{1}{Tp} \qquad freq = 1.5 \times 10^{5}$$

where T_p is the period.

The intended output voltage (V_o) was meant to supply a typical bus voltage for distributed power applications, namely 12 Vdc. It was also intended that the design span a range of output currents (I_{out}, in amps (A)):

$$I_{out} := 12 \qquad I_{out} := 25 \qquad I_{out} := 33$$

It is soon discovered that if confined to integer turns, one does not have as much flexibility as perhaps originally assumed. One wishes to maximize the duty cycle but the limitation of resolution offered by integer turns will quickly lead to the following turn ratio:

$$N_p := 5 \qquad N_s := 2$$

Magnetics design can be confusing at times but it is intuitively obvious that one needs to use the minimum number of turns practicable. Why? To put it simply, there is a cost or penalty to placing real-world turns on a magnetic structure—namely, resistance, voltage drop, and power loss. So use the least number of integer turns possible.

The duty cycle, D, (over each half-period) is:

$$t_{on} := 2.89 \cdot 10^{-6} \qquad D := \frac{t_{on}}{Tp} \qquad D = 0.434$$

Over a full period, the duty cycle is thus 86.8% at Vin minimum = 36 Vdc.

We use the following regulation voltage drops as assumptions:

$$V_{FET} := .1 \qquad V_{drop} := .2 \qquad V_{fet} := .6$$

This equation confirms the choices:

$$V_o := \left[\left(V_{in} - V_{fet} \right) \cdot \frac{N_s}{N_p} - V_{FET} - V_{drop} \right] \cdot 2 \cdot D \qquad V_o = 12.03$$

We choose a core with the following magnetic parameters:

$$A_c := 0.45 \qquad path\_length := 3.09 \qquad Vol := 1.57$$

where A_C is the core cross sectional area in cm^2, path_length is in cm, and Vol is the core volume in cm^3.

The core shape used in this design example is a tooled core available from Champs Technologies. As an alternative, designers may tool their own cores and in that case any of the core manufacturers can be consulted. In general, a power material in the frequency range of interest should be considered. Material such as 2M, 3H from Nicera or PC95 from TDK or 3C96, 3C95 from Ferroxcube are the most likely and recommended choices.

The peak-to-peak and rms flux densities(B_{pkpk} and B_{rms}, respectively) are:

$$B_{pkpk} := \frac{(V_{in} \cdot t_{on}) \cdot 10^8}{N_p \cdot A_c} \qquad B_{pkpk} = 4.624 \times 10^3$$

$$B_{rms} := \sqrt{\frac{2}{Tp} \cdot \int_0^{t_{on}} \left[\frac{(V_{in} \cdot t_{on}) \cdot 10^8}{2 \cdot N_p \cdot A_c} \right]^2 dT} \qquad B_{rms} = 2.153 \times 10^3$$

where B_{pkpk} and B_{rms} are expressed in Gauss.

To calculate core loss we will use a formula and core constants made available by Ferroxcube. (See Ref 3).

Specifically, for our purposes, using Temp = 50°C and B = Tesla:

$$Temp := 50 \qquad f_1 := \frac{freq}{1000} \qquad B := B_{rms} \cdot 10^{-4} \qquad B = 0.162$$

$$x := 1.72 \qquad y := 2.80 \qquad C_m := 8.27 \cdot 10^{-2}$$

$$C_{t2} := 1.83 \cdot 10^{-4} \qquad C_{t1} := 3.66 \cdot 10^{-2} \qquad C_{t0} := 2.83$$

Using the formula:

$$P := C_m \cdot freq^x \cdot B^y \cdot \left(\frac{C_{t0} - C_{t1} \cdot Temp + C_{t2} \cdot Temp^2}{1000} \right) \qquad P = 1.307 \times 10^3$$

We arrive at a core loss of:

$$Core\_loss := P \cdot Vol \cdot 10^{-3} \qquad Core\_loss = 2.052$$

where core loss is expressed in watts (W).

There is a further method to employ that involves computing the Fourier coefficients of the primary voltage waveform and applying the rms values to compute the core loss. The fundamental and first eight harmonics would produce the following composite waveform:

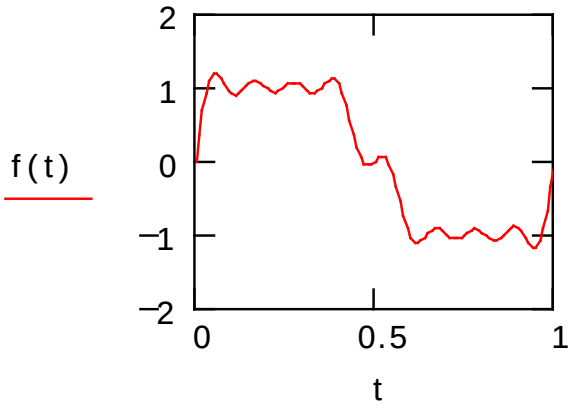


Fig. 2. Fourier components of composite primary voltage waveform.

In the case of duty cycle modulated square-wave forms, it is often the result that the fundamental is the greatest contributor to core loss. That is the case in this instance. In the interest of brevity, a complete derivation is not presented here, but can be obtained by contacting the author.

$PP_{i,0} =$

1.841
$8.667 \cdot 10^{4}$
$9.143 \cdot 10^{3}$
$1.727 \cdot 10^{3}$
$9.39 \cdot 10^{5}$
$1.48 \cdot 10^{3}$
0
$6.429 \cdot 10^{4}$
0

$$\sum PP = 1.855$$

So the value of 2.05 W or 1.86 W of core loss may be used to assess overall efficiency goals and thermal design.

This core loss is conservative by design as its intended use as a reference design is not to employ any particular attempt to lower thermal resistance to ambient temperature. There is no requirement for any air flow or thermal pad or heat sink and as such the core-loss figure is suitable for simple convective air flow when placed on a motherboard. Planar style cores do lend themselves to easy access to thermal pad/heat plate combinations since the core surface is broad and accessible.

It was also a desired goal in the design to give a substantial minimum floor on operating frequency. At a minimum rated frequency of 125 kHz the core loss rises to ~2.5 W. At the maximum rated frequency of 200 kHz, the peak-to-peak and rms flux density (in Gauss) was computed as:

$$B_{pkpk} := \frac{(V_{in} \cdot t_{on}) \cdot 10^{8}}{N_p \cdot A_c} \qquad B_{pkpk} = 3.472 \times 10^{3}$$

$$B_{rms} := \sqrt{\frac{2}{Tp}\cdot\int_0^{t_{on}}\left[\frac{(V_{in}\cdot t_{on})\cdot 10^8}{2\cdot N_p\cdot A_c}\right]^2 dT} \qquad B_{rms} = 1.617\times 10^3$$

At 200 kHz, the core loss is ~ 1.36 W.

We now proceed to evaluate copper loss.

One of the benefits of using planar construction is the opportunity to utilize 2-oz, 3-oz, and 4-oz copper weight, which results in very thin copper. The impact is that skin depth and proximity loss factors are usually much reduced versus using wire-wound magnetic structures. Knowing this to be true, we first examine copper loss based on dc resistance and will then extend it into an examination of ac loss due to frequency effects.

We pick the mid-range output current:

$$I_o := 25$$

The secondary rms current (I_{sec}) in each half of the center-tapped (CT) winding is:

$$I_{sec} := I_o\cdot\sqrt{D} \qquad I_{sec} = 16.47$$

Primary rms current (I_{pri}) may be computed as follows:

$$I_{pri} := I_o\cdot\sqrt{2D}\cdot\frac{N_s}{N_p} \qquad I_{pri} = 9.317$$

DCR values (Sec_DCR and Pri_DCR) are computed from the CAD drawings produced:

$$Sec\_DCR := .0023 \qquad Pri\_DCR := .025$$

Secondary copper loss is multiplied by 2 since it is a CT connection.

$$Sec\_loss := I_{sec}^2\cdot Sec\_DCR\cdot 2 \qquad Pri\_loss := I_{pri}^2\cdot Pri\_DCR$$

$$Sec\_loss = 1.248 \qquad Pri\_loss = 2.17$$

Now we simply add up total losses:

Loss RMS Method

$$Total\_loss1 := Sec\_loss + Pri\_loss + Core\_loss$$

$$Total\_loss1 = 5.466$$

Loss Fourier Method

$$Total\_Loss2 := Sec\_loss + Pri\_loss + \sum PP$$

$$Total\_Loss2 = 5.269$$

We need to recall that this is an iterative procedure. It seems a long way to go to arrive here but Mathcad and other programs simplify the task enormously. The results of each iteration performed for various core sizes and turns combinations and duty cycles can be evaluated and placed in a table format for comparison.

The major benefit of embedding the planar magnetics device is the improved thermal conductivity. A standalone device must conduct its heat out mainly through its terminals and convection to air. An embedded device has a shorter path and can spread its heat over a wider area.

This completes part 1 of the article. Part 2 will address the ac losses and the multi-layer PCB stack-up and design issues. More detail and complete design information can be found at the URLs indicated in Ref 1 and 2 below or by contacting the author.

References

1. Microchip dsPIC33F DC-DC Converter Reference Design
http://www.microchip.com/stellent/idcplg?IdcService=SS_GET_PAGE&nodeId=1406&dDocName=en549362

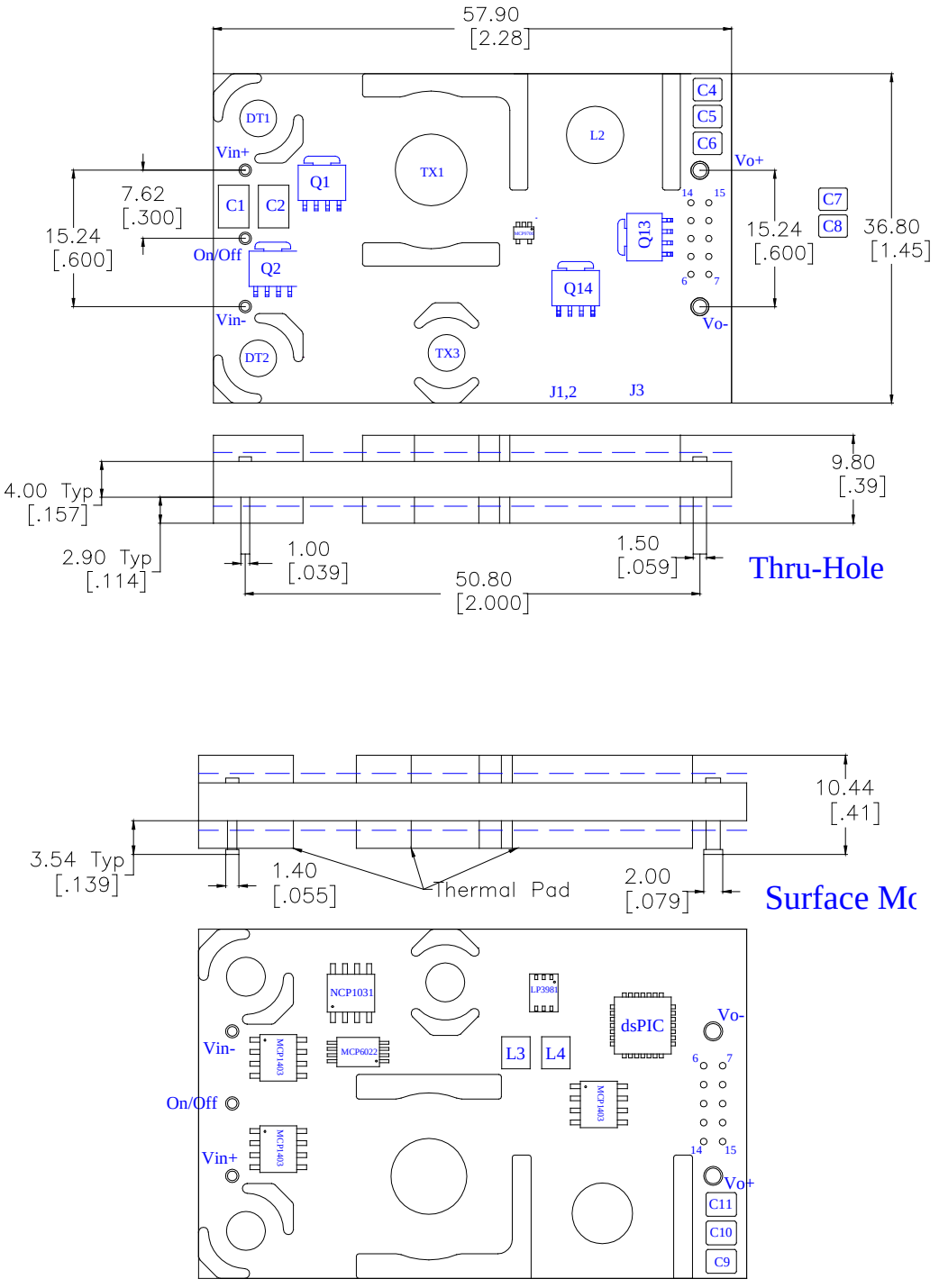
2. Champs Technologies Embedded DC-DC
http://www.champs-tech.com/Digital_Embedded_DC_DC.htm

3. Table. Ferroxcube Core-Loss Constants.

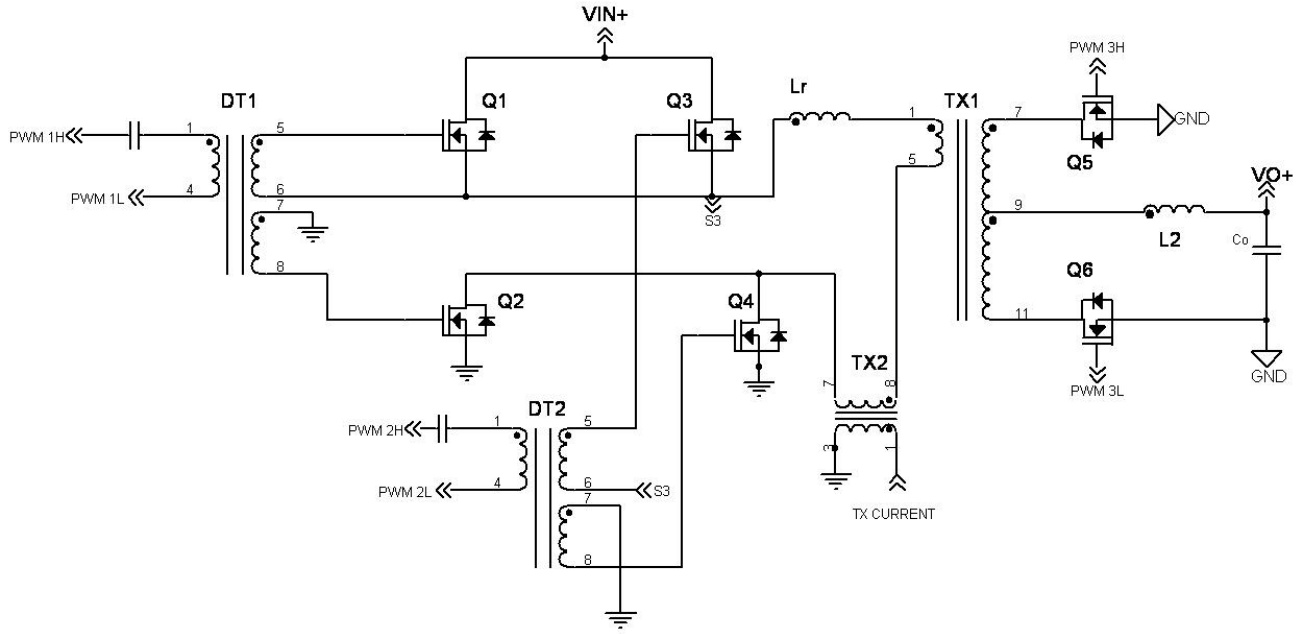
Matl	f (kHz)	Cm	x	y	Ct2	Ct1	Ct0
3C92	20-100	26.500	1.19	2.65	2.68E-04	5.43E-02	3.75
	100-200	0.349	1.59	2.67	1.51E-04	3.05E-02	2.55
	200-400	1.19E-04	2.24	2.66	2.08E-04	4.37E-02	3.29
3C96	20-100	5.120	1.34	2.66	5.48E-04	1.10E-01	6.56
	100-200	8.27E-02	1.72	2.80	1.83E-04	3.66E-02	2.83
	200-400	9.17E-05	2.22	2.46	2.33E-04	4.72E-02	3.39
3F35	400-1000	1.23E-08	2.95	2.94	1.38E-04	2.41E-02	2.03

Source: "New ER Cores for Planar converters". Ferroxcube Publication 939828800911 Sept 2002.

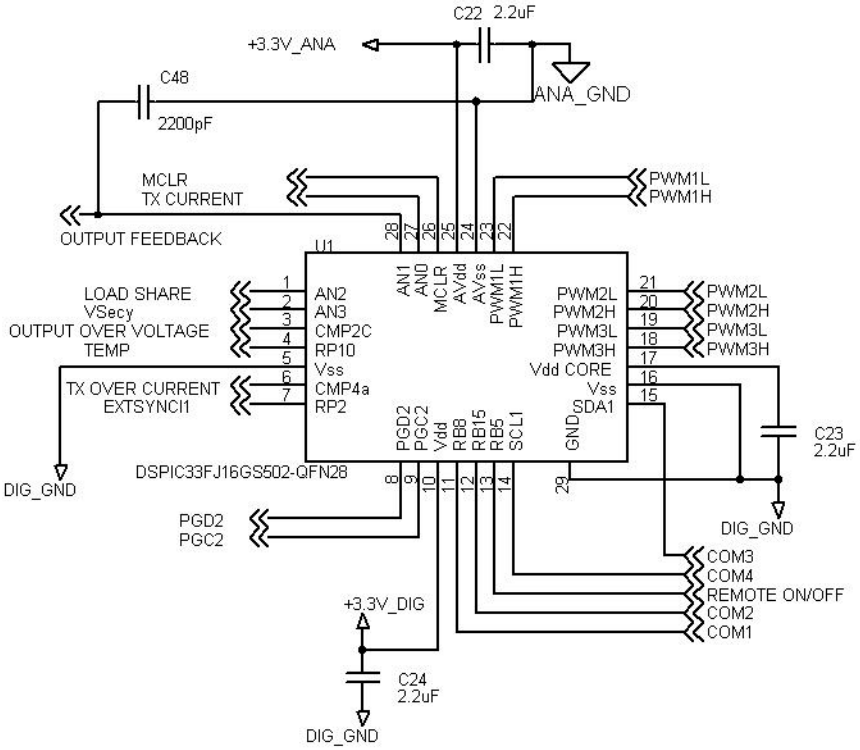
Appendix.



Appendix Fig. 1. Embedded magnetics dc-dc converter mechanical configuration.



Appendix Fig. 2. Embedded Magnetics Schematic (Illustrating magnetics).



Appendix Fig. 3. dsPIC33F Schematic

About The Author

Harold Eicher is VP of engineering at Champs Technologies, a company which he founded in 2005. In this role he has designed planar magnetics for telecom, industrial, computer and avionics markets. From 1985 to 2005, Eicher was the VP of engineering at Magnetico, which he also founded. At Magnetico, Eicher designed and developed magnetics and electronics for avionics, military, and space satellite markets. Eicher sold this company in Dec 2003 to Standex Electronics, but continued consulting through June 2005. Previously, Eicher was an engineer at AVM where he performed magnetics design and field application engineering. Eicher studied at Boston College where he obtained an AB degree in economics and political science, and then studied law, receiving a JD degree in 1979 from the Saint Louis University School of Law. The author can be reached via email at harold.eicher[at]champs-tech.com.

For further reading on magnetics design, see the How2Power Design Guide, search the Design Area category and select the Magnetics subcategory