Primary-Side Current Monitoring Won't Stop Overcurrents In DCM-Operated Flybacks

by John Bottrill, Senior Applications Engineer, and Lisa Dinwoodie, Applications Engineer, Power Management, Texas Instruments, Dallas, Texas

Many designers assume that the use of the primary-side pulse-by-pulse current monitoring and control in a flyback power converter is sufficient to limit the secondary-side current to slightly more than the maximum load requirement. A review of this technique demonstrates that this is not the case and that the current out of a flyback converter can easily result in higher than expected currents, if using this method. In turn, this can result in damage to the components in the power converter.

To explain why this is the case and why improved fault protection is needed, we'll begin by reviewing operation of the flyback converter and discuss the factors that leave the flyback converter vulnerable to an overcurrent event when operating in discontinuous mode. We'll then note the lesser impact of this problem on flybacks operating in the continuous mode. The focus here is on the discontinuous-mode (DCM) topology because it is the more popular topology, but also because this overcurrent problem is potentially more severe in DCM operation.

Flyback Operation

Fig. 1 shows a simplified circuit for the flyback converter that can be used to explain its operation.

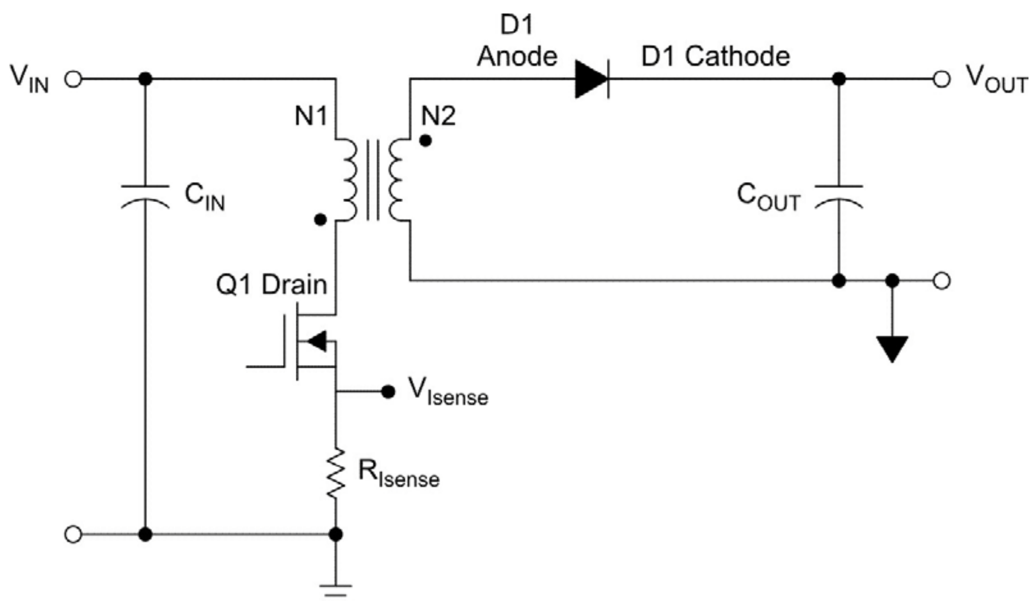


Fig. 1. Typical flyback topology power components.

To understand this discussion, it is important to recognize that the magnetic component of the flyback converter is not a transformer, but a coupled inductor. Energy is stored when the primary side switch, Q1, is on and this energy is released to the secondary side when Q1 is turned off. The current through Q1 at the point in time when Q1 turns off is equal to the initial current through the diode D1, once the turns ratio of the flyback inductor is taken into consideration.

The switching frequency (Fsw) and the maximum power out of the converter define the energy that the flyback inductor must process during each cycle of time (T) where

$$T = 1 \div Fsw\,.$$

In the design of a discontinuous-mode flyback converter, the maximum on time (Ton) of the primary switch must be less than the conduction time of the rectifying diode. If the reverse is true, the ringing of the primary side during light load and low-input voltage conditions could drive the drain of Q1 below ground. As this is not the subject of this article, we will not dwell on it here.

Examining the circuit requirements under minimum input voltage and maximum load leads to the design of the converter. We will assume that the duty cycle (Ton/T) of Q1 has a 45 percent maximum on time and a 50 percent maximum conduction time for the diode (D1).

The energy transferred during each cycle is the total input dc current (Idc) over a cycle T, multiplied by the input voltage. In a lossless system, this would be the same as the energy out of the converter. Let's assume for this discussion that we have a lossless system. We start with the following equation for charge:

$$Q = Idc_{in} \times T$$

where Q is the charge in Coulombs.

The energy in and out of the converter on a single cycle is defined as:

$$Energy = Q \times Vin = Vout \times Iout_{dc} \times T$$

When the main switch turns on, the current in the primary winding increases at a linear rate of di/dt. This is a function of the input voltage and the primary-side magnetizing inductance. When looked at on a scope, this forms a triangle. The area under that triangle must sum to Q.

$$di / dt = Vin \div Lmag$$

The integral of this triangle of current over the time Ton equals Q.

$$Q = 0.5 \times (Vin / Lmag) \times Ton^2 ,$$

which is the standard equation for the area of a triangle where the peak of the triangle is

$$Ipeak = (Vin / Lmag) \times Ton = (di / dt) \times Ton .$$

The energy being transferred to the secondary on each pulse is a function of the peak current and the magnetizing inductance

$$E = .5 \times Ipeak^2 \times Lmag$$

Since we know the input voltage (V_{IN}), the frequency Fsw (which gives us T), the duty cycle (Ton) and the power which gives us Idc and allowing for losses (in this case it is zero as we have defined it as a lossless system), it is relatively easy to calculate the maximum Lmag that will work for the primary side.

We know that when Q1 turns off, the energy stored in the inductor will cause the voltage on the anode of D1 and the drain of Q1 to increase. The voltage on D1 will increase until D1 is forward biased and the current out of N2 will equal

$$Ipeak \times (N1 \div N2) = Ipeak_{out}$$

since the same number of ampere-turns are needed as they represent the stored flux in the magnetic material. Now using the same equations, it is easy to identify the secondary inductance (Lmag-s). The typical circuit is shown in Fig. 1 and the associated waveforms are presented in Fig. 2.

The waveforms shown in Fig. 2 have been normalized for inputs and outputs, and the effects of leakage inductances are being ignored. Losses in the FET Q1 and the diode D1 are ignored. The top waveform is the voltage on the drain of Q1. The middle waveform is a composite of the current in the primary winding (black) and the secondary winding (red). The bottom trace is the voltage on the anode of D1.

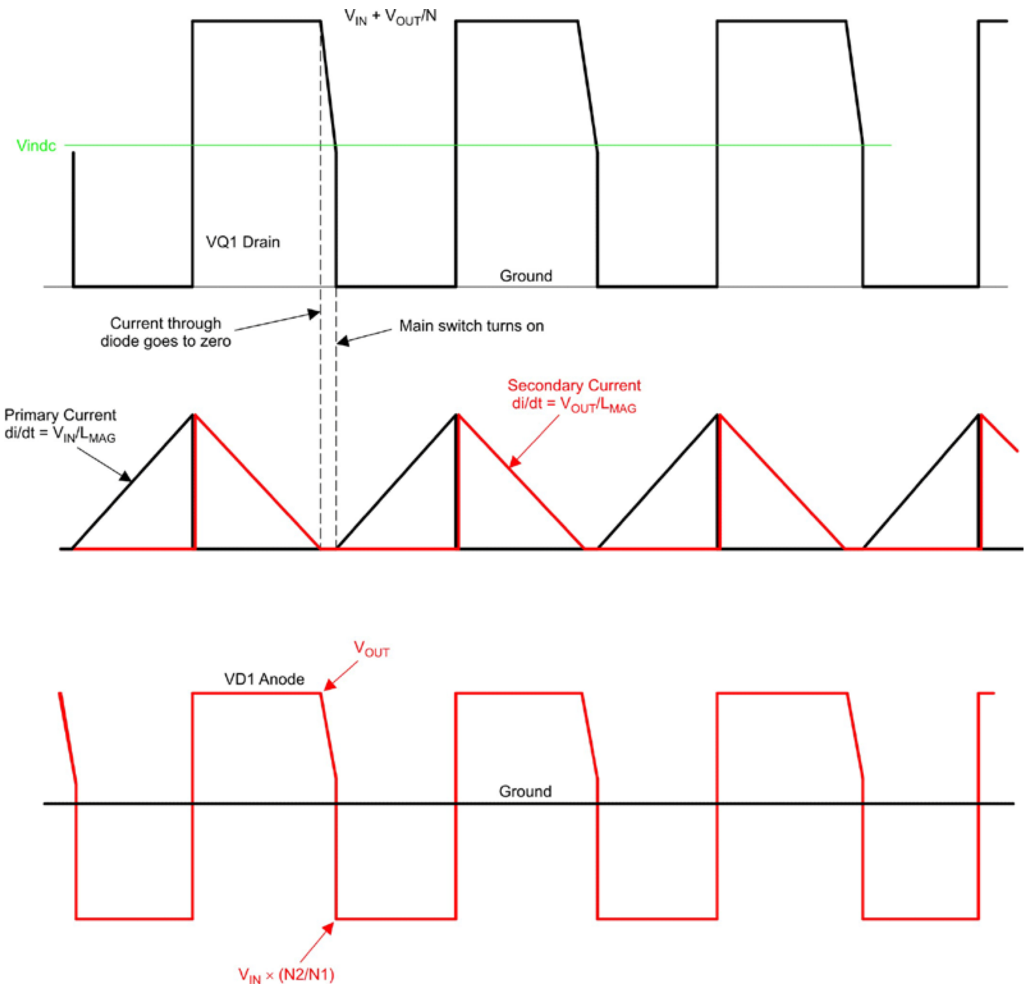


Fig. 2. Idealized voltage and current waveforms for a discontinuous-mode flyback converter.

As can be seen in the discontinuous mode, the current on the output falls to zero in each cycle. The peak current on the primary is sensed across the resistor, RIsense. This voltage level is compared to a control level and triggers the turn off of the FET. The control level is a function of the output voltage and the voltage feedback loop.

The overcurrent threshold limit is a function of internal set points in the controller. This overcurrent limit by design of the converter is user-defined to trigger if the input current peak gets to a level that is between 20 and 50 percent above the maximum current for the worst-case load condition. This allows the converter to handle transients without damaging the devices. This threshold tolerance depends on the IC, but the lowest trip point must be sufficiently above maximum worst-case operation to allow for transients.

For demonstration purposes, we will assume that there has been a sudden and permanent low impedance applied across the output so that the output voltage drops immediately to some arbitrary value, say 20 percent of nominal (see Fig. 3). Additionally, we will assume that the control loop responds instantly.

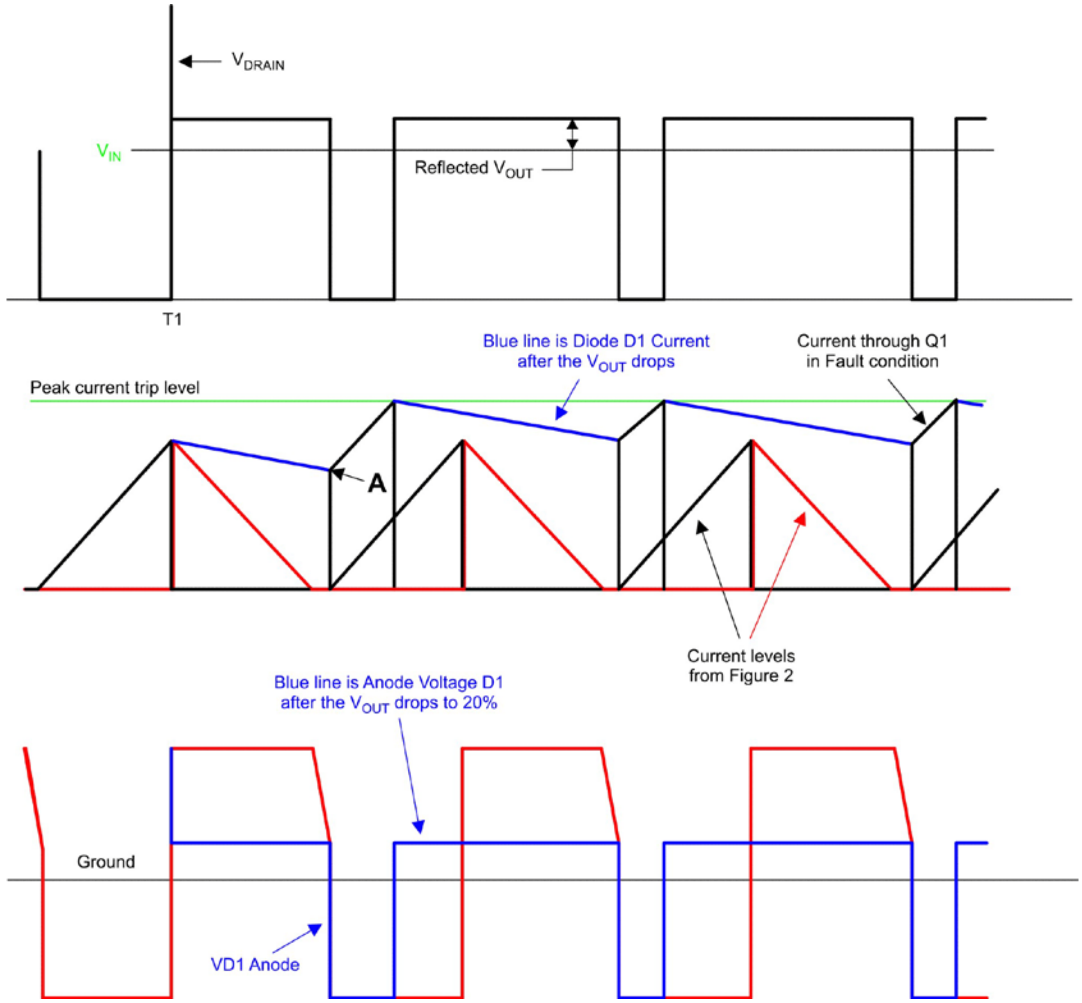


Fig. 3. Output voltage drops to 20 percent of initial value.

The result is that the di/dt of the output side of the coupled inductor decreases because the voltage across the secondary winding has decreased.

The voltage on the output has dropped (immediately after Q1 turns off on the first pulse of Fig. 3) so the control loop is now demanding more current. The main switch of the converter on subsequent pulses stays on until the primary current reaches the over current limit and shuts off the switch.

The current out of the inductor is significantly higher now than during normal operation, but the di/dt on the secondary is much lower also because the output voltage has dropped. Because the di/dt is so much lower, there is residual energy in the inductor when the converter main switch turns back on. And because there is residual current in the inductor when the main switch turns back on at the beginning of the next cycle, the primary-side current starts with an offset and reaches the overcurrent trip peak much faster. This results in reduced on time of the main switch and increased conduction time for the diode at higher currents. This does not mean there is more energy being transferred, only more current.

Fig. 3 shows the impact of the change in both the input and output voltage waveforms and current under these conditions.

As shown in Fig. 3, when the output voltage drops, the voltage on the anode of D1 drops as does the reflected voltage on the drain of Q1. Because the voltage across the winding drops, this changes the slope of the current out of that winding. This slope change results in the current through the secondary not going to zero before the initiation of the next power pulse. When the next power pulse starts the current in the coupled inductor, primary side starts at a level above zero (point A of Fig. 3).

When taken to the extreme limit with the output voltage dropping to zero, the down slope becomes flat and the on time of the main switch approaches zero. This means the current out of the diode will reflect the primary side overcurrent limit reflected to the secondary and at a near-continuous level.

If the peak current limit is 50 percent higher than the nominal maximum output current maximum trip point and the output voltage approaches zero volts, it is possible to get a rough estimate of the output current as a percentage of the Imax.

In operation with a 50 percent conduction time for the diode, the peak current is a factor of four times the peak dc output current. When the overcurrent trip point is reached, the peak will be 50 percent higher, resulting in six times the nominal maximum dc output current. By the same token, the primary-side input current has decreased because of the shorter on time of Q1. If the circuit has leading-edge blanking, which prevents the controller from seeing the initial current spike, this current level can be much, much higher. If the converter has not been designed for this continuous current level, it likely will be destroyed by running for an extended time with this output current.

A similar outcome is likely for the continuous-mode flyback converter, although the output current will not increase by a factor of six. More than likely it will hit a factor of two or three because the initial output slope is shallow and does not go to zero normally.

Again, under these conditions, leading-edge blanking will impact the current level in a negative manner.

To prevent this type of failure from destroying the converter (and for other reasons), the power to the control IC is usually off an auxiliary winding on the flyback converter. If the output voltage drops for more than a few hundred milliseconds, the converter is shut down and must attempt to go through a soft start, usually with a significant delay before restart.

Recent IC developments recognize this potential catastrophic failure for the discontinuous topology. These devices prevent the main switch from turning on again as long as there is current in the output winding of the transformer. Test data from an evaluation model (EVM) with this type of controller is shown in Fig. 4, illustrating the output current of the unit.

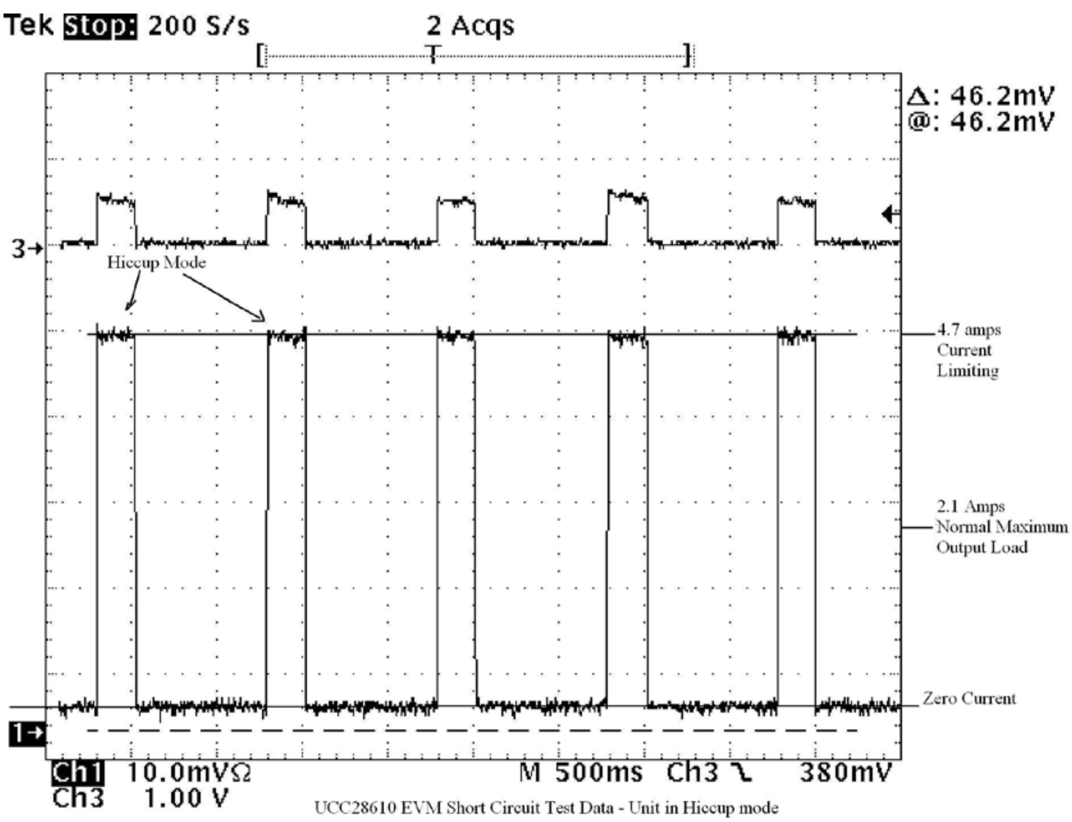


Fig. 4. Short circuit test data.

The pulses of current are a result of the intermittent operation where safety features inside the IC allow it to operate in the fault condition for a short period, then shut everything down for a predetermined time.

The image (Fig. 4 again) shows a converter with a normal 2.1-A output operating into a shorted output. The output current goes to 4.7 A average for the duration of the operating pulse.

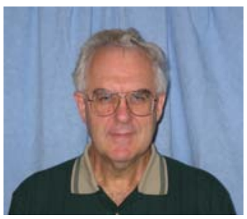
The output short circuit current can be defined as:

$$I\sec\_sc = ((Np/Ns) \times Ipeak) \div 2$$

Conclusion

Operating a flyback converter without the added protection like that provided by the latest-generation of controllers leaves the converter vulnerable to major damage in the event of a short circuit on the output. That is, unless additional circuits are added around the controller IC to prevent such damage. In the future, power converters using these controller ICs will be even better equipped to handle short-circuit conditions as the latest-generation controllers continue being developed to prevent this problem from occurring.

About the Author



John Bottrill is a senior applications engineer at Texas Instruments in Manchester, NH. John supports customers and evaluates new ICs before release. In doing so, he has produced more than 20 technical papers and has two patents to his credit. He received his B. Sc. in Electrical Engineering from Queen's University at Kingston, Ontario, Canada. You can reach John at ti_johnbottrill@list.ti.com.

Lisa Dinwoodie is an applications engineer at Texas Instruments where she supports customers, evaluates new ICs before release, and designs evaluation modules for customer use. Lisa has more than 16 years in the power supply design industry. She received her B.Sc. in Electrical Engineering from Northeastern University in Boston, Massachusetts. You can reach Lisa at ti_lisadinwoodie@list.ti.com.

For further reading on flyback converter design, see the How2Power Design Guide, search the Topology category and select Flyback as the subcategory.