HOW2POWER TODAY
Your Power Design Newsletter

Powering The Digital Media World
An Informative Monthly Column
Sponsored by IDT – Integrated Device Technology

ISSUE: June 2011

# *Dedicated Driver Squeezes Optimal Performance Out Of Enhancement-Mode GaN FETs*

*by Ashok Bindra, Technology Writer, Technika*

The emergence of commercial gallium-nitride-on-silicon (GaN-on-Si) based power transistors is very recent. While these transistors have a lot to offer, squeezing maximum performance out of these devices is tricky. Also, to effectively compete with entrenched silicon power MOSFETs, the designers must deliver an optimal combination of efficiency, size and cost.

To squeeze maximum performance from a GaN-on-Si device requires dedicated drivers that can maximize efficiency from a smaller die size to realize conversion efficiency and power density that is beyond the scope of power MOSFETs. To make GaN-on-Si transistors cost competitive with MOSFETs, GaN manufacturers are adopting larger silicon substrates.

Fundamentally, there are two types of GaN FETs, depletion-mode and enhancement-mode. Depletion mode is the normally-on type, while enhancement-mode is normally-off. Now, based on their properties, the drive requirements for each are different.

We know Efficient Power Conversion (EPC) has commercialized enhancement-mode GaN-on-Si FETs, or eGaN FETs as EPC calls them, for more than a year now. Concurrently, it has been working with partners to realize dedicated drivers for its eGaN FETs, which offer lower $R_{DS(ON)}$ at higher voltages, lower gate charge, and no reverse recovery loss ($Q_{RR}$)—all these properties from a smaller die size than silicon. In essence, by comparison to silicon MOSFETs, the eGaN FETs offer a dramatic reduction in figures of merit or FOM (Fig.1).

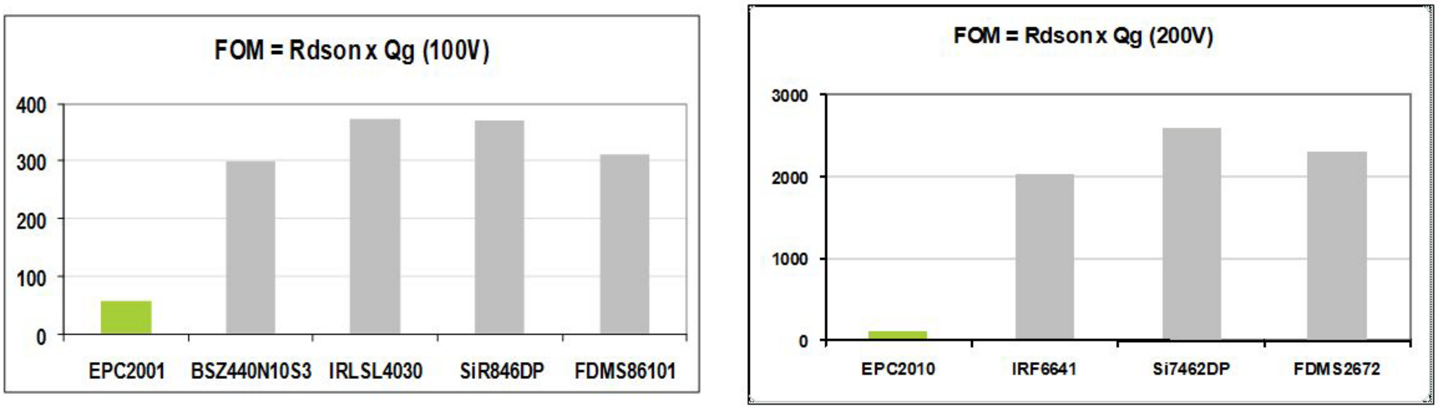


*Fig.1. In comparison to power MOSFETs with similar voltage ratings, eGaN FETs offer dramatically lower figures of merit or FOM.*

Because requirements for an eGaN FET gate driver are very stringent, three things must be kept in mind when driving eGaN FETs. First, they are sensitive to layout because of the high-frequency capability of the transistors. Second, eGaN FETs are more sensitive to gate overstress than similarly rated silicon MOSFETs. And absolute gate voltage must be less than 6 V. As a result, these transistors require a gate overvoltage clamp for protection.

Also, the gate threshold voltage is less than 1.4 V, which is much lower than that of MOSFETs. That means, eGaN FETs are prone to fault turn-on due to dV/dt during turn-off. Thus, these devices require a low-impedance driver to turn off the eGaN FET. Lastly, the body diode function has no $Q_{RR}$, but a large forward voltage drop (>1.5 V). Hence, to minimize conduction losses due to the large forward voltage drop, the dead-time must be minimized and precisely controlled.

Taking all these factors into consideration, National Semiconductor has developed the industry's first 100-V optimized half-bridge driver for eGaN power FETs. Called the LM5113, it offers precision gate voltage drive with flexible drive capability and matching of propagation delay between high-side and low-side drive for precise on/off timing of eGaN power FETs.

As shown in Fig.2, the high-voltage bipolar-CMOS-DMOS (BCD) based LM5113 incorporates on-chip independent source and sink outputs, bootstrap voltage limiter, independent TTL inputs for high- and low-side drivers, an optimized UVLO, and a voltage regulator. The package is National's 4 x 4 mm LLP-10.

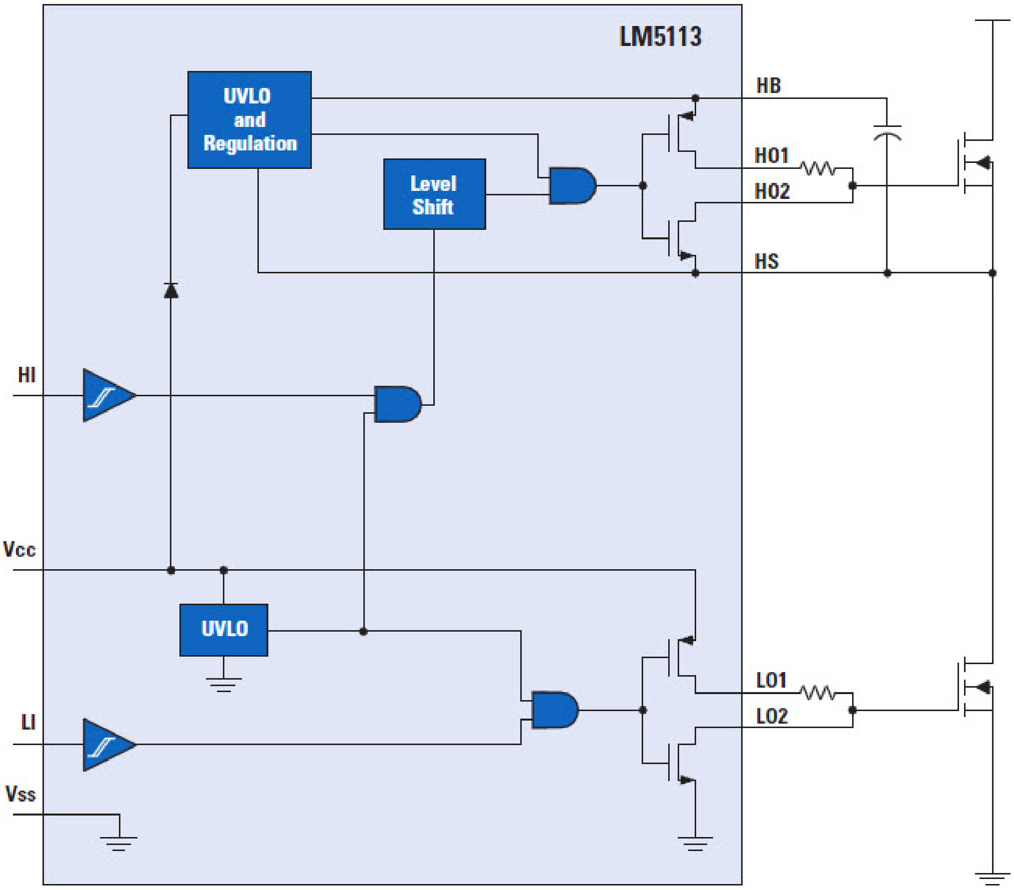
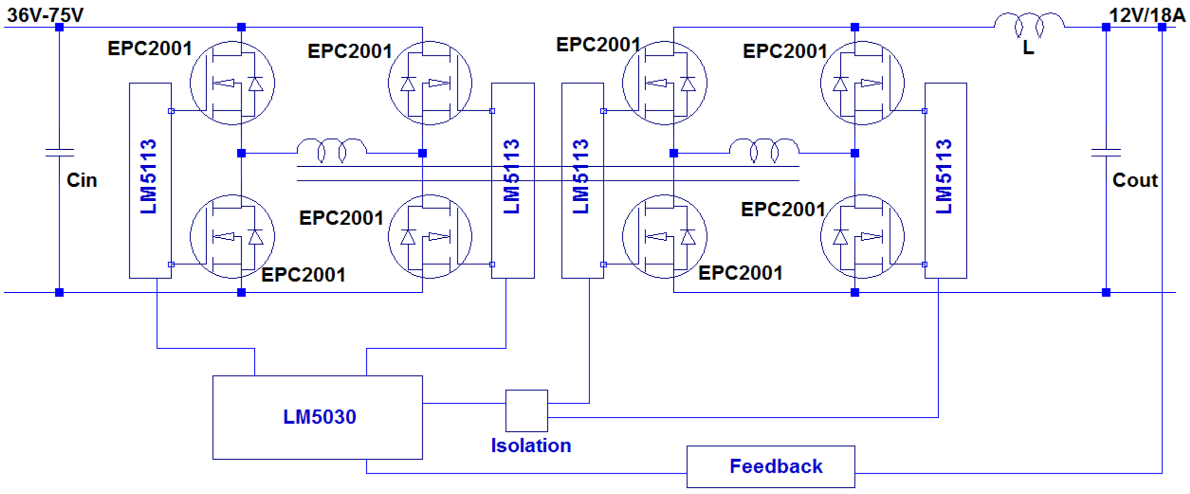


*Fig.2. Implemented in a high-voltage BCD process, the half-bridge gate driver LM5113 incorporates on-chip independent source and sink outputs, bootstrap voltage limiter, independent TTL inputs for high- and low-side drivers, and a tailored UVLO to optimally drive eGaN FETs.*

"Using proprietary technology, the device regulates the high-side floating bootstrap capacitor voltage at approximately 5.25 V to optimally drive eGaN power FETs without exceeding the maximum gate-source voltage rating," said James MacDonald, marketing director for National Semiconductor's Infrastructure Power Business unit. He added, "A low impedance pull down path of 0.5 ohms provides a fast, reliable turn-off mechanism for the low threshold voltage eGaN power FETs, helping maximize efficiency in high-frequency power supply designs."

According to the marketing director, the LM5113's integrated high-side bootstrap diode further minimizes PCB real estate. Also, the driver's independent logic inputs for the high- and low-side drivers enables flexibility in a variety of both isolated and non-isolated power supply topologies.

To evaluate the performance of the driver in a real world application, an eighth-brick module, offering 12-V regulated output for a 48-V input, was built using the LM5113 and 100-V, 7-mΩ EPC2001 eGaN FETs as shown in Fig.3. The measured efficiency results are compared with a similar design based on MOSFETs. The efficiency comparison is presented in Fig.4. As depicted in this figure, over a wide input range of 36 V to 75 V, and across a wide load range, the eGaN and LM5113-based eighth brick delivers 1% improvement versus a MOSFET solution. Besides the improvement in efficiency, the eGaN FET brick also brings a significant reduction in the component count and a substantial savings in the PCB area.



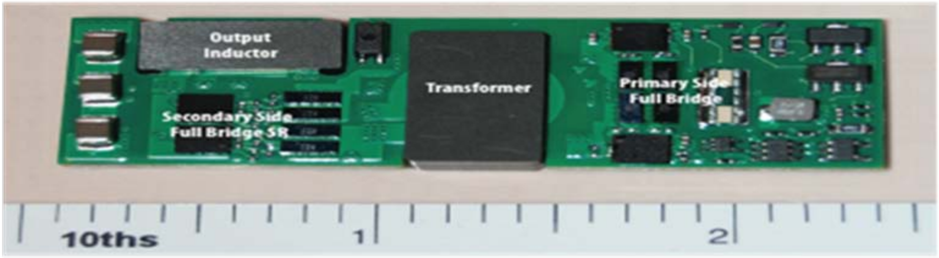


*Fig.3. The isolated 48-V in to 12-V out eighth-brick module uses the optimized driver LM5113 and EPC's 100-V eGaN FETs EPC2001 to realize higher conversion efficiency.*

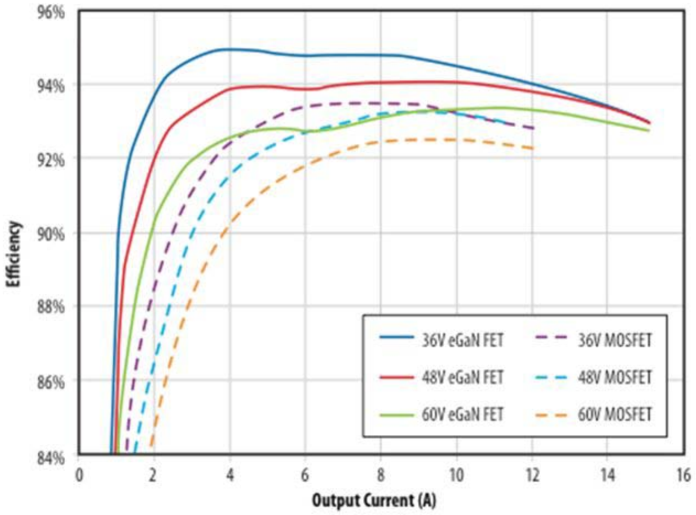


*Fig.4. In comparison with a MOSFET-based eighth brick, the eGaN FET and LM5113 driven eighth-brick module delivers at least 1% improvement in efficiency across a 6- to 12-A load. The power converter used to test these transistors was designed for operation at 36-V to 75-V input and 12-V, 15-A output. Measurements were taken with eGaN devices switching at 333 kHz and the MOSFETs switching at 250 kHz.*

## About The Author

*Ashok Bindra is a veteran writer and editor with more than 25 years of editorial experience covering RF/wireless technologies, semiconductors and power electronics. He has written, both for print and the web, for leading electronics trade publications in the U.S, including Electronics, EETimes, Electronic Design and RF Design. Presently, he has his own technical writing company called Technika through which he does writing projects for different trade publications and vendors. Prior to becoming an editor, Bindra worked in industry as an electronics engineer. He holds an M.S. degree from the Department of Electrical and Computer Engineering, Clarkson College of Technology (now Clarkson University) in Potsdam, NY, and an M.Sc (Physics) from the University of Bombay, India. He can be reached by email at bindra1[at]verizon.net.*