Tapped Inductors Enable Simple, Compact Buck-Boost Converters With Single Noninverting Or Dual, Complementary Outputs

by Hector F. Arroyo, National Semiconductor, San Diego, Calif.

Many applications require nonisolated, positive-output dc-dc converters where the output voltage falls within the input voltage range. This type of buck-boost converter finds use in industrial, automotive and low- and medium-voltage battery systems, among others. Today, these systems must not only be efficient, they must also be as compact and power dense as possible.

Traditional approaches such as SEPIC, four-switch buck boost or transformer-based topologies including flyback, forward and push-pull can provide a converter solution for the application needs. However, depending on the topology selected, these approaches also bring some compromises in the form of increased size, complexity or losses.

This article introduces and analyzes a different approach based on a tap-to-ground tapped-inductor buck-boost architecture. Converters based on this architecture are compact, uncomplicated and flexible enough to be used in single-output applications as well as those demanding dual complementary rails. The latter requirement is very common when powering analog electronics.

Existing Buck-Boost approaches

Topologies needing the lowest number of elements in the power train require only two switches and a single-winding magnetic device. Buck, boost and inverting buck-boost topologies all meet this minimalistic component criterion, with either two active switches or one active switch and one diode (Fig. 1).

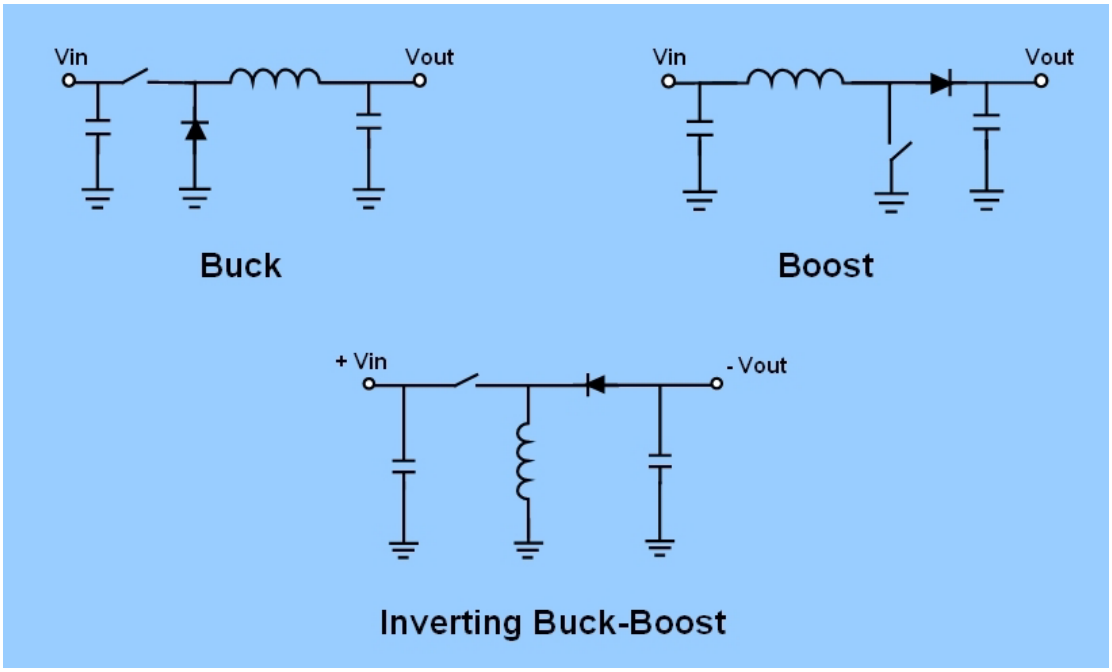


Fig. 1. Two-switch single-inductor topologies: buck, boost and inverting buck-boost.

It would be ideal if such simplicity could also be used to implement the noninverting buck-boost functionality; however, common architectures used to generate an output voltage that falls within the input-voltage range usually include additional elements in order to achieve it.

The SEPIC topology, for example, requires the use of two-winding magnetics, embodied either as two individual inductors or as a coupled-winding version.[1] This topology also uses a coupling capacitor between the input and output, which can carry high currents and can turn into a weak link in terms of reliability.

The four-switch buck boost, while using a single inductor, introduces the added complexity in its inherent four-switch architecture. Moreover, this architecture can decrease conversion efficiency due to the conduction and switching losses associated with its multiple switching elements.

The transformer-based implementations add extra complexity in the transformer itself and depending on the actual topology used may need additional primary-side switches or secondary-side rectifiers and inductors.[2,3]

Based on this need for a simpler noninverting two-switch buck-boost implementation, the proposed tapped-inductor approach is introduced.[6] Fig. 2 shows the basic architecture.

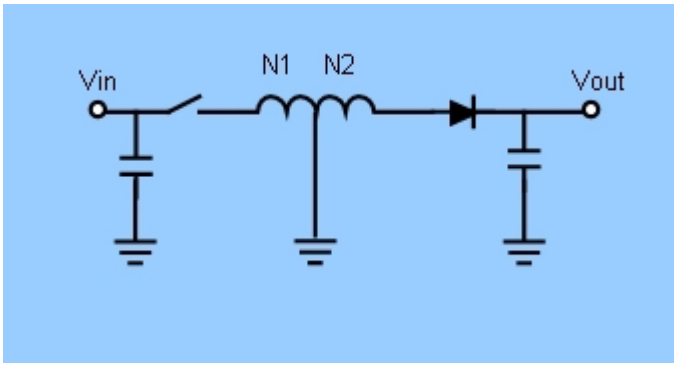


Fig. 2. Simplified implementation of a tapped-inductor-based single-output buck-boost converter.

Operating Principle

During the switch on-time (refer to Fig. 2), the N1 winding of the inductor will be energized and a current will flow from the input to the tap (ground). Following an autotransformer principle, the N2 winding will also develop a voltage across it, same as the one across N1 in magnitude but sized in proportion to the relationship of the number of turns between N1 and N2. If the turns in N1 and N2 are equal, the voltage at the right of the inductor will be –Vin. Since this voltage is negative during the on-time, the diode is reversed biased and no current flows through N2.

As the switch opens, current stops flowing through N1 and the energy stored in the inductor is released, causing a current to flow through N2, and imprinting a positive voltage on its right side. This positive voltage forward biases the diode and charges the output capacitor to produce a positive output voltage. During the off-time, the voltage across N1 is again the same as the one across N2 but scaled in proportion to the turns ratio between N1 and N2. If N1 and N2 are equal in the number of turns, the voltage at the far left of the inductor during the off-time is equal to –Vout.

The switch duty cycle and the location of the tap within the inductor (N1-to-N2 turns ratio) determine the Vout /Vin transfer characteristic, which may be >1 (gain) or <1 (attenuation). Assuming no losses, for N1 = N2 and D = 0.50, Vout = Vin. For a different duty cycle or tap location, the Vout/Vin transfer function is given by the following equation.

$$\frac{Vout}{Vin} = \frac{D}{1-D} \cdot \frac{N2}{N1} \qquad \text{Eqn. 1}$$

Fig. 3 plots the equation above, showing the Vout/Vin relationship for a duty-cycle range from zero to almost one for different inductor-tap ratios.

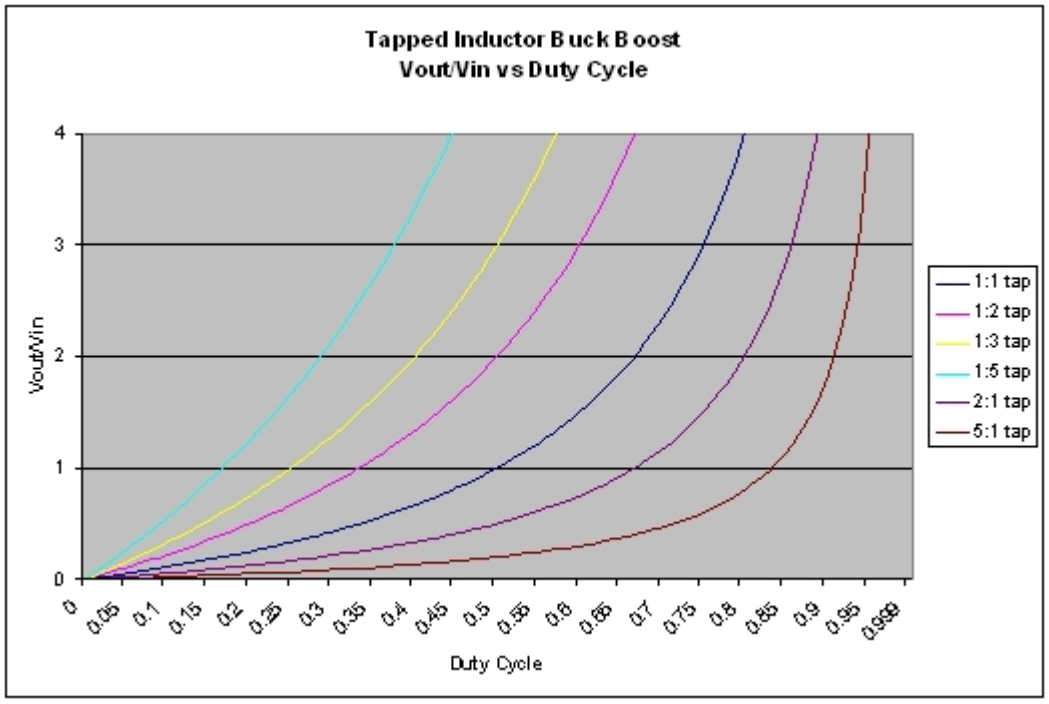


Fig. 3. Vout/Vin vs. duty cycle for different inductor-tap ratios.

Practical Implementation

As a whole, tapped-inductor architectures are not new in the industry. Tapped-inductor boost (tap to switch) and tapped-inductor buck (tap to diode) are relatively popular versions that have been used to help stretch the capabilities of the traditional boost and buck topologies. Through their use, it has been possible to boost output voltage, boost output current, or shift the duty cycle to more practical areas of operation, thereby making extreme stepup or stepdown conversion ratios feasible with simple boost and buck circuits.[4, 5]

Until recently though, most tapped-inductor designs needed custom magnetics, which prevented tapped-inductor solutions from becoming more popular. Today, most magnetic manufacturers provide off-the-shelf, compact, coupled inductors with 1:1 turns ratios, and in a few cases 1:N. These offerings make tapped-inductor architectures an extremely easy-to-implement option at any given production volume.

Fig. 4 shows a complete tapped-inductor buck-boost circuit implemented using the architecture introduced in Fig. 2, leveraging a controlled on time (COT) switching controller from National Semiconductor (LM5085). A switching controller using an external MOSFET was selected to allow flexibility in the voltage and current ratings of the MOSFET. The COT architecture was selected since it's simple to use, and requires no loop stability analysis nor stability-compensation components.[7]

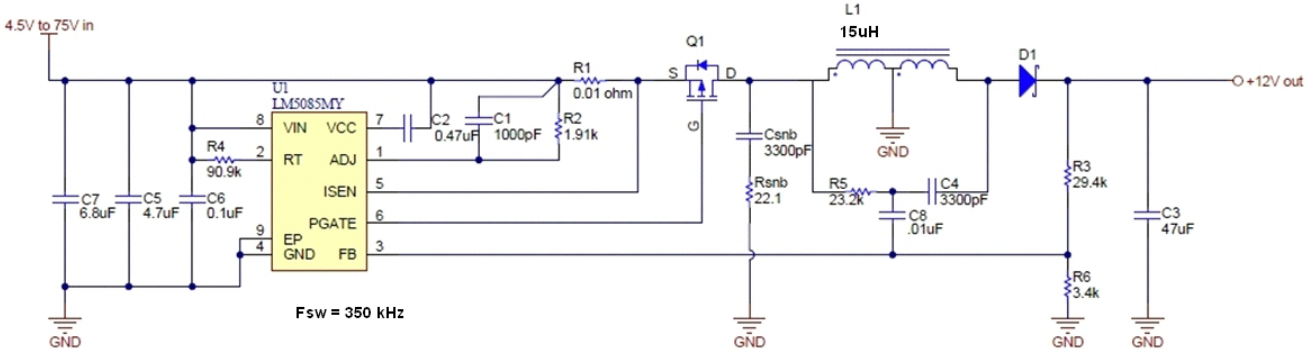


Fig. 4. Practical implementation of a single-output buck-boost using an LM5085 COT controller.

In the circuit, C7 and C5 are input capacitors. R4 sets U1's on-time for a given Vin, thus setting switching frequency. R1 is used as a current-sense resistor to implement current limiting. R3 and R6 set the output voltage. C3 is the output capacitor. R5 and C4 are small-signal components used to create a triangular waveform from the switching node and couple it to U1's FB pin through C8 for proper COT operation. Csnb and Rsnb form a snubber circuit used to dissipate ringing caused by any leakage inductance between the two windings in L1.

Q1, L1 and D1 need to be selected based on the desired output current of the circuit, and the Vout-to-Vin ratio. If N1 = N2, current stresses in both sides of L1 are basically the same, with an average ideal value, when conducting, of Iout x ((Vout/Vin) + 1). This is the same as most other buck-boost topologies.

Components should be selected based on peak currents (particularly for L1, to avoid saturation), which can be calculated adding half of the inductor ripple current to the average value above. Inductor ripple current (peak to peak) can be calculated using the standard relationship:

$$\Delta I_L = \frac{V_L \cdot t_{on}}{L} \qquad \text{Eqn. 2}$$

where V_L is the voltage applied across an inductor winding, t_{on} is the time this voltage is applied and L is the inductance value of such winding. In the case of the tapped-inductor buck-boost architecture, this relationship may also be expressed as:

$$\Delta I_L = \frac{V_{in} \cdot D}{L \cdot f_{sw}} \qquad \text{Eqn. 3}$$

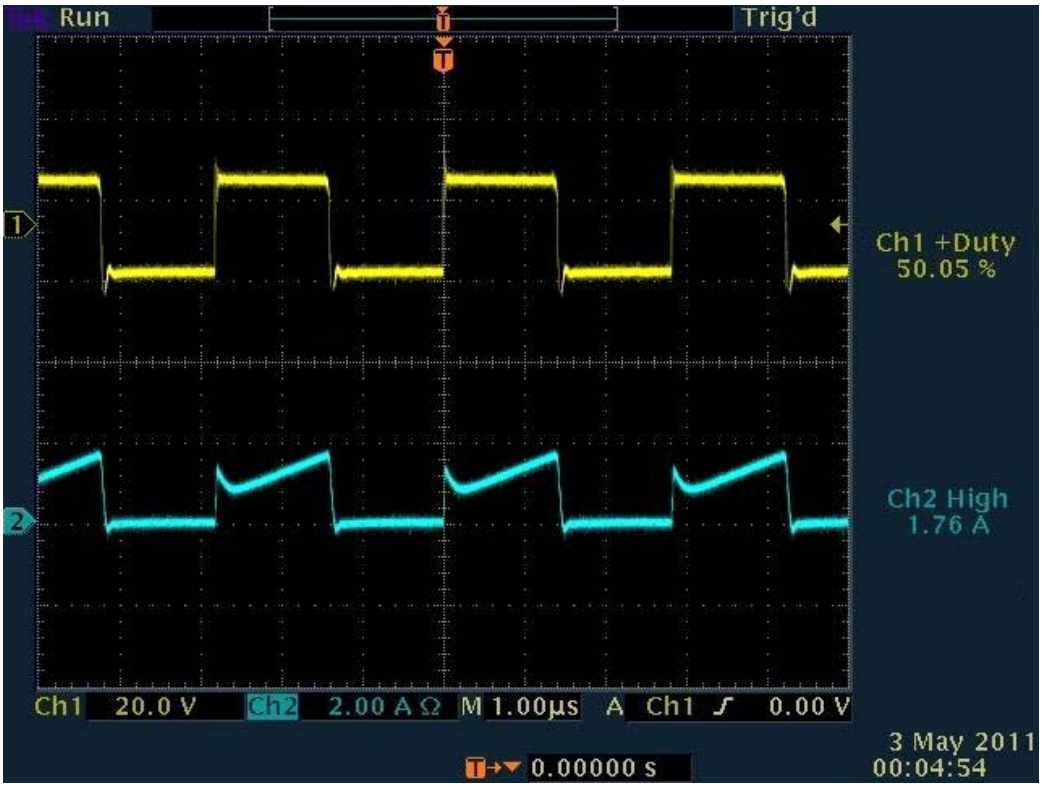
where V_{in} is the circuit's input voltage, D is the operating duty cycle, f_{sw} is the operating switching frequency and L is the inductance of the N1 portion of the inductor.

For Q1's Vds rating, a value larger than V_{in} + V_{out} should be selected, since this MOSFET will be seeing a voltage stress of at least that magnitude across it during regular operation.

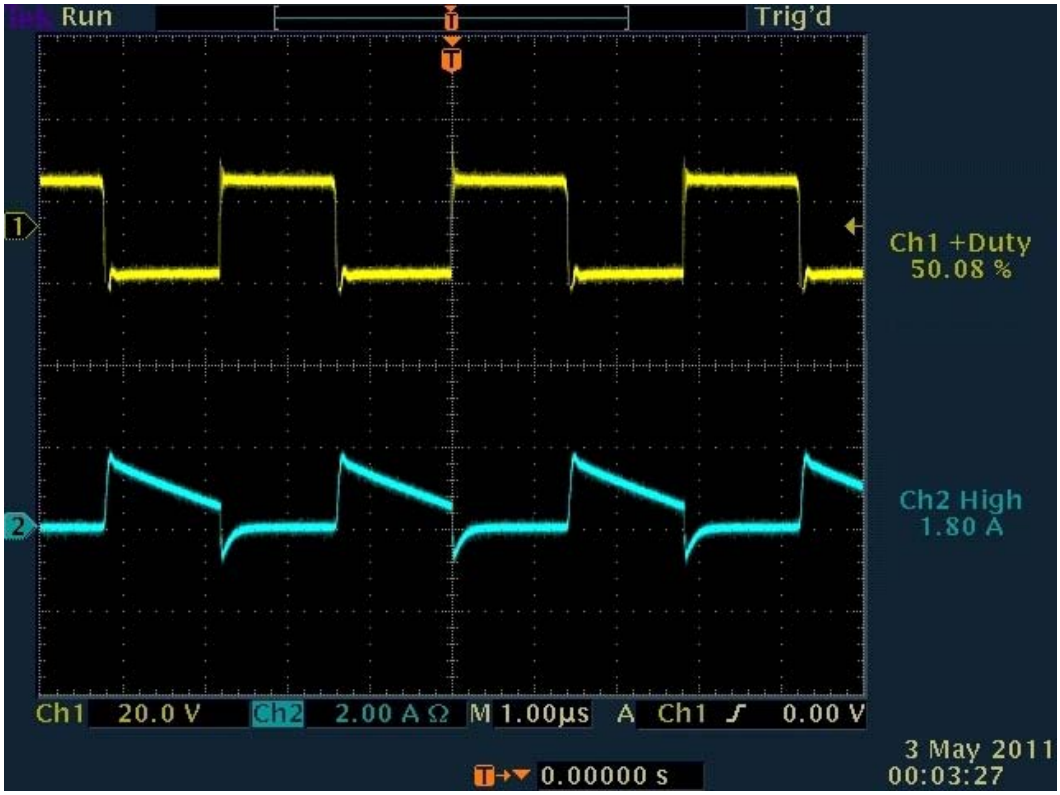
For L1, a dual-winding coupled inductor may be used. It is important to select one with the highest coupling available to minimize leakage inductance.

In the prototype, Wurth's 744873150 coupled inductor was used for L1. [10]

Fig. 5 parts a and b are oscilloscope images showing the operating waveforms for the circuit in Fig. 4. In both a and b, the yellow waveform on top is the signal measured at the switching node (Q1's drain.) Meanwhile, the blue waveforms in parts a and b are the currents through N1 and N2, respectively. The measurements were taken with the prototype circuit running at 12-V input, 12-V output and a test load of 500 mA.



(a)



(b)

Fig. 5. Operating waveforms for the LM5085 single-output buck-boost circuit in Fig. 4. Yellow waveforms are for the switching node (Q1's drain), while blue waveforms are for currents through N1 (part a) and N2 (part b).

Complementary Dual Outputs

In addition to generating Vout, during the switch off-time the architecture in Fig. 2 generates a duty-cycle-controlled voltage at the far left of the inductor. The polarity of this voltage is the opposite of Vout. Because of the presence of this secondary voltage, this circuit may be easily expanded to implement a dual-polarity generating architecture. Fig. 6 shows the simplified implementation of such a converter.

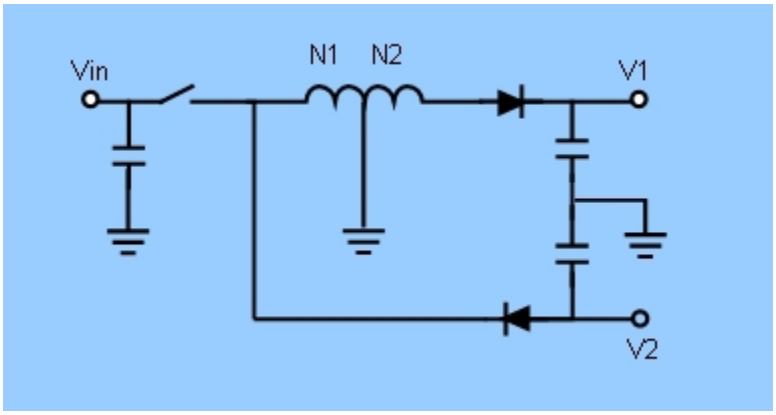


Fig. 6. Simplified implementation of a tapped-inductor-based buck-boost converter with dual outputs.

In this implementation, the V1-to-Vin relationship is still controlled by the duty cycle and the tap location as determined by equation 1. The V2-to-Vin relationship is tap location independent (it only requires N1 to be > 0 to exist), and is controlled by the switch duty cycle as given by:

$$\frac{V2}{Vin} = \frac{-D}{1-D} \qquad \text{Eqn. 4}$$

Fig. 7 shows a modified version of the circuit in Fig. 4 that generates dual complementary outputs. This circuit is very similar to the one in Fig. 4. Only an additional diode D2 and output capacitor C9 have been added, while the snubber components Csnb and Rsnb have been removed. These components are no longer necessary since there's always current flowing through N1 during the t_{on}-to-t_{off} transition when the V2 output has a load attached.

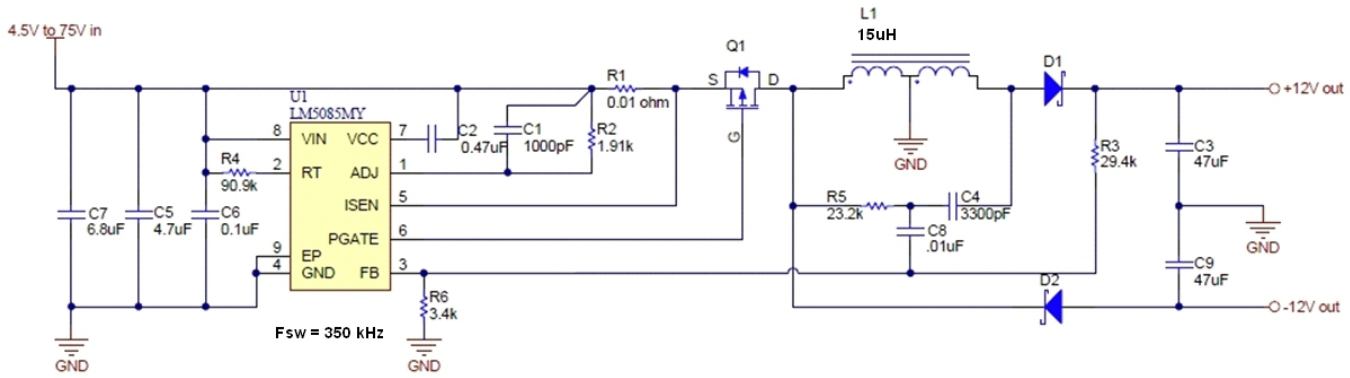


Fig. 7. Dual-output implementation using an LM5085 hysteretic COT PFET controller.

A more compact implementation using a monolithic switching regulator is also possible and Fig. 8 shows an example of such an implementation, leveraging National Semiconductor's LM22670 simple switcher regulator.[8] By combining a compact, off-the-shelf tapped inductor and a monolithic switching regulator with built-in FET and internal compensation, the simplicity of the proposed architecture in Fig. 6 may be better demonstrated.

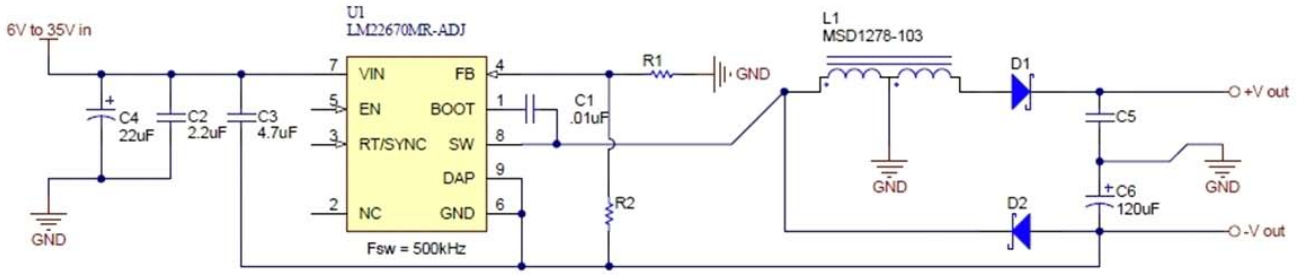


Fig. 8. Dual-output implementation using an LM22670 PWM voltage-mode monolithic switching regulator.

The circuit from Fig. 8 leverages another readily available, off-the-shelf compact inductor (Coilcraft's MSD1278.) This component has two windings in a 1:1 relationship and features a very high coupling ratio.[9]

Using a monolithic (internal MOSFET) IC, the system's max Vin will be somewhat lower than the IC's max Vin, depending on the output voltage selected.

For example, in the case of the LM22670 circuit of Fig. 8, the Vin range for U1 can go up to 42 V. However with a Vout of 5-V, the systems' input shouldn't be higher than 42 V – 5 V = 37 V. Thus, a max of 35 V is recommended. If Vout is raised to 12 V, a lower max Vin should be used accordingly.

When using a regulator with a built-in MOSFET, the GND pin of the IC may be referenced to the most negative rail in the system so the SW pin does not see a swing below the IC ground. Most commercially available ICs today limit how negative the SW pin may go (usually less than a couple of volts) by ESD protection diodes. So this approach, as shown in the Fig. 8 circuit, leverages existing off-the-shelf ICs for an easy dual-output implementation of the proposed tapped-inductor buck-boost architecture.

Conclusions

From the circuits presented, it can be seen that by leveraging a tap-to-ground tapped-inductor buck-boost architecture, a single-output or dual-polarity-output stepup/stepdown converter may be implemented with minimal complexity, low power-train component count and reduced overall size. With these benefits, the proposed architecture is not only a viable alternative but a higher power density realization than the typical solutions used today for such conversion needs.

As part of the buck-boost family of converters, the tap-to-ground tapped-inductor buck-boost architecture shares a similar transfer function and other electrical characteristics and behavior with other family members such as the inverting buck boost or the flyback architectures. However, when compared to those for the same conversion purposes (nonisolated, stepup/stepdown functionality with either a single output of the same polarity as the input or dual outputs of complementary polarities), the presented architecture is shown to provide additional advantages.

Compared to a flyback architecture used for generating dual complementary-polarity rails, the new architecture eliminates one of the transformer windings (the flyback primary) by magnetizing the inductor core directly through one of the "output" windings. This simplification reduces size, cost and the associated leakage inductance of the converter's magnetic element, along with its adverse effects.

When implemented with a properly chosen inductor and a highly integrated PWM controller, with a high switching frequency and small package for the given application, the presented architecture can deliver an extremely small solution size, effectively providing a very high-density buck-boost power converter alternative.

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About The Author

Hector F. Arroyo holds a BSEE degree with a major in Electronics and Communications from the Monterrey Institute of Technology (ITESM) in Mexico City. Hector joined National Semiconductor in 1997 and since then has held various positions in the applications, sales and technical marketing areas. Since 2005 he has been a senior field applications engineer and a staff field applications engineer in San Diego for local southern California markets as well as for Latin America on selected technologies such as LED lighting.

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