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Selecting A DSP Controller For Brushless Permanent Magnet Motor Drives

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The selection of a proper controller for a motor drive application is one of the critical decisions that determines the success or failure of a project. There are numerous criteria to consider when choosing a controller and this paper will enumerate most of them.

The main goal is to select the least-expensive controller that minimizes the overall cost of the system, while meeting system specifications. The optimum decision is one that reduces the list of controllers to a single choice by taking into account the overall product development cost, component pricing, availability, development tools, manufacturer's support, stability and sourcing considerations (for example, sole versus multisourced.)

In terms of electrical specifications, the foremost requirement is that the processor has enough bandwidth for the desired algorithm (i.e., trapezoidal, sinusoidal excitation, field oriented control, space vector modulation etc.) such that the motor can attain optimum performance.

This discussion focuses on the selection of a controller for applications employing brushless permanent magnet (PM) motors. To start, we briefly review the basic operating principles of a brushless PM motor. Next, we present an overview of motor control requirements associated with digital control—either one based on a microcontroller (MCU) or a digital signal processor (DSP) architecture. This leads us into a detailed discussion of controller selection criteria and the ability of MCUs and DSPs to meet these requirements.

Ultimately, we explain why DSP-based control is preferable to MCU-based control in brushless PM motor applications because of the special capabilities offered by digital signal controllers (DSCs). Distinct from general-purpose DSPs and other devices with a DSP core, DSCs represent a category of controllers that merge the characteristics of digital signal processors and microcontrollers to create a class of devices that are well suited for power supply and motor control. While some of the discussion about DSP architectures and cores relates generally to different types of DSP devices, the term DSP controller as it is used here generally refers to a DSC.

Brushless PM Motor Basics

A brushless permanent magnet (PM) motor is an electronically commutated motor with a permanent magnet rotor and a wound stator. It is a synchronous motor; the magnetic field generated by the stator and the rotor rotate at the same frequency. The knowledge of rotor position is important for efficient control. The rotor position can be detected by Hall sensors or rotary encoders attached to the motor. Rotor position can also be estimated by using back EMF information. This mode of feedback control eliminates the need for sensors and additional wires. Another option is the use of position or speed estimators to calculate rotor position.

A brushless permanent magnet motor can be driven by a rectangular or trapezoidal voltage in synchronization with the rotor position. The generated stator flux interacts with rotor flux, which produces torque. Sinusoidal and trapezoidal driving methods can be adopted. Brushless PM motors can be controlled either by scalar or vector-control techniques. These motors offer several advantages including linear control characteristics, high dynamic response, high efficiency, long operating life, noiseless operation, durability, higher speed ranges and higher torque-to-volume ratio.

Digital Control Of Brushless PM Motor Drives

In the past, brushless PM motor controls have been designed with analog circuitry. Today's competitive market demands higher performance and greater efficiency at a lower cost, so designers are switching to digital motor controls. As motor systems become more complex and place more demands on the processor, the performance of digital signal processor (DSP) or microcontroller (MCU) architectures allow cost-effective and energy-efficient design of digital motion control applications. DSPs provide real-time MIPS and tightly integrated peripherals to implement optimal control algorithms. Integrated high-speed ADC converters, high-resolution pulse-width modulators (PWMs) and sensor inputs on DSCs make them ideal for implementing brushless PM motor control.

Before selecting a DSC or an MCU, system requirements must be fully assessed. The capabilities of various processors should be evaluated in the light of these requirements.

Hardware Architecture

Most motor-drive applications require running the motor in a closed loop. Once the motor is running, the state of three Hall sensors changes based on the rotor position. Voltage on each of the three motor phases is switched based on the state of the sensors. Hall sensor transitions are counted to measure the motor speed (Fig. 1.)

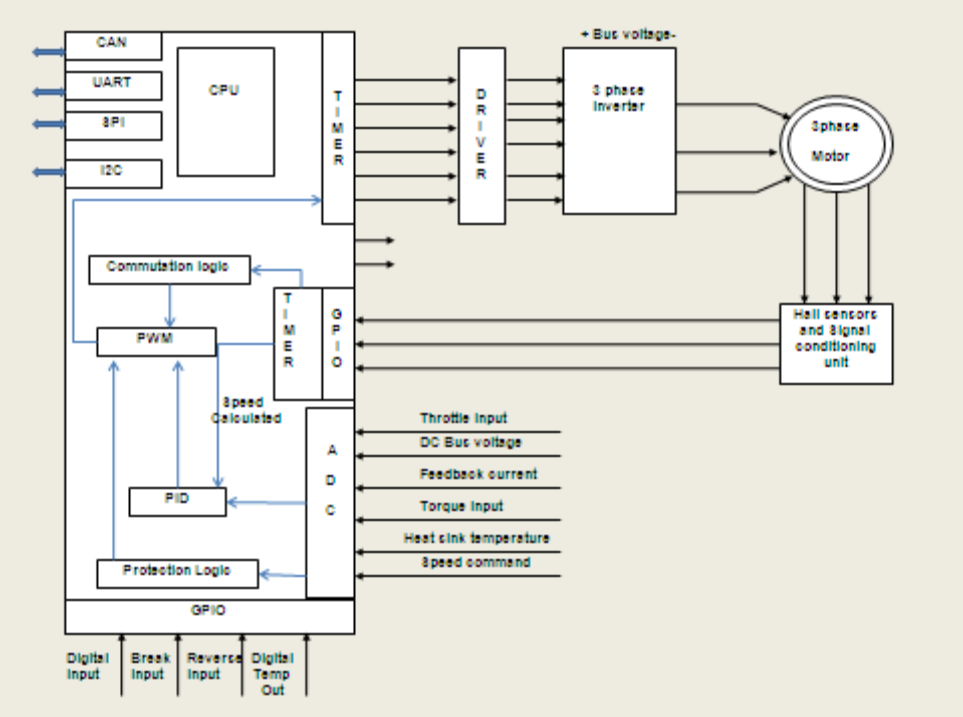

Fig. 1. A general block diagram of a brushless PM motor control.

As illustrated in Fig. 1, a brushless PM motor control block diagram consists of the following parts:

Bus Voltage. Dc bus voltage is supplied either through a battery bank or through a rectifier circuit.

Battery-pack technology requires managing the temperature of the individual cells and the low resistance of interconnecting conductors, connectors and switches. Cells have to work together effectively and safely to provide much higher capacities. The common requirement is the need for temperature management for high-power performance and operational life. Heat generated in the battery must be dissipated without damaging surrounding material.

Power Module / Inverter. The power module is developed by using switches with low on-state voltage drop and high switching frequency.

To turn on an n-channel MOSFET, the gate-source voltage must be greater than the inherent threshold voltage. The three-phase bridge consists of six switches connected in bridge fashion used to drive the three phases of the brushless PM motor. An independent or complementary mode of switching is adopted. PWM switching schemes to achieve maximum power output are high-side PWM, high- and low-side PWM, and all-channel PWM, which improves speed control and reduces the power losses in the system.

When there is an interaction between magnets and stator teeth, cogging torque is produced which is nothing but torque ripple. Torque ripple can also be created by imperfections in magnets, back EMF, inverter saturation, and unequal rise and fall time as the phases turn on and off. These torque-ripple issues have to be resolved through motor design and also by the control mechanism. Hence, using a fast speed loop with an adaptive current reference can reduce the ripple torque.

Driver. The gate drive-circuit forms the interface between the controller and the power switches. First, it buffers the gate signals generated by the controller. The controller can only source a maximum of 20 mA from each pin. However, the peak charging current required to turn on the power switches may be as high as 2 A. This is due to the high switching frequency used along with the inherent gate capacitance of the switches.

Generating a gate voltage for the low-side switch is straight forward, as it is ground referenced. But the high-side switch presents a problem. The gate control voltage, which goes from rail to rail, must be referenced to the switch source terminal, which in this case is not at ground. The second purpose of the gate-drive circuit is to generate the gate voltage required to activate the top-side switch adopting a bootstrapping technique. If the bus voltage is 36 V, and 12 V is required to turn the switch on, a gate voltage of 48 V would be needed to turn on the top switch.

Motor with Hall Sensors. Often, a motor is equipped with Hall sensors. A Hall-effect sensor is a transducer that varies its output voltage in response to changes in magnetic field. Typically, Hall sensor outputs with pull ups are directly interfaced to a DSP, which generates the necessary switching sequence as per commutation.

Digital Signal Processor. The processor needs to be powerful enough to implement math-intensive control algorithms as shown in equation 1. The DSP provides large-word-lengths support for required resolution and dynamic range, small interrupt latency and fast branch operations capabilities to facilitate quick response to expected and unexpected events. A high-MIPS CPU is required to increase the range of sampling frequency and to integrate the application-specific peripherals with the processor such as timers, A-D converters, PWM generators and communication interfaces (see Fig. 2), hence CPU overhead and total system costs are reduced when a DSP is used.

$$y(t) = \sum_{m=0}^{M} a(m)y(t-m) + \sum_{n=0}^{N} b(n)x(t-n) \qquad (1)$$

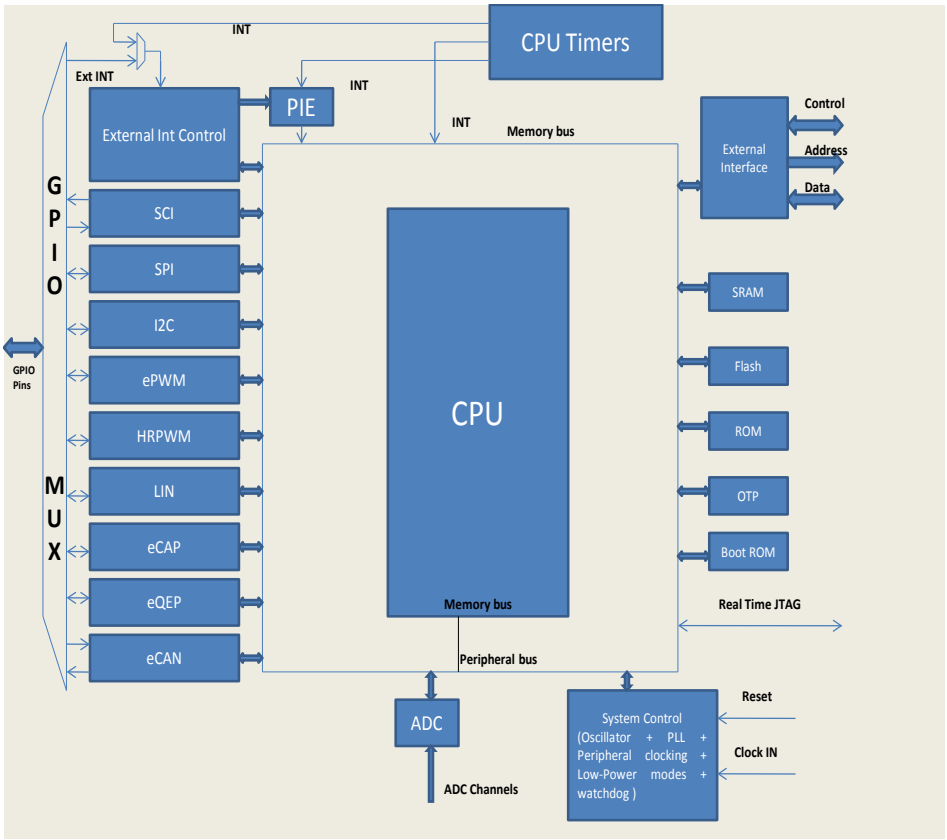

Fig. 2. Functional block diagram of processor.

Bus voltage, feedback current, back EMF, throttle, controller temperature, winding temperature, and brake voltage are all needs to be monitored through the ADC of the controller. Hall signals need to be fed to the capture module. Encoder signals are fed to the quadrature encoder module. Logic inputs/outputs are fed to the GPIOs.

The speed of a motor depends on the amplitude of the applied voltage, which is adjusted by the PWM technique. The required speed is controlled by a PID speed controller. The difference between the actual and the required speed is input to the PID controller, and based on this difference, the controller determines the duty cycle of the PWM pulses. These comparisons of speed signals and the generation of error signals in the control loop must be performed quickly. Hence, the performance of the control loop is dependent on the ADC. Allowing some settling time for the ADC channels, signal reading is affected by the conversion time, resolution and bandwidth of the ADC channels.

All analog inputs need to be verified after power up, while in standby and before entering drive operation. In a PWM cycle, how fast we correct the phase current depends on the sampling speed as it has an effect on the compensation and stability of the control system. When there is a change in the sampling frequency, the values of PID control change. PWM resolution has to be equal to or greater than the resolution of the power supply as the PWM filter will smooth out the generated waveform and reduce its amplitude. If the PWM pulse is wider, more time is required to integrate to reach a stable filter voltage. If the resolution is low, the signal which is reconstructed from samples will be different from the original signal.

Another requirement is that different power-down modes must be available when the DSP is not performing operations. These include sleep mode, idle mode, and wake up mode to restore operation. Also, there must be different reset options like brown out reset and others to avoid infinite loops executing unnecessarily.

Controller Selection

The main objective of this article is to select a controller for a brushless PM motor control. We'll consider both MCU and DSP options here for the controller to determine the suitability of each for this application.

Starting with the MCU, as the first step in controller selection, the designer needs to estimate program size, data size and execution time requirements. Time constraints and task deadlines need to be kept in mind while choosing a processor as these factors will have a direct influence on cost and design performance.

Comparison Of Controllers: Architecture, Memory Size And Speed

Architecture. Although traditional microcontrollers include the necessary peripherals to provide solutions for digital control applications, they lack both the performance and architecture needed to perform real-time, math-intensive, advanced control algorithms at the desired bandwidth. In contrast, DSPs are built with the Harvard architecture. This configuration employs separate program and data memories, associated data and address buses. The benefit of this arrangement is increased speed, because instructions and data can move in parallel instead of sequentially.

DSPs include a powerful pipelining feature to operate on several instructions simultaneously. In DSPs, most instructions execute in one machine cycle because all functions are performed internally in hard-wired logic. The accumulator handles overflow by saturating to the most positive or least negative value, thus eliminating rolling over. They support a large word length, thus reducing the quantization error. In addition, hardware shifters allow scaling of data used in computations. This helps prevent overflows, and keep the required precision. Such shifters allow shifting to take place simultaneously with other operations and without additional execution time.

Special single-instruction, multiple-data (SIMD) operations can be done using DSPs. Some DSPs use very long instruction word (VLIW) techniques so each instruction drives multiple arithmetic units in parallel. Special arithmetic operations, such as fast multiply–accumulates (MACs) are the major feature of DSPs. Many fundamental DSP algorithms, such as FIR filters or the fast Fourier transform (FFT) depend heavily on multiply–accumulate performance. Bit-reversed addressing, a special addressing mode in DSPs, is useful for calculating FFTs.

Special loop controls, such as architectural support for executing a few instruction words in a very tight loop without overhead for instruction fetches or exit testing are available. There are no memory management units. DSPs frequently use multi-tasking operating systems, but have no support for virtual memory or memory protection. Operating systems that use virtual memory require more time for context switching among processes, which increases latency. The special DSP instructions supplement the computational speed of DSPs and make them ideal for high-performance real-time applications. Many DSP chips include input/output (I/O) functionality, timing circuitry, direct memory access (DMA) controllers, and high-speed memories on chip.

Memory Size. Brushless PM motor control requires a minimum of 64 KB of flash program memory and up to 16 KB of RAM data memory for implementing scalar or vector algorithms. As an example, consider Texas Instruments' TMS320F28035 DSC, which provides 64K×16 on-chip flash memory segregated into eight 8K×16

sectors, single 1K×16 OTP memory. The user can individually erase, program and validate a flash sector while leaving other sectors untouched. The 'F28035 provides special memory pipelining to enable its flash module to achieve higher performance. This controller's flash or OTP can be mapped to both program and data space.

This DSC also contains up to 8K×16 of single-access RAM, which can be mapped to both program and data space. In addition, 8K×16 size boot ROM is factory programmed with boot-loading software. For sensorless closed-loop control of a brushless PM motor, 7.62 kbytes of ROM and 324 bytes of RAM are required. For sensor closed-loop control, these requirements change to 7.46 kbytes of ROM and 328 bytes of RAM. In both cases, the use of an 8-bit MCU with the DSC is assumed.

Speed. Today's DSPs are typically run at an internal clock rate of 1 GHz, while transmit and receive signals to and from external devices operate at rates higher than 200 MHz. These fast-switching signals generate a considerable amount of noise and radiation, which degrades system performance and creates electromagnetic interference problems.

The speed of the processor depends heavily on the RAM size, operating frequency, and architecture. A speed of 32 to 60 MIPS is preferred for implementation of advanced algorithms for motor control application with the exact speed depending mainly on the control strategy being employed. With an increase in operating frequency, the cycle time required to correct the phase current in the windings of a motor may be reduced, which demands an improvement in the resolution and conversion time of the ADC and controller block.

Core Size And Operating Voltage

Core Size. The core sizes available in the market for motor-control applications are 8-bit, 16-bit, and 32-bit. With the 8-bit controller, programming complexity may increase. Though 8-bit processors were the universal computing engine found in smart products, most fixed-point DSP processors employ a 16-bit data word as it is sufficient for many DSP applications. A few fixed-point DSP processors use a 32-bit data word to enable better accuracy, ease of programming and complex algorithm implementations in motor applications.

Operating Voltage. New generations of motor-control DSCs have lowered their operating voltages from 5 V to 3.3 V to offer higher performance. Replacing traditional 5-V digital control circuitry with 3.3-V designs introduces no additional system cost and no significant complication in interfacing with TTL and CMOS compatible components as well as with mixed-voltage ICs. However, good engineering practice needs to be exercised to minimize noise and EMI effects by proper component layout and PCB design in a motor control using a mixed-signal environment with high- and low-voltage analog and switching signals.

Cycle Time, Lead Time And Manufacturability

Lead time is the time period required for delivery of a product after the product has been ordered. Cycle time is a more mechanical measure of process capability, which measures the period from start of the process to its delivery. To begin, the time lag between the occurrence of the order and the actual process needs to be minimal. The design methodology called design for manufacturability includes a set of design rules for integrated circuits, in order to improve their functional, parametric yield, or their reliability.

The processor must be feasible to manufacture and must lie in the normal distribution region, which can have 68% of tolerance in the range $\pm\sigma$. The process capability ratio must be equal to zero to be under normal distribution region considering statistics ideally. Process capability is given by

$$C_p = \left(\frac{upper\ Spec - lower\ Spec}{6\sigma}\right) \tag{2}$$

where σ is a standard deviation of tolerance, which helps in the evaluation of manufacturability. Process capability index is given by

$$C_{pk} = \min\left[\frac{X - lower\ Spec}{3\sigma}, \frac{upper\ Spec - X}{3\sigma}\right] \tag{3}$$

where X in (3) represents the mean. We should avoid process stack up, which leads to extra cost and drift in the curve to the left with respect to mean deviation. Thus all mechanical and electrical variables have to be normally distributed. Fig. 3 gives the probability distribution of products in manufacturing. Though each product

in a system meets tolerance criteria, the curve shifts from the nominal distribution when considering the system performance as a whole with statistics.

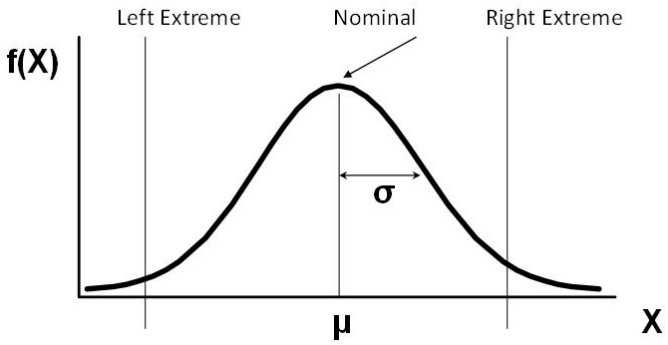

Fig. 3. Nominal distribution statistic.

The process stack up can be avoided by considering tolerances while designing with the help of Monte-Carlo or parametric sweep analysis, which would greatly help in manufacturing to maintain the quality too.

Packaging And Pin Count

Both technical and commercial requirements must be considered in the selection of appropriate package configurations keeping in mind chip assembly and device application. It's important to consider that the DSP's physical design should support and protect the semiconductor chip, accommodate the appropriate number of I/O pins and satisfy space, weight and interconnection restrictions imposed by higher-level packages. A thermal design evaluation should be done to check that the package can withstand temperature cycles during chip assembly. In electrical design, we have to consider the impact of the interconnect path between the chip and board package on transmission of power and signals through it.

The pin count is another factor in package selection. Pin-count proliferation leads to undesirable package expansion and reduction in current density that is number of bits/gates per unit area. The different types of packaging available are single inline package (SIP), dual inline package (DIP), pin grid array (PGA), zigzag inline package (ZIP), quad flat package (QFP) and flat package. For high-density packaging we go for PGA but due to interconnect routing problems they are used in surface mount. The quad flat package, which has pins on all four sides, is also commonly used for DSPs.

Thus keeping all the issues mentioned above we should choose the right package type with the lowest number of pins necessary. Lower pin counts not only enhance current density, as described above, they also help to control device cost. As the pin count increases, the size and cost increases. Hence, in general, processors with smaller size and pin counts have to be chosen without compromising on the device's functionality.

System Cost Considerations

The overall cost of the system includes engineering research and development, manufacturing parts and labor, warranty repairs, updates, and field service. New generations of equipment must have higher performance such as better efficiency and reduced EMI. System flexibility must be high to facilitate market modifications and reduce development time. All these improvements must be achieved while at the same time decreasing system cost.

A single-chip solution combines a fixed-point DSP core with MCU peripherals to be able to perform sophisticated control schemes as well as algorithms. The improvement in the performance of DSPs enables high-resolution control and minimizes control-loop delays such that motor designs are optimized leading to a reduction in system cost and better reliability. Considering all these parameters, selecting a DSP controller with a cost of less than $7 would suffice for a brushless PM motor application.

Peripherals And Connectivity

The peripherals on the DSP controller make virtually any digital control requirements possible. Communication peripherals make possible the communication with external peripherals to increase the safety and reliability of systems. Intelligent peripherals on board include timers, PWM generators, ADC, general-purpose bi-directional

digital I/O pins, capture inputs, compare registers, dead-band logic, test and program interface, low-voltage detection unit and watchdog timers, and high-speed serial communications peripherals like CAN, SPI, I^2C and UART/LIN.

GPIO. These pins should support easy interaction with various peripherals like LEDs, buzzer, LCD display and other peripherals. They should also support push-pull and open-drain inputs and outputs. They must be fast to interact with peripherals with an interface speed of about 400 kHz. They should also come with smaller size, predictable latency, easier routing, and low power consumption. Their port bits must be able to configure individually, optionally for slope control to reduce EMI noise and must be fast enough to transmit the feedback signals that are given to ADC.

ADC. The most-significant factor to be considered in selecting an appropriate controller is its on-chip ADC's ability to measure different samples simultaneously. This allows the measurement of motor voltages and currents to occur in-phase to avoid errors in the control loop. The analog signals are to be passed through the sample-and-hold circuit before it is sent to the ADC for conversion. By this, sampling errors are introduced. After the conversion into digital signals, quantization errors are introduced due to noise.

The sampling of a signal is to be performed with twice the highest frequency component of that signal, obeying the Nyquist criteria. To avoid aliasing of the signals, multi-rate sampling has to be performed. By using a low-pass digital filter, noise can be removed. As the digital filters can avoid the ripples in the pass-band and have smooth transition and accuracy, we go for digital filters rather than analog filters.

The required accuracy or precision of the system is based on the number of bits required for an ADC. It is important to always design a system to allow for more bits than initially required. For example, if an application calls for 10 bits of accuracy, choose a 12-bit converter. The achievable accuracy of a converter will always be less than the total number of bits available.

A high-speed analog-to-digital conversion rate is beneficial for many reasons. First, it minimizes sample latency, which increases closed-loop performance. Secondly, high-speed conversion allows sampling of multiple channels with high throughput for all channels. Additionally, a high-speed conversion rate coupled with the DSP capabilities allows oversampling and filtering of noisy motor-feedback signals.

Consider a 10-bit ADC with a 5-V supply used for the motor control having a peak current of 25 A. We can get 1024 discrete levels. Therefore, the resolution of the ADC will be 5/1024 = 4.8 mV. When this value is amplified by a gain of 20, we get 0.24 mV. To sense the current obtained placing a 1-mΩ resistor, one count of the ADC is equal to 0.24 A. (2.5V offset) and with a 12-bit ADC having 3.3-V supply, one count of the ADC is equal to 0.04 A. Hence, the resolution increased by 16%. Thus, the error in the 12-bit ADC is less than the 10-bit ADC. The maximum steady-state error due to quantization is inversely related to the resolution of the ADC. An improvement in resolution of just 2 bits will result in up to a four times decrease in steady-state error. As the controlling becomes fast, we can get converted values faster and hence settling time of the signals are faster.

Timers. Timer hardware is a crucial component of most embedded systems. The timer should have automatic reload capability, which will have a latch register to hold the count written by the processor, which is generally supported by software. The accuracy of the clock generation must be high. They must have the capability to interact with other GPIO pins and support other peripherals in a processor.

The considerations to be made when configuring the timer module for PWM are its frequency and duty cycle. According to the required PWM frequency, bus clock frequency and timer prescaler must be set, which depends upon the degree of resolution of the PWM signal. The maximum and minimum resolution of the PWM signals are limited by the timer clock frequencies. These calculations are given by the following equations:

$$\text{Target Time Prescaler value} = \frac{\text{Bus clock frequency}}{\text{Timer clock frequency}} \tag{4}$$

$$\text{PWM period} = \frac{\text{Bus clock frequency}}{\text{Timer prescaler} \times \text{PWM frequency}} \tag{5}$$

$$\text{PWM mark time} = \frac{\text{PWM period}}{100} \times \text{Duty cycle} \tag{6}$$

PWM space time available= PWM period- PWM mark time (7)

The DSP must be able to service the timer PWM interrupts in time for the next edge to be configured. This sets an upper limit on the frequency or resolution of the PWM signal that can be reproduced, and will vary from system to system depending on DSP application.

Watchdog Timer. For the processor to be self reliant we need a watch-dog timer (WDT). A watchdog timer can get a system out of a lot dangerous situations. However, if it is to be effective, resetting the watchdog timer must be considered within the overall software design. When multitasking kernels are used, deadlocks can occur.

For example, a group of tasks might get stuck waiting on each other and some external signal that one of them needs, leaving the whole set of tasks hung indefinitely. If such faults are transient, the system may function perfectly for some length of time after each watchdog-induced reset. However, failed hardware could lead to a system that constantly resets. For this reason, it may be wise to count the number of watchdog-induced resets, and give up trying after some fixed number of failures.

Communications Peripherals. The *CAN bus* is used in the motor industry to reduce the amount of wiring. By using a single data wire to link electronic devices together, savings in cable cost and weight are achieved. A master bus network of CAN bus technology uses a single “plug-and-play” connection that seamlessly links every device of the system abroad. With its ability to exchange high-speed data between equipment such as battery charges, inverters and digital switches, a CAN bus system is considered self contained.

A system can access many nodes at a time through the CAN bus, since it supports multiple master/slave nodes. The transfer bit rate can be up to 1 Mbits/s, with selectable clock source. The CAN protocol supports two message-frame formats, the only essential difference being in the length of the identifier. The “CAN base frame” supports a length of 11 bits for the identifier, while the “CAN extended frame” supports a length of 29 bits for the identifier. Cyclic code redundancy check, frame check and ACK errors are the mechanisms for error detection at message level. Meanwhile, monitoring and bit stuffing are the mechanisms for error detection at bit level. CAN BUS technology is internationally accepted in the automobile industry.

The *Serial Peripheral Interface (SPI)* is a fast synchronous serial interface that allows a serial bit stream of programmed length to be shifted into and out of the device at a programmable bit transfer rate**.** The SPI bus is implemented using separate clock, transmit and receive data lines such that each communicating device can simultaneously send and receive data over the SPI link.

Three-wire SPIs found on most DSP controllers are a popular means for transmitting and receiving data. The SPI is normally used for communications between the DSP controller and external peripherals or another controller. Typical applications include external I/O or peripheral expansion via devices such as shift registers, display drivers, and ADCs. Multi-device communications are supported by the master/slave operation of the SPI. They have a communication speed of 10 MHz with CRC for reliability and a provision to avoid data contention on data lines.

The *I^2C bus* is used in a wide range of applications because it is simple and quick to use. It consists of a two-wire communication bus that supports bidirectional data transfer between a master and several slaves. The master or processor controls the bus in particular, the serial clock (SCL) line. Data is transferred between the master and slave through a serial data (SDA) line. This data can be transferred in three speeds or modes: standard (0 to 100 kbits/s), fast (0 to 400 kbits/s) and high-speed (0 to 3.4 Mbits/s). The most common speeds are the standard and fast modes. I^2C can also be used for data storage in external EEPROM.

The *UART* is used for asynchronous communication. Transmitting and receiving must be set for the same bit speed, character length, parity, and stop bits for proper operation. The UART usually does not directly generate or receive the external signals used between different items of equipment. Separate interface devices are used to convert the logic-level signals of the UART to and from the external signaling levels. Examples of standards for voltage signaling are RS-232, RS-422 and RS-485. Multi-processor communications is also possible.

Generally, the connectivity between the processor and the computer is done with a *JTAG interface*. This is used to access on-chip debug modules inside the target CPU, which is done with a JTAG adapter. It must be able to store the program and must be fast enough to access the variables and constants of the program and must support its variations during run time. Though there are different interfacing devices available for different processors like SWIM, the interfacing between the processor and the PC functionality remains the same.

PID Controller

Closed-loop speed regulation is done using digital proportional, proportional integral or proportional integral derivative (PID) control. When the motor is running, the measured speed is subtracted from the reference speed and the resulting error signal is processed by the PID controller to generate the amplitude of a sinusoidal or trapezoidal wave. The reference speed is set by an external potentiometer, while the measured speed is derived from the Hall sensors.

The PID controller implementation takes advantage of the MAC instruction of the DSP for fast execution. Closed-loop control systems must act very quickly to implement the error correction without delay, before the system has time to change to a different state. Otherwise, the system will possibly become unstable.

The Nyquist stability criterion is used to predict whether or not a system is unstable from a knowledge of the loop gain and the loop delay as follows. If the loop gain is unity or greater at the frequency of an input sinusoid where the time delay in the system is equal to half of a cycle period, the system will be unstable.

The performance of a digital system depends on the sampling time. Larger sampling times usually give rise to higher overshoots in step response, and eventually may cause instability if the sampling time is too large. Thus, to make the controller stable, the proportionality constant values have to be increased. If we increase the sampling frequency (i.e., performing multi-rate sampling) we can reduce the values of proportionality constants to maintain the stability. Hence the poles are brought inside the unit circle in the Z-plane.

It is possible to improve controller performance simply through tuning, but doing so usually involves certain trade-offs. It is generally accepted that modifying gain parameters in a PID control system produces the effects shown in Table 1.

Table 1. Effect of increases in PID gain parameters on system performance.

	Rise time	**Settling time**	**Overshoot**	**Steady state error**
Increase K_p	Decreases	Not affected much	Increases	Decreases
Increase K_i	Decreases	Increases	Increases	Decreases
Increase K_d	Not affected much	Decreases	Decreases	Not affected much

As you can see, an improvement in one area often means a compromise in another. For example, increasing the proportional gain will improve settling time but will have an adverse effect on the amount of overshoot. If, on the other hand, we address the I/O capabilities of the system, it is possible to achieve performance improvements in all aspects, as Table 2 indicates.

Table 2. Effect of I/O capabilities on system performance.

	Rise time	**Settling time**	**Overshoot**	**Steady state error**
ADC resolution	Not affected much	Decreases	Not affected much	Decreases
Signal conditioning	Decreases	Decreases	Decreases	Decreases

Calibration	Not affected much	Decreases	Not affected much	Decreases

Electrical And Mechanical Characteristics

Electrical Characteristics. The package is a complex electrical environment and the characterization of this environment is a multi-faceted task that consists of models constructed from both theoretical calculations and experimental measurements. In simple terms, a package electrical model translates the physical properties of a package into electrical characteristics that are usually combined into a circuit representation. The typical electrical circuit characteristics that are reported are the dc resistance (R), inductance (L), capacitance (C), and characteristic impedance (Z_o) of various structures in the package. The processor built must be tested with its equivalent circuit and analyzed to verify it meets all the electric specifications that give long life and lower power consumption.

Mechanical Characteristics. When the device is powered up, its temperature rises, and when it is shut down, its temperature drops. The magnitude of the maximum temperature on the die surface depends on the thermal solution employed, and is usually between 80°C and 125°C. In addition to the power-on and power-off cycles (maxi-cycles), the processor is cycled between different intermediate temperature values depending upon processor usage (mini-cycles) in any application program.

The dynamic response of a package can introduce high-frequency cyclic stresses in some components of the package leading to the possibility of high cycle fatigue. Repeated flexure of a structure within the package will put the copper lines and solder joints through a fully traversed stress cycle. The ability of a package to survive these stress-inducing environments is governed by the properties of the materials used in its construction, as well as by its design. Since the processors are mounted on the PCB, which will typically be embedded within the brushless PM motors, it must be able to withstand all the disturbances.

Development Tools And Computing Capabilities For Implementation Of Algorithms

Development Tools. A software development tool is a program that software developers use to create, debug, maintain, and support other programs and applications. Development tools provide an easy and economical way to evaluate motor-control applications. Development boards and advanced developmental tools demonstrate the capabilities of motor-control silicon solutions. These tools work for program and debug application software.

In addition, emulators that aid the development of embedded systems are available for popular programmable controllers. They replace the controller chip in the system being developed and emulate the controller's functionality in real time. They allow the user to view internal registers and memory, set breakpoints, disassemble code, watch interrupt handling, and look at port inputs and outputs.

A motor-control development board features a three-phase inverter bridge, Hall sensors or quadrature encoder interface for sensored motor control and phase voltage feedback for sensorless brushless PM operation. The board will also offer a dc bus current-sense resistor for single-shunt vector control, a phase current-sense resistor for dual-shunt vector control, overcurrent protection, input or output control switches, potentiometer, and LED indicator for PWM outputs. Also, CAN, I^2C, SPI, and UART communications ports are typically included.

Computation Capability. A digital signal processor (DSP) core brings significant performance enhancement as a result of its instruction set architecture (ISA) and it incorporates support for fixed/floating-point computations in the same processing core. A DSP controller or DSC has the best features of digital signal processing, reduced instruction set computing (RISC), and microcontroller architectures, firmware, and tool sets. The CPU features include a modified Harvard architecture and circular addressing. The RISC features are single-cycle instruction execution, register-to-register operations, and a modified Harvard architecture.

The microcontroller features also include ease of use through an intuitive instruction set, byte packing and unpacking, and bit manipulation. The modified Harvard architecture of the CPU enables instruction and data fetches to be performed in parallel. The CPU can read instructions and data while it writes data simultaneously to maintain the single-cycle instruction operation across the pipeline. The CPU does this over separate address/data buses.

Control algorithms used for the speed control have been implemented by assembly or embedded C/C++ language programming in the controller. According to the input command, the feedback and the control

algorithm, the PWM pulses for each phase are generated by the controller and are fed to the MOSFET/IGBT driver.

The speed with which a DSP executes operations in an application is a critical consideration. Designers should implement the DSP format that will process algorithms with the greatest efficiency. DSPs resemble reduced instruction set computers (RISC), in that a small set of frequently used instructions are optimized for numerical processing at the expense of less frequently used general-purpose operations. DSP instruction sets efficiently handle mathematical operations common to many algorithms that are repeatedly executed in time-critical loops. For example, digital filters, which are often used in signal processing and control applications, are implemented using recursive difference equations of the form

$$y(n) = \sum_{i=0}^{N} a(i)x(n-i) + \sum_{j=1}^{M} b(j)y(n-j)$$

where y(n) is the output, y(n - j) are the past outputs, x(n) is the present input, x(n - i) are past inputs, and a(i), b(j) are weighing factors.

This equation basically says that any output y(n) can be computed as a weighted sum of the input at the present time n, past inputs x(n - i), and past outputs y(n -j). Each step in this computation involves a multiplication and addition. The multiply and accumulate (MAC) instruction in DSPs performs this in a single instruction cycle. In contrast, in a typical fixed-point microprocessor, a multiply and add typically executes in 15 to 20 machine cycles.

The MAC instruction is also highly effective in matrix multiplication and fast Fourier transform (FFT) algorithms. MAC is the one instruction that most distinguishes DSPs from microcontrollers. DSPs also significantly increase execution speed by performing multiple operations in parallel. For instance, in the same instruction cycle that a MAC operation is being performed, a parallel data move can be carried out. Thus, the special DSP instructions supplement the computational speed of DSPs and make them ideal for high-performance real-time applications.

Reasons For Selecting A DSC

The speed of execution of a brushless PM motor system implementing scalar control using an 8-bit microcontroller is low as is it runs at 20 to 30 MIPS. Since look up tables are being used for complex calculations, commutation cannot be done at run time. The system is also unable to go to a higher switching frequency as current correction would be a difficult task with the shorter PWM cycle time.

Current waveshaping is an important criterion for better power, which would not be promising with lower resolution and fewer levels of look-up table. Obtaining the true resolution and bandwidth of ADCs with an 8-bit controller is not feasible. The resulting lower sampling rate has an effect on the compensation and stability of the control system.

Other limitations of 8-bit microcontrollers include their lack of a scan-mode ADC, fewer complementary PWM channels, greater programming complexity as it is 8-bit length, low code-size capacity, and longer control-loop execution times. Another shortcoming is that additional functionalities cannot be imported and designers cannot implement complex algorithms like field oriented control with space vector modulation. Other possible problems are the system's inefficiency in delivering torque and hence power and inaccurate signal reading and correction in a PWM cycle.

All these drawbacks can be eliminated using a digital signal processor, particularly the type known as a digital signal controller or DSC. A DSC (also referred to here as a DSP controller) is chosen on the basis it provides an optimal solution for brushless PM motor drives requiring high speed in the range of 40 to 80 MHz , high-resolution control-loop capabilities, single-cycle multiply accumulate units, barrel shifters, large accumulators , fast interrupt responses and peripherals like flexible high-resolution PWMs, high-performance ADC, advanced capture and quadrature encoder interfaces, CAN, SPI, SCI, I2C, Timers and WDT.

DSCs offer independent register set, memory bus structure and processing unit, low interrupt-response time, execution of algorithms in parallel with the C28x CPU, a floating point (32-bit) format that removes scaling and saturation burden, and assembly and C-callable libraries. Based on a DSP architecture, the core is optimized to quickly execute math-based operations, but can also handily process general-purpose code.

DSCs are fine tuned for real-time control. These specialized DSP controllers are being marketed as green technologies for their potential to reduce power consumption in electric motors combing the processing power of a DSP and the functionalities of an MCU with a flexible set of peripherals to create a cost-effective solution.

In order of market share, the top three DSC vendors are Texas Instruments, Freescale Semiconductor, and Microchip Technology, according to market research firm Forward Concepts. These three companies dominate the DSC market, with other vendors such as Infineon Technologies and Renesas Electronics taking a smaller slice of the pie. Referring to Table 3 for comparison of microcontroller and DSCs, we recommend the TI DSC for brushless PM motor applications as it gives optimal design with low cost and good performance.

Table 3. Comparison of DSCs suitable for motor control drive.

	STM8S208MB	***TMS320F28035***	***MC56F8335MFGE-ND***	***DSPIC30F6015***	***XE167GM***
Manufacturer	STMicroelectronics	Texas Instruments	Freescale Semiconductor	Microchip Technology	Infineon Technologies
Core Processor	STM8	C28x	56800E	dsPIC	C166SV2
Core Size	8 bit	32 bit	16 bit	16 bit	16 bit
Series	STM8S	TMS320F2803x	56F8xxx	dsPIC 30F	XE167xM
Speed	24 MHz	60 MHz	60 MHz	30MIPs	80MHz
Connectivity	CAN, I²C, IrDA, LIN, SPI, UART/USART	SCI, SPI,UART, CAN,LIN,I2C	CAN, EBI/EMI, SCI, SPI	CAN, I²C, SPI, UART/USART	CAN, EBI/EMI, I²C, LIN, SPI, SSC, UART/USART, USI
Peripherals	Brown out detect/reset, POR, PWM, WDT	Brown-out Detect/Reset, POR,PWM, WDT	POR, PWM, Temp Sensor, WDT	Brown-out Detect/Reset, LVD, Motor Control PWM, QEI, POR, PWM, WDT	I²C, POR, PWM, WDT
PWM outputs	12	15	12	10	8
Number of I/O	52	45	49	52	119
Pin count	80	80	128	64	144
Program memory size	128KB (128K x 8)	128KB (64K x16)	72KB (36K x 16)	144KB (48K x 24)	384KB (384K x 8)
RAM Size	6K x 8	10K x 16	6K x 16	8K x 8	34K x 8
Supply voltage	2.95V ~ 5.5V	1.71 V ~ 1.995 V	2.25 V ~ 3.6 V	2.5 V ~ 5.5 V	3 V ~ 5.5 V
Analog to digital converters	A/D 16 x 10b	A/D 16x12b	A/D 16x12b	A/D 16x10b	A/D 16x10b

Operating temperature	-40ºC ~ 85ºC	-40°C ~ 105°C	-40°C ~ 125°C	-40°C ~ 85°C	-40°C ~ 85°C
Package	80-LQFP	80-LQFP	128-LQFP	64-TQFP	144-LQFP
Packaging	Tray	Tray	Tray	Tape & Reel (TR)	Tape & Reel (TR)
Unit Price	$5.9	$9.095	$10.45	$12.64	$7.68

Migration And Future Developments

Common architecture and common on-chip peripherals of processor cores allow designers to migrate from one processor core to another per the application requirement and for design optimization. The DSC has the flexibility to scale up or scale down the design provided that members of a DSC family offer code and pin compatibility while meeting electrical specifications too. In addition, in selecting a DSC, designers should note that it must support future improvements in which functionality may be added to an existing system.

Conclusion

Computational speed, processing capability, memory, and interface, ease of programming, real-time concerns and cost are the parameters to be kept in mind while choosing a DSC for motor applications. DSCs play a significant role in improving efficiency, reliability and these controllers provide a speed of 20 to 150 MIPS. Motor control implementing complex algorithms typically requires 40 to 80 MIPS speed. Hence, use of DSCs can reduce the size and cost of the overall system.

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