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More Boost With Less Stress: The SEPIC-Multiplied Boost Converter

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This article introduces a novel and tested topology for boost converters with moderately high boost ratios in the range of 10:1 to 50:1. This topology, which I call the SEPIC-multiplied boost, is suitable for applications with voltages ranging from as low as about 1.8 V on the input, up to perhaps 500 V on the output. This new topology overcomes many of the disadvantages presented by other methods.

First, it significantly reduces the voltage stress on the main and rectifier switches without any accompanying significant increase in current stress. This widens and improves the choices in MOSFETs and Schottky rectifiers, where high voltage is often a problem. The new topology also operates with moderate (as opposed to very high) PWM duty cycles, which allows continuous-conduction mode (CCM) operation and makes feedback loop compensation easier.

Another benefit of the SEPIC-multiplied boost is its higher efficiency, which is attributed to its moderate duty cycles, use of lower-voltage MOSFETs and rectifiers, and reduced switching losses from lower ac voltage amplitude. Finally, the topology offers quieter operation. There is reduced noise due to reduced energy in the switch-node capacitance. Also, high-frequency emissions may be reduced because the presence of multiple inductor-energy discharge paths seems to dampen high-frequency ringing.

This article describes the origins and operation of the SEPIC-multiplied boost converter. In doing so, it also compares this topology with other boost topologies for obtaining high boost ratios. Test results for an actual design example are presented and the article adds information about design variations and component considerations (see Note 1.)

Existing Boost Topologies

There are several dc-dc converter topologies for obtaining relatively high (over 10:1) boost ratios. These include:

- simple boost
- charge-pump-multiplied boost and
- tapped-inductor boost

The simple boost has the simplest schematic design with the lowest parts count (Fig 1.) It also offers very high efficiency when used with low boost ratios. However, there are several limitations to the simple boost. For example, high boost ratios impose both high-voltage and high-current stress on Q1. The MOSFET must be rated for full output voltage and relatively high current (translating to low RDS(on).) This results in a large MOSFET die, which tends to be expensive and requires a strong gate driver. Furthermore, switching losses are likely to be high due to large voltage transitions on the large die transistor.

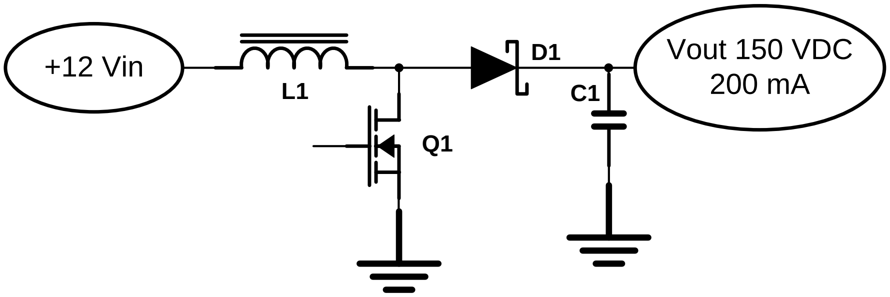


Fig. 1 Simple boost topology.

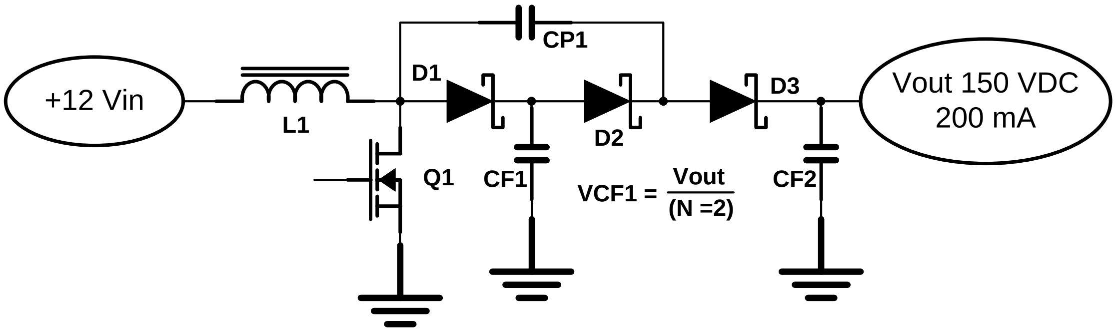
Another drawback of the simple boost topology is that high voltage on the rectifier may preclude the use of common Schottky diodes, so a lossier ultrafast type may be needed. Additionally, large boost ratios require high duty cycle. High duty cycles and ultrafast diodes can both lead to discontinuous conduction mode (DCM), which usually increases conduction loss (Table 1.)

Table 1. Equations and example values for key parameters of a simple boost converter.

Parameter	Equation	Numerical value for design example (12 V in to 150 V out at 200 mA)	Comment
Voltage CF1	N/A	N/A	No such node in this topology.
CCM duty cycle, D	$D = \frac{Vout-Vin}{Vout}$	92%	
Q1 peak volts	**Q1 Vpk = Vout**	150 V	
Q1 amps RMS (large L)	$I_{rms} \sim \frac{\sqrt{D} * Iout}{(1-D)}$	2.6 A	Approximation is very close for low inductor ripple.
D1 peak volts	**D1 Vpk = Vout**	150 V	

Charge pump multipliers are an economical choice for high output voltage and low output current (Fig. 2.) They provide high boost ratios with improved duty cycle and reduced voltage stress on the rectifiers and main switch.

But as was the case with the simple boost, this topology has limitations. Each charge-pump-multiplier stage requires two added series diodes, which contribute to loss from forward voltage drop. In addition, the pump capacitors need to be large so as to avoid a differentiated current waveform with significant cyclic droop. This differentiated current waveform increases RMS switch current and can corrupt current-mode-control waveforms. For these reasons, charge-pump multipliers are best confined to applications where output current does not exceed 50 to 100 mA (Table 2.)



$$D = \frac{VCF1-Vin}{VCF1} \qquad Q1\ Vpk = VCF1 \qquad Dn\ Vpk = VCF1$$

Fig. 2. Charge-pump-multiplied boost topology. This example uses N=2 stages.

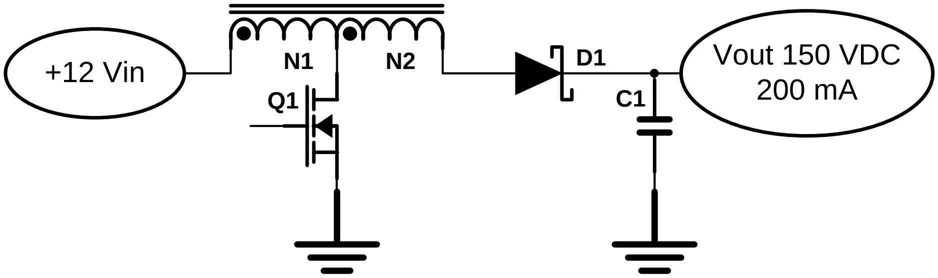
Table 2. Equations and example values for key parameters of a charge-pump-multiplied boost converter.

Parameter	Equation	Numerical value for design example (12 V in to 150 V out at 200 mA)	Comment
Voltage at CF1	$VCF1 = \frac{Vout}{(N=2)}$	75 V	
CCM duty cycle, D	$D = \frac{VCF1-Vin}{VCF1}$	84%	
Q1 peak volts	**Q1 Vpk = VCF1**	75 V	
Q1 amps RMS (assuming large L1 and CP1)	$I_{rms} \sim \frac{\sqrt{D} * N * Iout}{(1-D)} + \frac{Iout}{\sqrt{D}}$	2.51 A	
D(n) peak volts	**D(n) Vpk = VCF1**	75 V	Same for all the diodes.

The tapped-inductor boost converter can provide high output voltage with improved duty cycle and reduced voltage stress on the main switch, assuming the design is done well (Fig. 3.) But once again there are several disadvantages.

This topology cannot reduce voltage stress on the output rectifier. In fact, the voltage stress on the output rectifier is worse than that obtained with a simple boost. Tapped-inductor boost converters also suffer from effects of transformer leakage inductance. The leakage inductance causes voltage spikes and ringing, which in turn causes EMI and increases voltage stress on both the MOSFET and the output rectifier.

These effects can be controlled with snubbers but such remedies waste power. The high voltage stress on the output rectifier frequently precludes the use of Schottky diodes, so the use of ultrafast diodes with discontinuous conduction mode and lower efficiency is often indicated. What's more, the tapped inductor frequently needs to be custom-manufactured (Table 3.)



Tapped-inductor boost topology. In this example N1 = N2. The tapped inductor may also be described as an autotransformer with a gapped core.

Table 3. Equations and example values for key parameters of a tapped-inductor boost converter.

Parameter	Equation	Numerical value for design example (12 V in to 150 V out at 200 mA. N1 = N2.)	Comment
Voltage CF1	N/A	N/A	No such node in this topology.
CCM duty cycle, D	$D = \frac{1}{1+\frac{Vin*(N1+N2)}{N1*(Vout-Vin)}}$	85.19%	
Q1 peak volts	$Q1\ Vpk = Vin + \frac{(Vout-Vin)*N1}{(N1+N2)}$	81 V	Does not include leakage L spikes.
Q1 amps RMS (large L)	$I\ rms \sim \frac{\sqrt{D} * Iout * (N2+N1)}{(1-D)*N1}$	2.492 A	Approximation is very close for low inductor ripple.
D1 peak volts	$Vout + \frac{N2*Vin}{N1}$	162 V	Does not include leakage L spikes.

Need For A Better Technique

All of the above techniques have significant drawbacks for delivering significant power at large boost ratios. As a result, there is a need for a converter topology that offers the following capabilities:

- Delivers high boost ratios with minimum voltage and current stress being imposed on the switches (We would like to use moderately rated (for example, 30 to 100-V range) MOSFETs and Schottky rectifiers if we can do so.)
- Operates at moderate duty cycles (for example less than 85% to 90%) for easier CCM and PWM control
- Is a "true switcher" without the drawbacks (including low output current) of charge pumps
- Avoids the voltage spikes and ringing associated with transformer leakage inductance

The SEPIC-multiplied boost converter achieves all of the above goals. Specifically, it offers the following advantages:

- Voltage stress on the main switch and rectifiers is reduced. This results in an improved set of component selection tradeoffs for price and performance. Peak-to-peak voltage swing on the switch node is greatly reduced so that switching losses are reduced.
- The duty cycle is much closer to symmetry, often enabling CCM with straightforward current-mode control.
- EMI and noise are reduced due to lower peak-to-peak voltage swing on the switch node, and also often due to reduced ringing caused by multiple inductor current discharge paths.
- The converter experiences no ringing or voltage stress resulting from transformer leakage inductance.
- There is none of the increased current stress or distorted current waveforms that charge pumps typically cause.

Comparison Example Of The SEPIC-Multiplied Boost Converter

Compared to a straight boost converting the same voltages, this technique provides a more symmetrical duty cycle and reduced voltage stress on the MOSFET and the rectifiers (Fig. 4.) Although having two diodes increases total diode forward drop, lower peak reverse voltage on each allows use of Schottky or lower V_f types, and the smaller peak-to-peak ac waveform reduces switching loss.

The SEPIC-multiplied boost also avoids the spikes and ringing that are caused by leakage inductance in a transformer. It is a “true” switcher that uses inductor windings as current sources and capacitors as voltage sources. It therefore avoids the differentiated current spikes that are characteristic of charge pumps.

Despite those benefits, the SEPIC-multiplied boost does have some disadvantages that must be acknowledged. The increased number of series-connected rectifiers raises the total rectifier forward voltage drop. Although, this loss is usually outweighed by other efficiency advantages. Another drawback is the increased complexity and parts count of the SEPIC-multiplied boost (Table 4.)

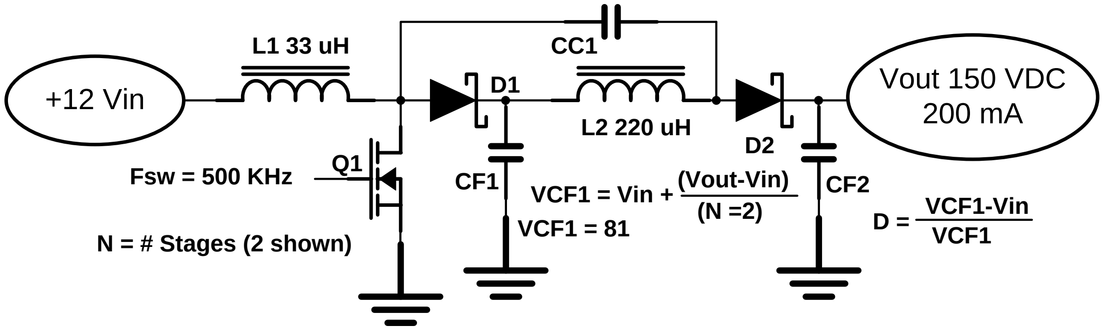


Fig. 4. SEPIC-multiplied boost converter. This example uses N=2 stages. Inductor windings may be discrete or coupled. In the latter case, the inductances of the windings shown as L1 and L2 will be identical.

When comparing boost topologies, it should be noted that none of the voltage-multiplication techniques (including the SEPIC-multiplied boost) are particularly helpful when Vin and Vout are both high. For example, if we had 140-V input and 150-V output, no number of multiplier stages N would reduce the peak imposed on the diodes and MOSFET to less than 140 V. The large number of stages would simply add more series windings and diodes, thus increasing the cost and the total circuit losses. Regardless of Vout, within the scope of this application note, if the boost *ratio* is low then a simple boost will probably be the best approach.

Table 4. Equations and example values for key parameters of a SEPIC-multiplied boost converter.

Parameter	Equation	Numerical value for design example (12 V in to 150 V out at 200 mA.)	Comment
Voltage CF1	$\mathrm{VCF1} = \mathrm{Vin} + \frac{(\mathrm{Vout}-\mathrm{Vin})}{(N=2)}$	81 V	
CCM duty cycle, D	$D = \frac{\mathrm{VCF1}-\mathrm{Vin}}{\mathrm{VCF1}}$	85.19%	This is a figure that is readily achieved by most controller ICs.
Q1 peak volts	Q1Vpk = VCF1	81 V	Q1Vpk varies with Vin and Vout and is higher than with charge-pump-multiplied boost.
Q1 amps RMS (large L)	$I\ \mathrm{rms} \sim \frac{\sqrt{D} * N{*}\mathrm{Iout}}{(1-D)}$	2.492 A	Approximation is very close for low inductor ripple.
D(n) peak volts	D(n)Vpk = VCF1	81 V	D(n)Vpk varies with Vin and Vout and is higher than with charge-pump-multiplied boost.
Total effective parallel inductance Lp(eff) using "n" discrete inductors	$\mathrm{Lp(eff)} = \frac{1}{\frac{1}{L1} + \frac{1}{L2} + \dots \frac{1}{Ln}}$	29 µH	The total effective parallel inductance determines ripple current through Q1 during D. It is possible for some of the inductor currents to pass through zero while the totaled waveform at Q1 is CCM.
Total effective parallel Lp(eff) inductance using one multi-winding coupled inductor.	Use rated inductance for any one winding or for all windings connected in parallel.	33 µH would be a good choice but is not shown in the example above.	Although coupled inductors tend to understress the output winding current, using one multi-winding component may save BOM/assembly cost or PCB space compared to several discrete inductors.
Peak-to-peak ripple current in Q1 during on-time	$\mathrm{Q1\ Ip\text{-}p} = \frac{\mathrm{Vin} * D}{\mathrm{Lp(eff)}{*}\mathrm{Fsw}}$	710 mA	Note that the ripple current passing through Q1 is not represented by that in any one inductor winding.
Q1 peak amps (for CCM)	$I\ \mathrm{in} = \frac{I\ \mathrm{out} * N}{(1 - D)} + 0.5{*}\mathrm{Ip\text{-}p}$	3.06 A	

Derivation Of The SEPIC-Multiplied Boost Converter

This section intends to illustrate how the SEPIC-multiplied boost converter is derived from SEPIC and boost topologies. Figs. 5 through 8 show the evolution of the SEPIC-multiplied boost from the related topologies.

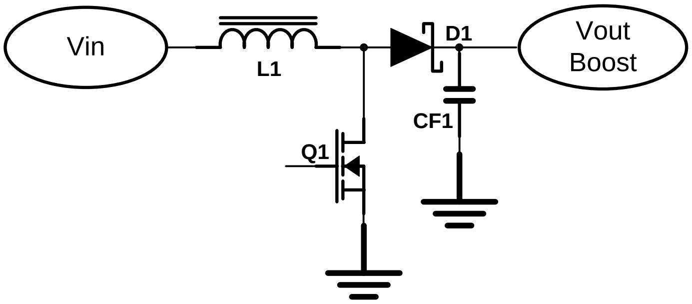


Fig. 5. Simple boost converter. This is one of the most basic converter topologies. It produces Vout > Vin.

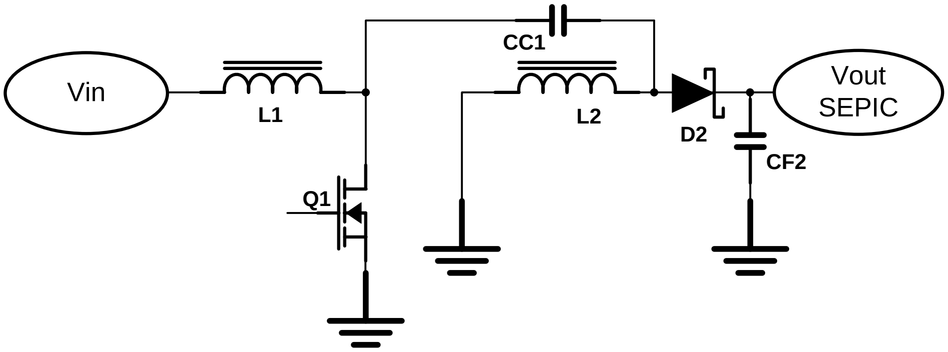


Fig. 6. Single-ended primary inductance converter (SEPIC). The SEPIC is a member of the buck-boost family. Vout and Vin have the same polarity. Its primary application is where Vin can vary above or below Vout. Note that one end of L2 is grounded. Both ends of L2 have an average dc voltage of 0 V.

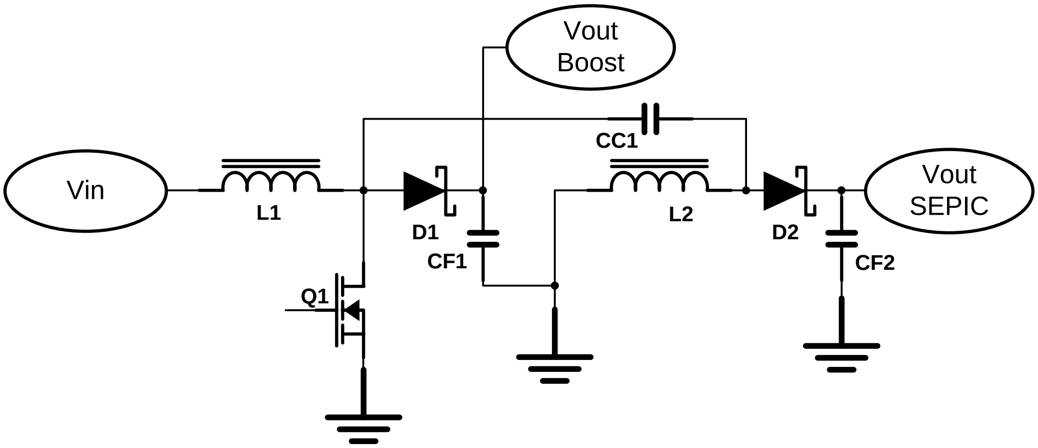


Fig. 7. SEPIC with added boost output. By adding a diode and output filter to the SEPIC we can obtain an additional boost output. Only one of the two outputs (either the boost or the SEPIC) can be regulated while the other will vary with Vin, so the usefulness of this dual-output technique is limited to special circumstances. However, both outputs are delivered "cleanly" without corruption of key voltage or current waveforms.

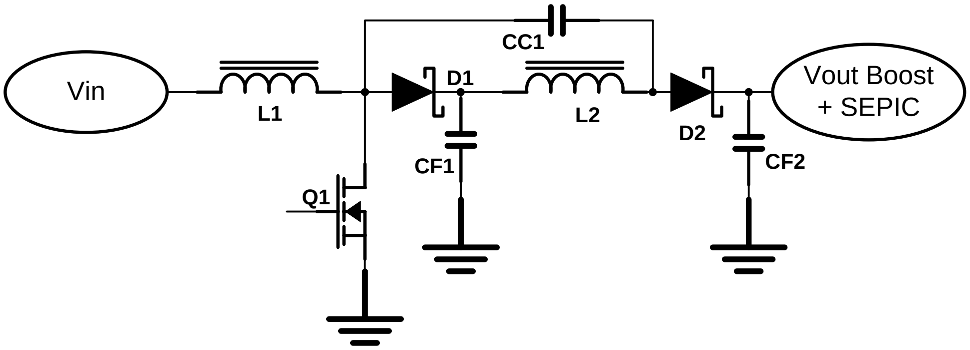


Fig. 8. SEPIC-multiplied boost (N = 2). This topology is based on the SEPIC with added boost output example. The only change is that L2 is now connected to D1-CF1 (which was Vout boost) instead of to ground. L2 and the SEPIC stage are connected in dc series with the boost output at CF1. Both ends of L2 have an average dc voltage equal to the boost voltage on CF1.

Circuit Analysis Of A Multistage SEPIC-Multiplied Boost

In this section, we'll analyze the circuit operation of a multistage SEPIC-multiplied boost converter (Fig. 9.)

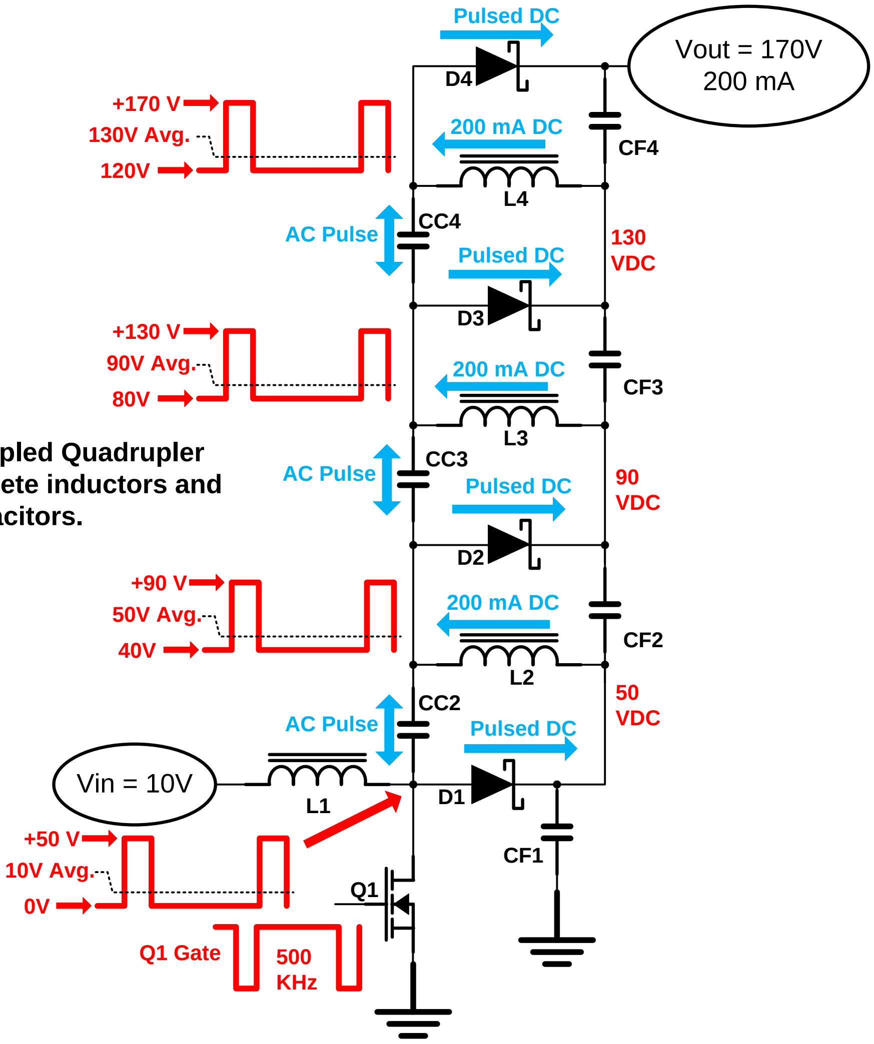


Fig. 9. SEPIC-coupled quadrupler.

We will start off with some simplifying assumptions:

- All components are perfect. The MOSFET and diodes have 0-V forward drop and zero off-state leakage current.
- The inductor values are large so that inductor ripple current is negligible. The current through the inductors is relatively pure dc.
- The capacitors function as dc voltage sources with negligible ripple. Therefore, the ac voltages on both ends of any given capacitor may be assumed to be identical.
- Operation is continuous-conduction mode (CCM) with instantaneous transitions and no dead time.
- There are no losses.

This example has been constructed to give us easy calculations. Our requirements are Vin = 10 V and Vout = 170 V at 200 mA. Our controlling IC switches the MOSFET at 500 kHz.

First, by examination we see that the only dc current path from L1-Q1 (the switch node) to the output is via L2 through L4 and D1 through D4. (L1 needs to be considered separately because it also passes current into Q1. We will discuss L1 later.) Therefore, L2 through L4 and D1 through D4 must all carry 200 mA dc.

Because the ac voltage waveform (not the dc component) on both ends of any capacitor are assumed to be identical, we can see that the *ac* waveform present at the switch node (that is the drain of Q1, which is the main switch) is replicated on both ends of CC2, CC3, and CC4. By visual analysis and inductor volt-second balancing, we can see that if the switch node peaks at some boost value equal to Vb volts above Vin, then the voltage at the anode of D2 must likewise peak at Vb volts above the voltage at the cathode of D1.

Similarly, the voltage at the anode of D3 must peak at Vb volts above that on the cathode of D2, and the voltage at the anode of D4 must peak at Vb volts above that on the cathode of D3. All four stages have similar ac voltage waveforms, so the Vb voltage "gain per stage" is identical for each stage. The total voltage gain achieved (170 V – 10 V = 160 V) is divided evenly among the four stages.

The numerical expression which gets us to Vb is

$$\mathrm{VCF1} = \mathrm{Vin} + \frac{(\mathrm{Vout}\text{-}\mathrm{Vin})}{(N = 4)},$$

which gives us 50 V out of the first stage. Because each stage produces the same boost differential, each stage then produces 50 V – 10 V = 40 V of Vb boost differential or "gain." The four stages produce dc levels of 50 V dc, 90 Vdc, 130 Vdc. and 170 Vdc, respectively.

Next, we calculate duty cycle based on inductor volt-second balancing. The expression

$$D = \frac{\mathrm{VCF1}\text{-}\mathrm{Vin}}{\mathrm{VCF1}}$$

gives us 80% duty cycle. (By comparison, a simple boost would require >94% duty cycle in order to produce the same 10-V to 170-V voltage conversion.)

The above information allows us to construct the ac voltage waveforms that are included (shown in red) in the Fig. 9 schematic diagram. The waveform at the anode of D1 has an 80% duty cycle, a peak-to-peak value of 50 V, and a dc average of 10 V = Vin. Diodes D2 through D4 each have the same ac waveform but the dc voltages are shifted by 40 V for each stage.

At this point, it's time for some visual analysis: If D = 80% then diodes D1 through D4 are only conducting during (1-D) = 20% of the time. The average of 200 mA dc passing through D4 is actually embodied in a 20% duty cycle current pulse. If our current pulse waveforms have a dc average of 200 mA and a 20% duty cycle, the pulses must have an amplitude of 200 mA/20% = 1 A.

It follows that the current waveform in diodes D1 through D4 looks like the one in Fig. 10.

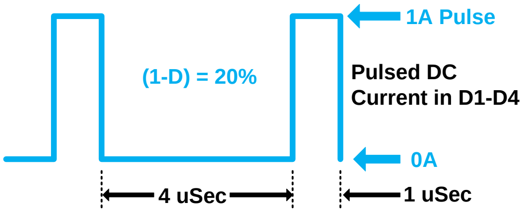


Fig. 10. Pulsed dc current in diodes D1 through D4 of the SEPIC-coupled quadrupler in Fig. 9.

This waveform has a 1-A peak-peak ac component combined with a 200-mA dc offset. This combination is consistent with the instantaneous current never getting below 0 A. The ideal diodes do not conduct reverse current. In fact, most modern Schottky diodes rated above 25 V come pretty close to this, with 100°C reverse current below 100 µA.

For D1, this diode current waveform is supplied by L1 and Q1. Q1 cannot source positive current, and the current through L1 is positive dc coming from the 10-V input. It follows that the 1-A level is supplied by the inductor to diode D1 when Q1 is off during (D-1) and diverted to ground through Q1 when it is turned on during D. The total amount of current passing through L1 and Q1 will be calculated later.

Let us now focus our attention on D4. Because capacitors cannot pass dc current, we know that CC4 can provide only ac. At the same time, L4 supplies 200 mA of relatively pure dc. It is helpful to compare the current sources feeding D4 with those feeding D1. For both D4 and D1, the dc current component is supplied by the respective inductor windings. For D1, the ac current component is supplied by Q1 while for D4, the ac component is supplied by CC4.

The current waveform through CC4 looks like that shown in Fig. 11:

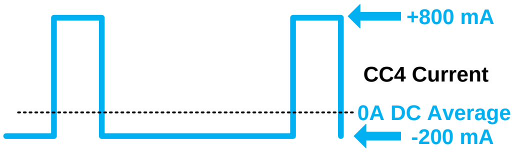


Fig. 11. Waveform for current through CC4 of the SEPIC-coupled quadrupler in Fig. 9.

This ac-only current in CC4 does not pass through L3, but instead gets to CC4 via CC2 and CC3. This ac current adds to the dc component from L4 to produce the common diode-current waveform shown at the beginning of this discussion. This diode current gets averaged by the output filter capacitor, which is comprised of CF1 through CF4 connected in series.

We have a similar situation for D3, CC3, and L3, with one important difference. While L2, L3, and L4 all pass the same 200 mA dc in series, D3 and D4 each require their own 1-A p-p ac pulse. These ac current pulses are additive:

- CC4 passes 1 A p-p for D4
- CC3 passes 1 A p-p for D3 + 1 A p-p for D4 = 2 A p-p.
- CC2 passes 1 A p-p for D2 + 1 A p-p for D3 + 1 A p-p for D4 = 3 A p-p.

This current feeding CC2 all originates from the combination of Q1 and L1.

The current waveforms through CC2 and CC3 are shown in Fig 12.

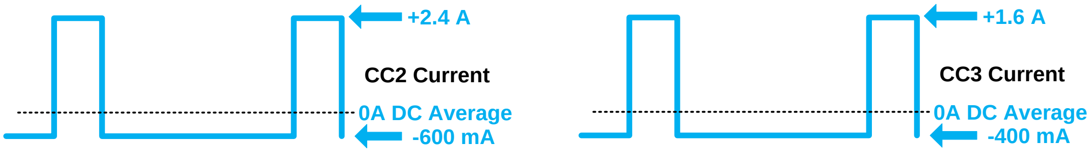


Fig. 11. Waveform for current through CC2 and CC3 of the SEPIC-coupled quadrupler in Fig. 9.

In addition to the ac current for CC2, Q1 and L1 also supply all of the ac + dc passing through D1 (see current waveform common to all four diodes towards the top of this discussion). If we add the CC2 current to the D1 current we get the total waveform supplied by Q1 and L1. Note that the average dc value of this composite total is NOT zero amps:

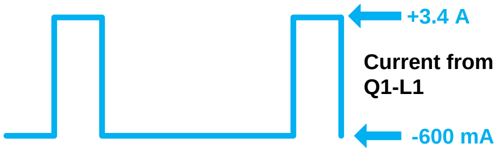


Fig. 11. Total current supplied by Q1 and L1 of the SEPIC-coupled quadrupler in Fig. 9.

The 3.4-A level is supplied by L1 to (CC2 and D1) during (1-D).

During D when Q1 is on, the switch node is at 0 V and L1 supplies 3.4 A to Q1. D1 is blocking, and CC2 conducts 600 mA so Q1 is handling 3.4 A + 600 mA = 4 A. During D, we have a total negative 600 mA into CC2 and D1. Of course this is all passing through CC2 as D1 does not conduct reverse current.

We just observed that the current in L1 is 3.4 A. Our input voltage is 10 V so the input power is 3.4 A x 10 V = 34 W. Notice that the output power is 170 V x 200 mA = 34 W and we figured no losses, so input power equals output power. This agreement suggests that our calculations are valid.

As a further observation, note that the multiple stages operate in ac parallel but in dc series. As a result, in the large signal analysis, the SEPIC-multiplied boost converter models much like a boost converter producing a voltage equal to that on CF1 and an output current equal to Iout x N. Experience suggests that the efficiency approaches that, which would make it better than a straight boost whose efficiency tends to drop more rapidly as the boost ratio increases.

Design Methodology

Step 1) The first task is to choose the best topology for the needed voltage conversion. This may or may not be the SEPIC-multiplied boost, depending upon several constraints:

Step 1a) In order for the SEPIC-multiplied boost topology to benefit the maximum duty cycle and component stress, the output voltage required (or the maximum output voltage, if it is variable) must be at least several times higher than the maximum input voltage. A low boost ratio and high Vout implies that Vin is also high. In this case, the duty cycle of a straight boost will not be high, and the SEPIC-multiplier technique will not offer significant reductions in the maximum stress on the MOSFET and diodes. A straight boost is probably the best option in that case.

Step 1b) For low output current (50-mA range or less, depending on the boost ratio and semiconductors being used) a charge-pump-multiplied boost is likely to be sufficient and less expensive than the SEPIC-multiplied boost. The efficiency for the SEPIC-multiplied boost should be better than that for the charge-pump multiplier, so high efficiency is another reason to prefer the SEPIC multiplier.

Table 5 presents some sample sets of requirements along with observations on whether the SEPIC-multiplied boost is recommended for each set of operating conditions.

Table 5. Rating the usefulness of the SEPIC-multiplied boost converter under various operating conditions.

Vin min. (V)	Vin max. (V)	Vout min. (V)	Vout max. (V)	Iout (mA)	Comment
5.0	6.0	12	80	150	Compared to a straight boost, the increased total rectifier forward voltage drop in the SEPIC doubler or tripler will cause some reduction in efficiency when Vout = 12 V. However the technique will help significantly when Vout = 80 V. A SEPIC-doubled or -tripled boost is worth considering.
30	60	70	80	150	No quantity of multiplier stages can prevent the MOSFET and rectifiers from voltage stress of at least 60 V, and a simple boost will result in 80 V of stress on these. The SEPIC-multiplier technique will not be helpful.
5.0	6.0	80	80	5	Due to the low current, a charge-pump-multiplied boost will probably be adequate and should be considered first. The SEPIC-multiplied boost will also work nicely and may provide better efficiency, but will usually be more expensive.

Step 2) Although the subject of this article concerns high boost ratios, it is usually better to avoid a high ratio boost if you can. For example if you need to create 200 V and have a choice of starting with 5 V or 12 V as your power input, the 12-V option will almost always yield better performance, even if you are using the SEPIC-multiplied boost. If you have both input rails available, by all means use the 5 V for biasing ICs such as the ADP1621 or ADP1613. The 12-V input will cause a small increase in the peak switch-node voltage, but (for the same ratio N) it will provide a lower duty cycle, lower peak current, and usually better efficiency.

Step 3) Using the formula

$$V_{Q1pk} = V_{CF1} = V_{in} + \frac{(V_{out}-V_{in})}{N}$$

determine the value of N that will allow your MOSFET and diodes (Schottky diodes are much better if you can use them) to operate with reasonable voltage ratings. If you are using the ADP1621 controller with 5-V bias, you have a strong 5-V gate driver. The vast majority of good 30-V Vds rated MOSFETs are "logic level" types; specified for 4.5 V of gate drive. However, unless you are boosting from ~ 4.3 V or less (which will make the overall design more challenging) 30 V seems an unnecessarily low constraint on the peak voltage at the switch node.

While not all 60-V Vds MOSFETs are capable of working with 5-V drive, many of them are and that is one useful popular rating. As the Vds rating of MOSFETs increases to 75 V to 100 V, there is a dwindling selection of logic-level MOSFETs. Schottky diodes are readily available with ratings up through 100 V but there are few over 100 V. Make sure you can actually get the components you want to use. For ADP1621 designs, peak switch-node voltages in the range of 50 V to 90 V (allowing margin from the device rating) are a reasonable starting point for the high-ratio boost when 5 V or higher input voltage is available. The ADP1613 is limited to a peak switch-node voltage of 20 V unless the cascode configuration is used.

Step 4) Choose controller IC and driver configuration. The simplified "configuration example schematic" diagrams shown in Figs. 12 through 16 include input/output voltages that are reasonable for the components and the topology. In Fig. 12, the ADP1621 controller is used in a standard current-sense-resistor configuration. This is the configuration that is likely to be most popular for the SEPIC-multiplied boost. The ADP1621 is capable of controlling peak MOSFET currents of up to at least 10 A, and MOSFETs are available that will allow peak switch-node voltages in the 50-V to 90-V range.

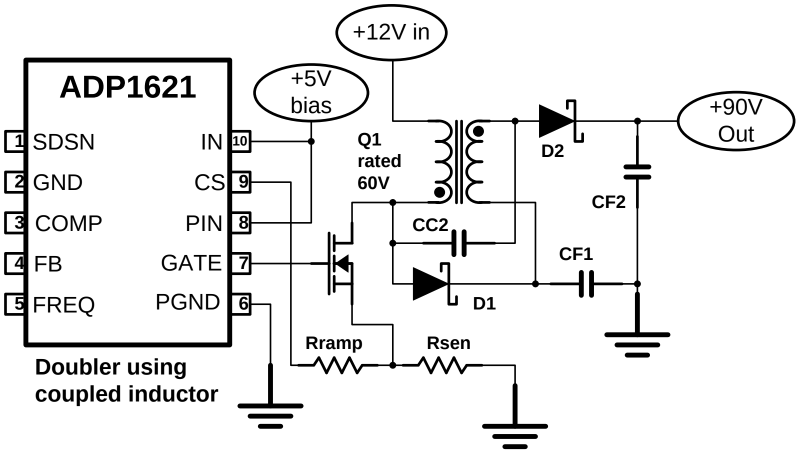


Fig. 12. ADP1621 step-up dc-dc controller in a standard current-sense-resistor configuration.

Fig. 13 shows the ADP1621 in a standard "lossless-current-sense" configuration. For this mode of operation the ADP1621 itself limits the peak switch-node voltage to 30 V, so it best fits use with MOSFETs that are rated at 30 V. Lossless current sense and a 30-V MOSFET may be a reasonable approach if your input power rail is 5 V.

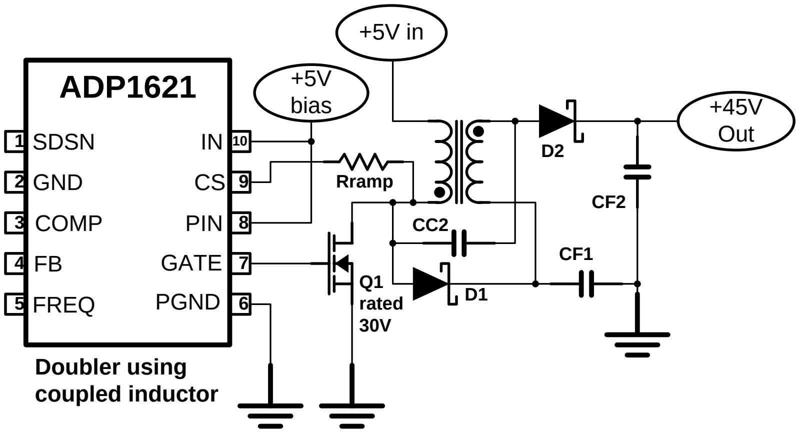


Fig. 13. ADP1621 in a standard lossless-current-sense configuration.

In Fig. 14, the ADP1621 appears in a cascode configuration. The cascode topology provides the highest switch-node voltage capability. This approach can be reasonable for switch-node voltages above 50 V to 100 V. If appropriate cascode gate bias is available, it eliminates the restriction of logic-level gate drive for the upper MOSFET. You can use lossless current sense on the lower MOSFET unless accurate current limiting is a priority. Remember that the diode reverse-voltage rating has to exceed the peak switch-node voltage.

This drive topology may be difficult to implement unless adequate gate bias (such as 12 V) is available. Because the turnoff gate current in the cascode MOSFET is all derived from drain current, excessive gate charge in this MOSFET will cause switching losses and efficiency to suffer. For this reason, the MOSFET die must not be oversized and it must have a good gate-charge figure of merit. As load current is reduced, efficiency will fall because the reduced available gate current slows the turnoff transitions.

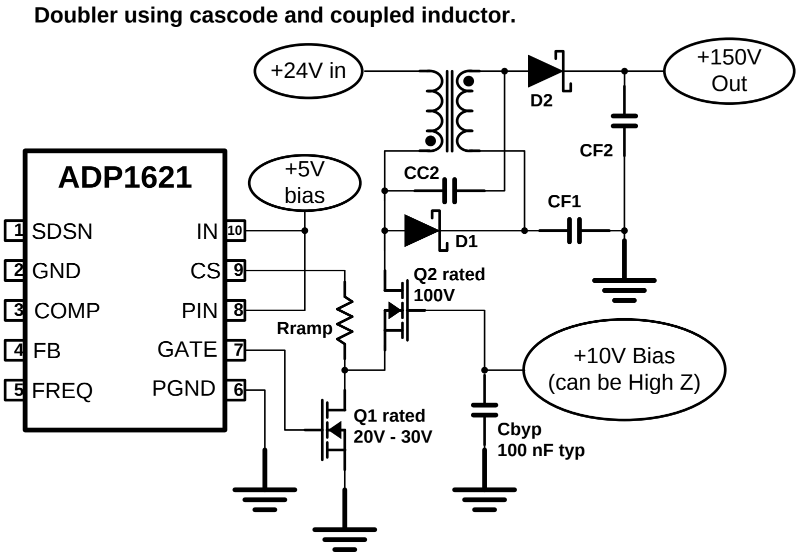


Fig. 14. ADP1621 in a cascode configuration.

The ADP1613 is applied in the standard configuration in Fig. 15. The ADP1612 can also be used in this configuration. Because the output switch on the ADP1612/3 is limited to 1.3 A and 20 V, this approach makes the most sense for relatively low current and low voltage applications. An example would be a 3-V to 60-V conversion (with a tripler) or a 3-V to 40-V conversion as shown here, where no higher input-bias rail is available. The ADP1613 should be used for Vin between 2.5 V and 5.0 V; use the ADP1612 for applications where the input voltage can go as low as 1.8 V.

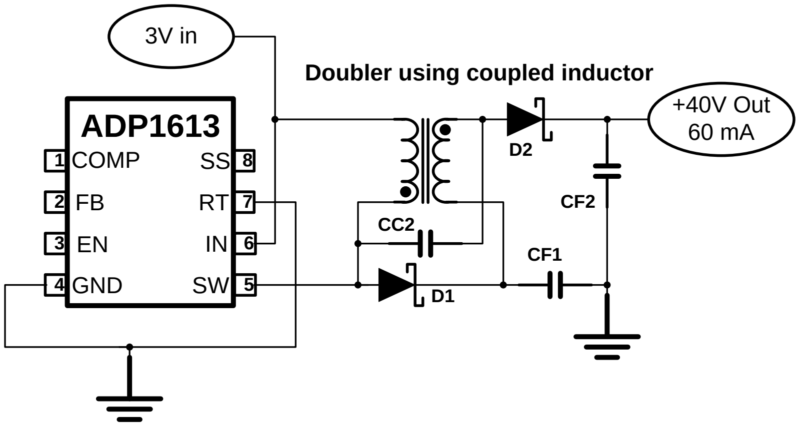


Fig. 15. Either the ADP1613 or ADP1612 dc-dc converter IC can be used in this standard configuration. (The controller choice depends on the input voltage requirement.)

Like the ADP1621, the ADP1613 can also be used in a cascode configuration as shown in Fig. 16. The cascode topology provides the highest switch-node voltage capability. The ADP1613 works nicely in this role so long as you observe a few rules. You are limited to the 1.3 A of peak current in the main ADP1613 output switch.

Some of the same cautions given for the cascode circuit in Fig. 14 apply here as well. This drive topology may be difficult to implement unless adequate gate bias (such as 12 V) is available. Due to the fact that turnoff gate current in the cascode MOSFET is all derived from drain current, excessive gate charge in this MOSFET will cause switching losses and efficiency to suffer. For this reason, the MOSFET die must not be oversized and it must have a good gate-charge figure of merit. As load current is reduced, efficiency will fall because the reduced available gate current slows the turnoff transitions. The higher operating frequency of the ADP1613 means that excessive gate charge in the cascode MOSFET can easily contribute a significant amount of switching loss.

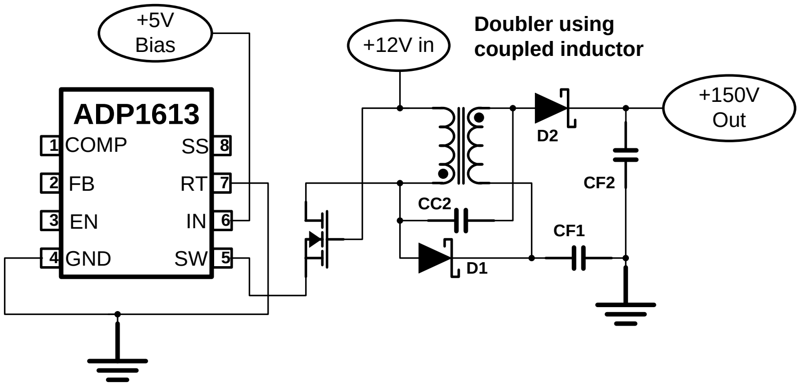


Fig. 16. ADP1613 in a cascode configuration.

Step 5) Determine D using $D = \frac{VCF1 + Vf - Vin}{VCF1 + Vf}$ where Vf is the Schottky diode Vf; generally 500 mV to 600 mV.

Step 6) Figure the dc input current. For CCM operation (preferred in most cases) the input inductor current is approximately

$$I\ in = \frac{I\ out * N}{(1 - D)}$$

Step 7) Figure the peak MOSFET current. Iin from above must include some ripple. For a typical design with 40% input ripple, assume that the MOSFET must handle a peak current ~ Iin x 120%.

Step 8) From step 7, we can probably now choose our IC. If the peak MOSFET current is under about 1.4 A, then the ADP1613 can probably provide the lowest-cost solution. If the peak MOSFET current exceeds this level, or if the best efficiency is required with peak MOSFET current, which is more than a 600 mA or so, then the ADP1621 is indicated.

Step 9) Figure RMS MOSFET current using

$$I\ rms \sim \frac{\sqrt{D} * N*Iout}{(1-D)}$$

Step 10) Choose MOSFET based upon RMS current and VCF1.

- If using an ADP1621 without the cascode MOSFET; the MOSFET must be a logic-level type that is rated for a suitable RDS(on) (based on conduction losses given the calculated RMS current) with 5 V or less of gate drive. Of course, it must have a Vdss rating that exceeds VCF1.
- If using the ADP1613 with a cascode MOSFET, the cascode MOSFET need not be a logic-level type. However, the MOSFET should be chosen to have very good switching figure of merit. While the RDS(on) must be low enough for the current, oversizing the cascode MOSFET will cause excessive switching losses and may interfere with proper voltage conversion. You need to produce the necessary gate dc bias voltage for the cascode MOSFET; generally 5 V to 12 V. This requires negligible dc current so high-value resistor dividers can often provide it. However it must be carefully bypassed to ground at the MOSFET gate using a 100-nF to 1-µF ceramic capacitor.
- If using the ADP1621 with a cascode MOSFET, the cautions regarding the cascode MOSFET for the ADP1613 are also applicable. However you also need the “bottom” MOSFET, which will be driven by the ADP1621 gate driver. This bottom MOSFET can be a relatively small 20-V to 30-V type that has fast switching and is suitable for the RMS current. Because this MOSFET will see a peak drain voltage less than ~ 15 V, the ADP1621 can be operated in lossless-current-sense mode where the bottom FET RDS(on) serves as the current-sensing resistance.

Step 11) Operating frequency: Higher frequency can usually help reduce the size of ceramic filter and coupling capacitors. It may also permit a size reduction in the inductors. However, given the high-voltage intent of these converters, maximizing switching frequency will tend to increase switching losses. Higher switching frequency also interacts with minimum off-time to limit maximum duty cycle. For ADP1613 designs, choose the lower 700-kHz Fsw. For the ADP1621, let’s choose the not-too-aggressive figure of 400 kHz. These settings can be modified later if desired.

Coupled Versus Uncoupled Inductors

Similar to SEPIC and Cuk converters, the SEPIC-multiplied boost can often use coupled inductors. Coupled inductors have both advantages and disadvantages relative to uncoupled (discrete) inductors. One advantage is that the use of coupled inductors often results in a lower overall BOM cost than discrete inductors. Another is that coupled inductors may allow a more compact design using less PCB area.

On the other hand, coupled inductors may tend to concentrate heat in a small area, which makes thermal management more challenging. Also, the input inductor handles much more current than do the other windings, especially with high-order N multipliers. In these designs, matching the windings (as on one multi-winding structure) may result in oversizing of the output windings. Another drawback is that, in some cases, the best design may involve dissimilar inductor values; which is not an option with coupled inductors.

In addition to designs using either all discrete or all coupled inductors, another option that may be worth considering is the combination of coupled and uncoupled structures. For example, consider that two-winding coupled inductors are common and inexpensive. This can be advantageous in SEPIC-multiplied boost converters where all windings (other than the input) are subjected to a lower current than that on the input inductor. So, depending on the specific requirements of the design, it may be reasonable to build a tripler using a larger discrete inductor for the input and a two-winding coupled structure for the SEPIC stages.

Variations In Capacitor Connections

Whereas Fig. 9 shows series-connected capacitors used for CC and CF, this is not the only reasonable way to design the converter. When the series connections of CC and CF are used, the capacitors connected in series all operate at the same voltage, so they can have a common voltage rating. However, as explained, CC3 handles twice as much current as CC4 (so CC3 should ideally have double the capacitance) and CC2 handles three times as much current as CC4. As a result, the most cost-effective series-connected design will use similar voltage ratings but dissimilar capacitance ratings.

One disadvantage of the series approach is increased stray inductance due to the multiple series connections. This may cause an increase in spikes, ringing, and EMI.

An alternate "parallel" connection method is shown in Fig. 17. Using this method, all of the CC capacitors and all of the CF capacitors have the same current but the applied voltages differ. The ac parallel connection of the CC capacitors should decrease equivalent series inductance (ESL) presented to Q1, thus reducing spikes in the drain of Q1, damping ringing. Similarly, lower inductance in the output filter should reduce noise spikes there.

Regarding output noise, either the series or parallel configuration can benefit from added output-filter capacitors to ground and/or an added pi filter using a small-value inductor. Remember that while larger case sizes (such as 1210) provide more capacitance, the smaller sizes offer lower ESL. The best designs may parallel 2 to 3 output filter capacitors of different sizes.

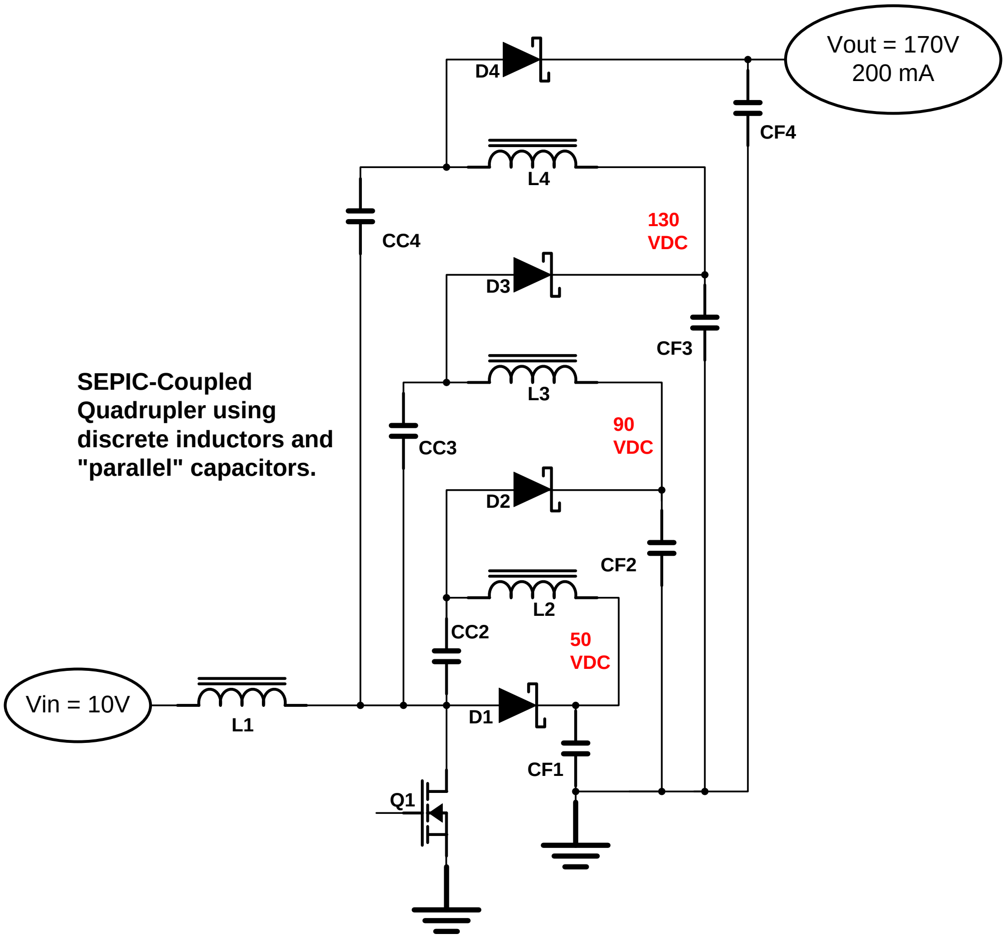


Fig. 17. SEPIC-coupled quadrupler using discrete inductors and parallel capacitors. The ac parallel connection of the CC capacitors should decrease the ESL presented to Q1, reducing spikes in the drain of Q1 and damping ringing.

Choosing Other Components

Of course, the switching MOSFET is a key component in this design. In selecting this component, there are a number of concerns to consider. These concerns are explained here and ranked in approximately descending order of priority:

1) The MOSFET must be rated for the expected voltage stress plus some margin to allow for voltage spikes. Voltage spikes are caused by stray inductance in components (such as the diodes and coupling capacitors) and PCB layout. A good PCB layout will allow spikes that are much lower in voltage than those encountered in transformer-based designs. But even though an excellent PCB layout will do a lot to minimize these spikes, they cannot be eliminated completely. Spike amplitudes in the range of 5 V to 10 V (above the ideal predicted peak voltage on the MOSFET) are reasonable and can vary depending upon many factors.

2) The MOSFET must be rated (mainly according to its RDS(on)) for power that will be dissipated by the expected RMS current. I^2 x R loss is usually the main heating mechanism in the MOSFET. In general, the MOSFET manufacturers' current ratings are very optimistic. A calculation of I^2 x R using the elevated temperature value of the MOSFET on-resistance is the best way to start. From there, use worst-case operating conditions and a conservative estimate of thermal resistance to figure MOSFET die temperature during operation. Maximum operating die temperatures in the range of 85° to 105°C are generally reasonable.

3) The MOSFET RDS(on) must be rated with a gate-drive voltage that is within the capability of the driver IC. In the case of the gate-driven (not cascade, if used) MOSFET used with the ADP1621, a logic-level drive of 5 V or less (4.5 V is a common gate-drive voltage rating) is required. MOSFETs requiring 6 V or more may not be gate driven reliably by the ADP1621 or other controllers with 5-V drive. However, this requirement does not prevent these MOSFETs from working well as cascode MOSFETs.

4) The voltage rating requirements of the diodes and the MOSFET are very similar. As with MOSFET current ratings, diode manufacturer current ratings are usually optimistic. Do not exceed diode datasheet current ratings, but beyond that, the suitability of the diode for the current it conducts should be determined mainly by die temperature and thermal resistance. Generally diodes with a maximum Tj rating of 150°C should not be operated with junction temperatures over 105°C or 110°C.

5) With the exception of bulk bypass electrolytic capacitors for holdup time and/or damping the inductance of wiring between boards, the requirements of these converters are handled nicely by SMT ceramic capacitors. Use X5R for filter capacitors rated 25 V or less, X7R for signal capacitors in the 1-nF to 100-nF range and filters rated over 25 V, and NP0 for signal capacitors of 1 nF or less.

Capacitors should be rated to handle the RMS current to which they will be subjected. When ceramic capacitors are used at frequencies up to a few hundred kilohertz, and ripple voltage is limited to a few percent of the dc rating, ripple-current calculations will usually show that the capacitor is comfortably within its current ratings. For that reason, ceramic capacitors should be first chosen for voltage and (conservatively for capacitance based upon desired ripple voltage.) After the capacitor is chosen, a check of ripple current ratings will usually show ample margin.

A 50-W 200-V Output Pentupler Using ADP1621

This converter boosts 12-V input to 200-V 250-mA output. A schematic for this 5X boost converter is shown in Fig. 18 and the associated BOM is given in Table 6. In this design, we make good use of 60-V-rated MOSFET and Schottky rectifiers. U2 serves as an input undervoltage lockout (UVLO). Unlike transformer-based designs, this converter switches cleanly so that loss-inducing snubbers are not required (Fig. 19.) It has demonstrated efficiency exceeding 91% (Fig. 20.)

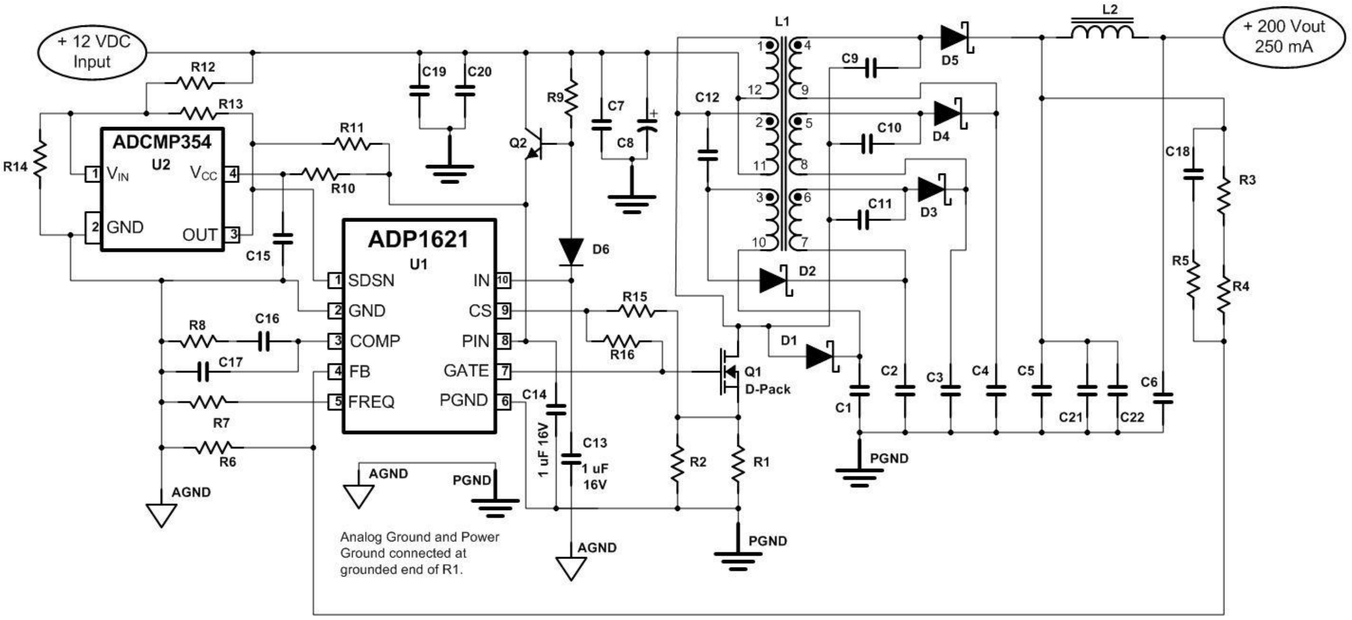


Fig. 18. This SEPIC 5X-multiplied boost converter produces 50-W output at 200 V.

Table 6. BOM for the SEPIC 5x-multiplied boost based on ADP1621.

Item	Ref	Description	Vendor	Part Number
1	C1	1.0 µF X7R 100 V 1206	Murata	GRM31CR72A105MA01K
2	C2	1.0 µF X7R 100 V 1206	Murata	GRM31CR72A105MA01K
3	C3	220 nF X7R 250 V 1210	Murata	GRM32DR72E224KW01L
4	C4	220 nF X7R 250 V 1210	Murata	GRM32DR72E224KW01L
5	C5	220 nF X7R 250 V 1210	Murata	GRM32DR72E224KW01L
6	C6	220 nF X7R 250 V 1210	Murata	GRM32DR72E224KW01L
7	C7	22 µF X5R 25 V 1210	Murata	GRM32ER61E226KE15
8	C8	1000 µf 16V Alum Elect low ESR	Suncon	16ME1000WGL
9	C9	220 nF X7R 250 V 1210	Murata	GRM32DR72E224KW01L
10	C10	220 nF X7R 250 V 1210	Murata	GRM32DR72E224KW01L
11	C11	1.0 µF X7R 100 V 1206	Murata	GRM31CR72A105MA01K
12	C12	1.0 µF X7R 100 V 1206	Murata	GRM31CR72A105MA01K
13	C13	1.0 µF X5R 16 V 0603	TDK	C1608X5R1C105K
14	C14	1.0 µF X5R 16 V 0603	TDK	C1608X5R1C105K
15	C15	1.0 µF X5R 16 V 0603	TDK	C1608X5R1C105K
16	C16	4.7 nF X7R 25 V 0603	Generic	
17	C17	DNP		
18	C18	DNP		
19	C19	22 µF X5R 25 V 1210	Murata	GRM32ER61E226KE15
20	C20	DNP		
21	C21	DNP		
22	C22	DNP		
23	D1	Schottky Diode 1 A 60 V SMA	ON Semi	MBRA160T3
24	D2	Schottky Diode 1 A 60 V SMA	ON Semi	MBRA160T3
25	D3	Schottky Diode 1 A 60 V SMA	ON Semi	MBRA160T3
26	D4	Schottky Diode 1 A 60 V SMA	ON Semi	MBRA160T3
27	D5	Schottky Diode 1 A 60 V SMA	ON Semi	MBRA160T3
28	D6	Diode Signal 100 V 200 mA	ON Semi	MMSD4148
29	L1	Coupled Inductor 6 Windings	Coilcraft	HPH6-0158L
30	L2	Inductor 22 µH	Coilcraft	ME3220
31	Q1	MOSFET 60 V D-Pak Logic Level	Infineon	IPD079N06L3G
32	Q2	BJT NPN 40 V Gen Purpose	Generic	MMBT3904

33	R1	0.020 ohms 0805 5%	Susumu	RL1220
34	R2	0.012 ohms 0805 5%	Susumu	RL1220
35	R3	634K ohms 1% 1206	Generic	
36	R4	1.00 M ohms 1% 1206	Generic	
37	R5	DNP		
38	R6	10.0K ohms 1% 0603	Generic	
39	R7	45.3K 0603 1%	Generic	
40	R8	10K 0603 5%	Generic	
41	R9	1.5K 0805 5%	Generic	
42	R10	100 ohms 0603 5%	Generic	
43	R11	DNP		
44	R12	47.5K 0603 1%	Generic	
45	R13	1.00 M 0603 1%	Generic	
46	R14	2.67K 0603 1%	Generic	
47	R15	499 ohms 0603 1%	Generic	
48	R16	100K 0603 5%	Generic	
49	U1	IC Boost Controller	Analog Devices	ADP1621
50	U2	IC Comparator + Reference	Analog Devices	ADCMP354

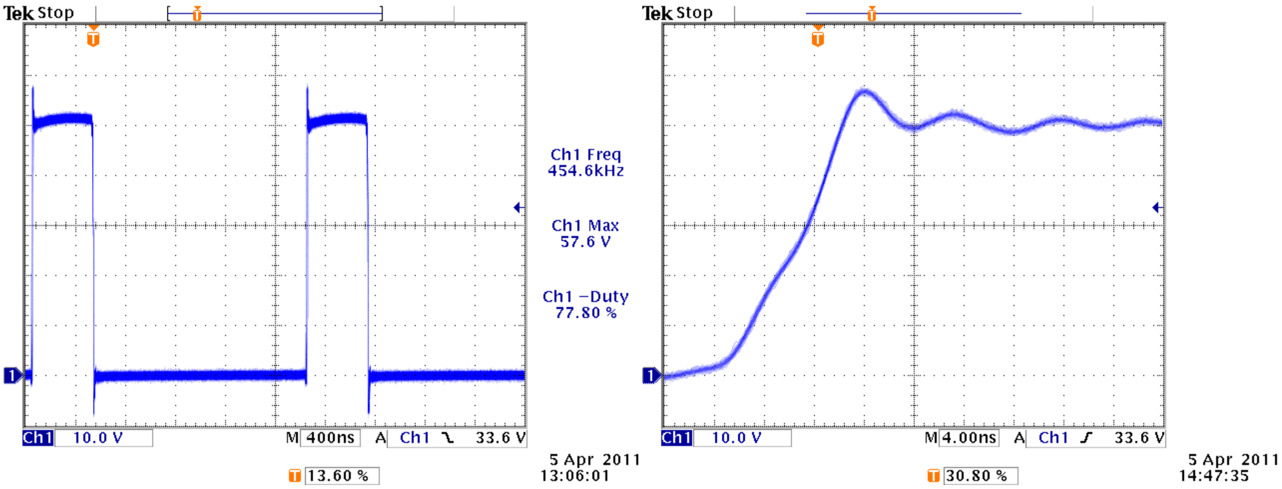


Fig. 19 Waveforms measured at the switch node (drain of Q1) with the boost converter operating at 11.5-V input and 200-V 260-mA output. These waveforms are relatively clean and show that the voltage stress on the 60-V rated MOSFET is much lower than the 200-V dc output voltage. The oscilloscope image on the right focuses on the rising edge of the switch-node waveform and is displayed with a faster oscilloscope timebase. It is difficult to obtain so clean a waveform with transformer-based designs (see Note 2), unless lossy snubbing is used.

Notes:

1. This article is not intended to be a complete or exhaustive design manual. Design engineers requiring assistance with any aspect of designing with this topology are encouraged to contact applications engineering at Analog Devices.

2. As the BOM indicates, the converter uses a member of the Coilcraft HPH series of coupled inductors. These inductors have low leakage inductance and may be used (or referred to) as transformers in some other contexts. But as applied in this SEPIC-multiplied boost, this component functions as a coupled inductor.

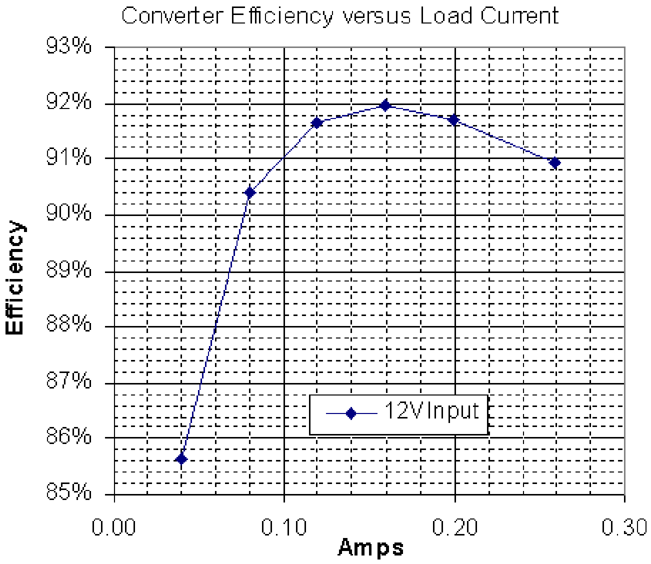


Fig. 20. The peak value of measured efficiency for the SEPIC 5x-multiplied boost converter is almost 92%.

About The Author

Bob Zwicker received a BSEE in 1974 from North Carolina State University and began designing switching power supplies in 1980. He has one patented invention for a method of secondary-side control of synchronous rectifiers. Bob became an applications engineer in 2002 and began doing semiconductor power applications with Analog Devices in 2005. He lives and works out of his home in Olympia, Wash.

For further reading on boost converter design, see the How2Power Design Guide, select the Advanced Search option, go to Search by Design Guide Category, and select "Boost" in the Topology category.