Internal LDO Circuit Offers External Control Of Current Limiting

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There is a growing trend within power semiconductor development to expand the feature set of these devices in order to offer users greater flexibility in their circuit designs. With low drop-out voltage regulators (LDOs), a key function that can be augmented is current limiting. In particular, giving designers external control of current limiting is particularly useful as this enables them to limit power dissipation without resorting to overly complex methods.

Fig. 1 shows a block diagram of a soft-start adjustable CMOS LDO that includes the current-limit protection with external control.[Note] The current through the power transistor P_POWER is replicated through transistor P_TRAD, though at a much lower level, and compared with a reference current sunk by an NMOS transistor (NB2). Three other transistors (PB1, PB2 and NB3) are used to keep P_TRAD at the same drain-to-source voltage as P_POWER.

If the current passing through P_TRAD reaches an equal magnitude to the current sunk by NB2 within the active region, then the current comparator will control the gate-to-source voltage of P_POWER in a way that maintains the level of the existing output current (i.e. the current limit.) By using an additional current-limit block, the size of the reference current through NB1 (as well as NB2 and NB3) can be controlled by using an external resistor (R_{EXT}.) For accurate control, the voltage across R_{EXT} should be kept constant versus the current through it.

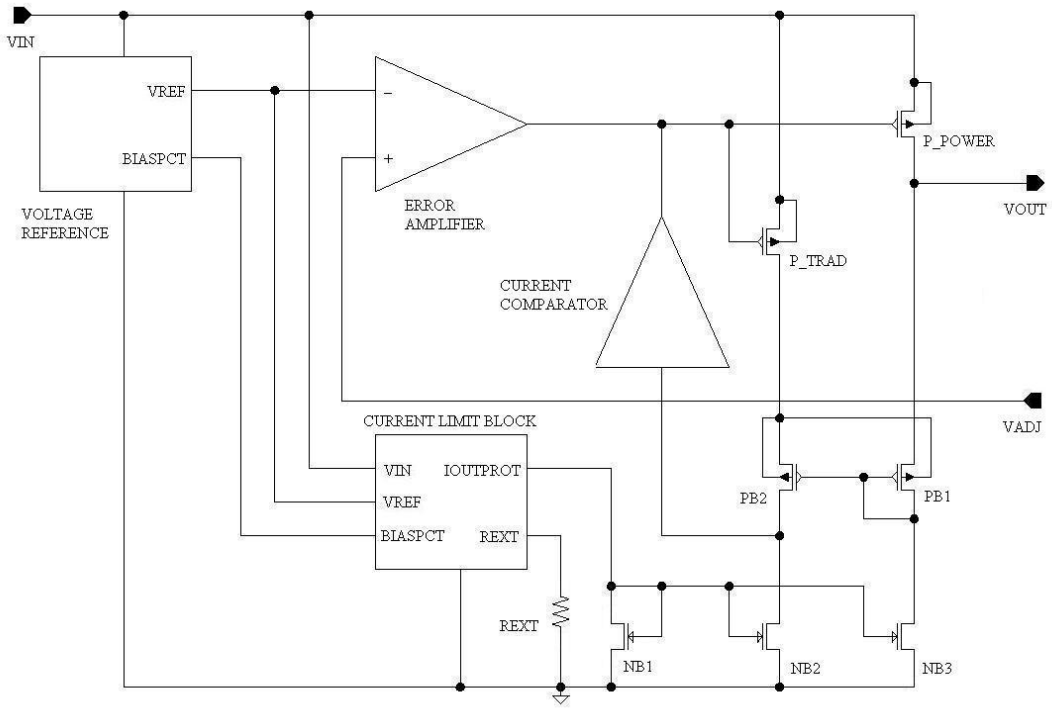


Fig. 1. Block diagram of a CMOS LDO showing current-limit protection.

In Fig. 2 a simplified schematic of the current-limit block is presented. It effectively works as a voltage buffer, delivering the reference voltage V_{REF} to R_{EXT}. The resulting current $I_{OUTPROT}$ is used to bias the diode-connected NB1 from Fig. 1.

The operational amplifier in Fig. 2, configured as a voltage buffer, has two stages. The first stage is a transconductance-amplifier stage with NMOS input transistors (N4 and N5) and PMOS transistors (P2 and P3)

forming the active load. The second stage is a common-drain amplifier stage built around the isolated NMOS transistor (N6). The buffer is biased via transistors N1, N2 and N3, which are biased with a current delivered by the voltage-reference block, which has a temperature coefficient close to zero.

The current mirror formed by the PMOS transistors (P4 and P5) is used to obtain the output current from the block. Frequency compensation is done on the highest impedance node with capacitor CC. All current mirrors are designed for proper overdrive voltage, while N6 is big enough to easily handle a current that is tens of microamps. The current level through N1, N2, and N3 is close to 1 µA. The presence of N3 assures that there is a non-zero current $I_{OUTPROT}$, even if there is no external resistor at all. N6 must be an isolated NMOS device in order to maintain a low gate-to-source voltage while the voltage on its source is close to V_{REF} (i.e. 1.25 V.)

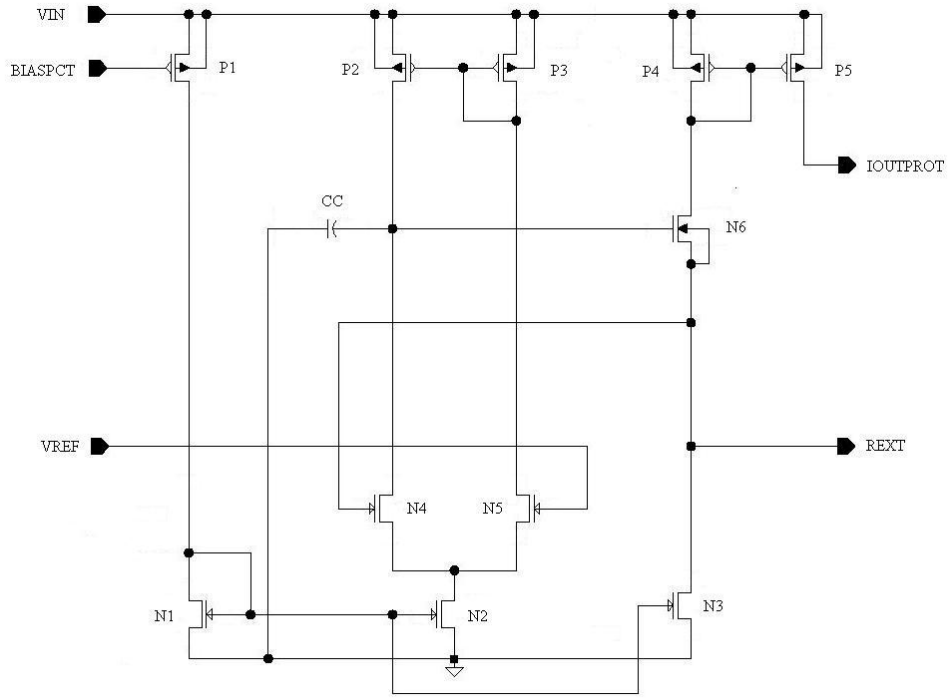


Fig. 2. Simplified schematic of the current-limit block.

The current through resistor R_{EXT} is set so as to keep the resistance value equal to or lower than 100 kΩ for the intended application (which needs continuous load current of 0.3 A or a current limit of at least 0.45 A.) For example, considering R_{EXT} = 82 kΩ and V_{REF} = 1.25 V, it results in:

$$I_{REXT} = \frac{V_{REF}}{R_{EXT}} = \frac{1.25V}{82K\Omega} \approx 15\mu A \qquad (1)$$

Nevertheless, for other applications, R_{EXT} can be easily increased to higher values. The width-to-length ratios of P4 and P5 are designed to lower the value of $I_{OUTPROT}$ in order to save unwanted current consumption. The minimum V_{IN} for which the block is working properly is:

$$V_{IN\_MIN} = V_{REF} + V_{SG\_N6} + V_{OV\_P2} \qquad (2)$$

This is dependent on IR_{EXT} through the value of VSG_N6. It will be quite high due to the fact that N6 is a high-voltage transistor with a high threshold voltage. The overdrive voltage of transistor P2 is 0.3 V.

Circuit Analysis

A series of high-accuracy HSPICE circuit simulations were performed to verify the characteristics of the proposed technique. Fig. 3 shows the variation of VR_{EXT} versus V_{IN}, considering a sweep of IR_{EXT} between 0 and 20 µA, with a step of 5 µA. It is desired for the voltage VR_{EXT} to be constant in relation to both V_{IN} and IR_{EXT}

variations. For V_{IN} higher than 4 V, up to 14 V, VR_{EXT} has a good line regulation, at any IR_{EXT} value, better than 40 mV.

As expected, the knee of the graph does, depend on the IR_{EXT} current level to some extent, but not very much. It is between 3.4 V (at zero current) and 4 V (at 20 µA.) Load regulation (i.e. VR_{EXT} variation versus IR) is also good, being close to 80 mV.

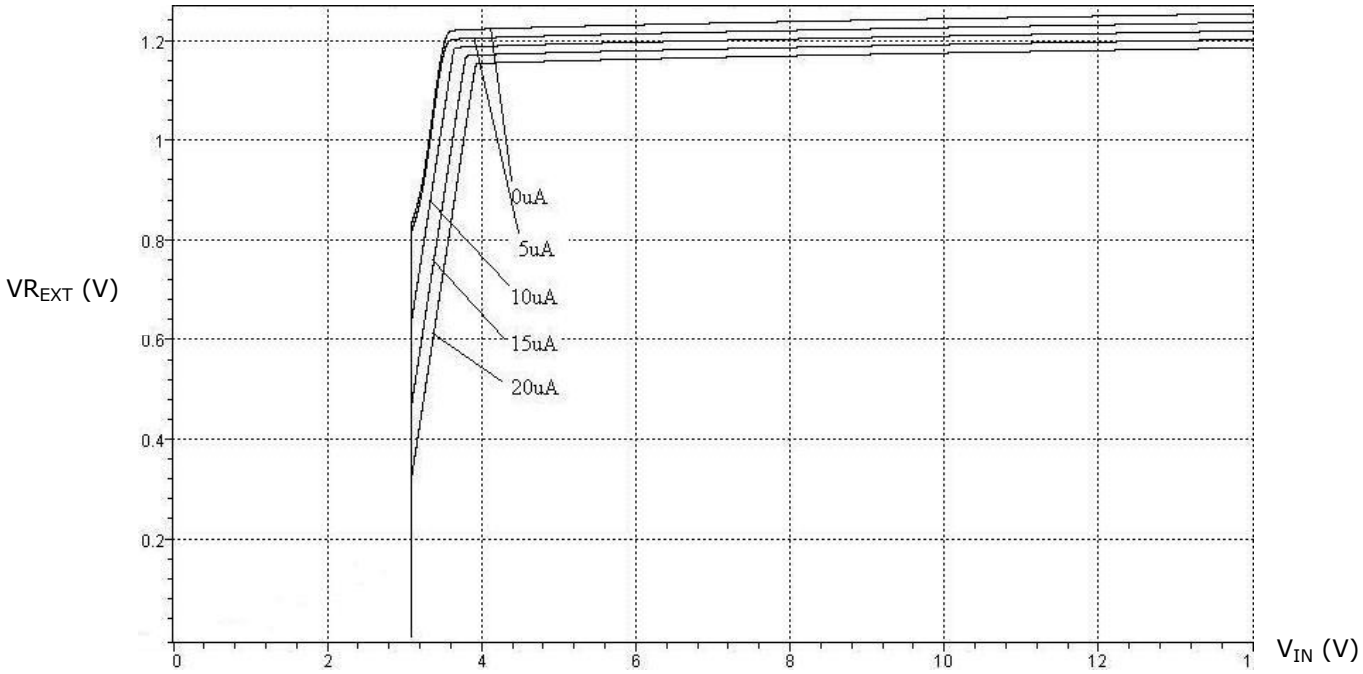


Fig. 3. Simulated VR_{EXT} versus V_{IN} for IR_{EXT} values of 0, 5, 10, 15, and 20 µA.

Fig. 4 shows the short-circuit current of the LDO itself versus V_{IN}, considering the same IR_{EXT} sweep. For zero IR_{EXT} (no R_{EXT}), the current limit is lower than 0.1 A and is slowly increased with V_{IN}. The short-circuit current value increases almost linearly with IR_{EXT}.

For IR_{EXT} = 15 µA, the current limit will be 0.44 A to 0.47 A, which is appropriate for an application with 0.3-A continuous current. This corresponds to R_{EXT} = 82 kΩ. For IR_{EXT} = 20 µA, the current limit is already pretty high, at 0.54 A to 0.605 A. From this, the recommended V_{IN} domain was considered to be between 4 V and 14 V.

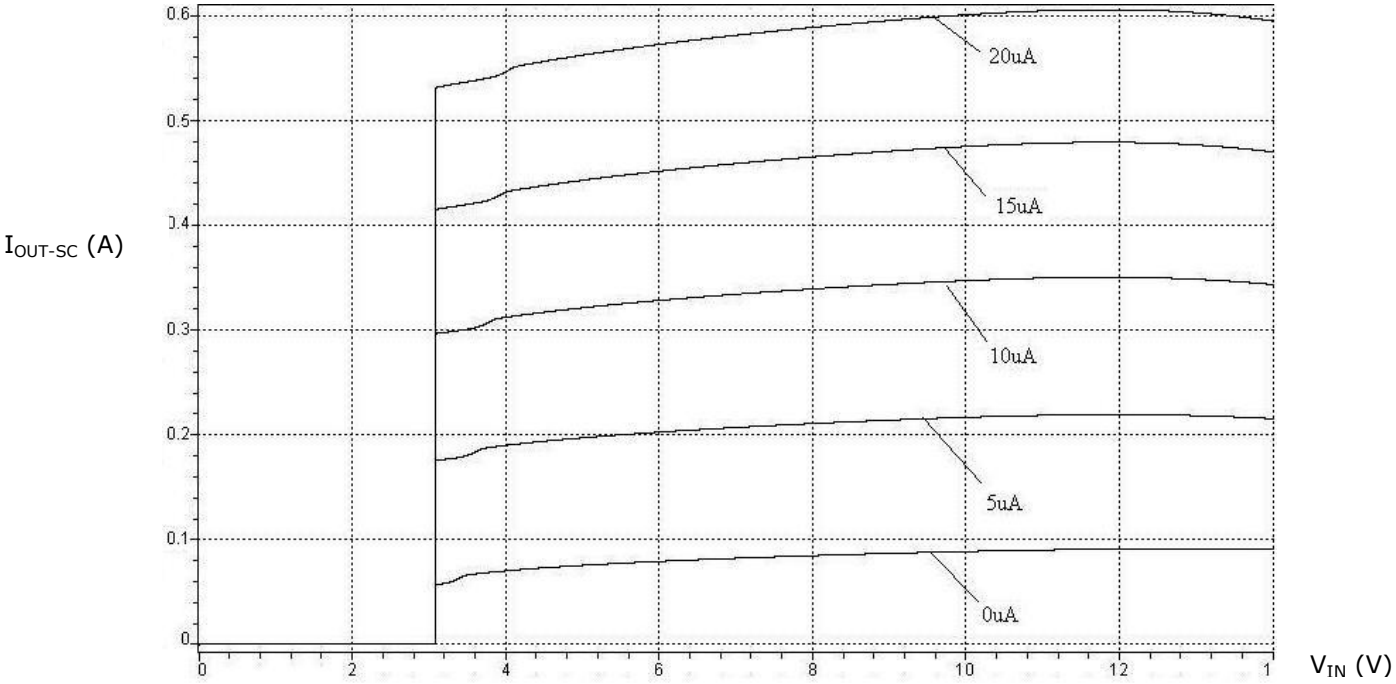


Fig. 4. Simulated current limit of LDO (for R_L = 0) versus V_{IN} for IR_{EXT} values of 0, 5, 10, 15, and 20 µA.

Measurement Results

The circuit used to test out the proposed technique was fabricated in a triple-metal 0.5-µm standard 16-V CMOS process. The circuit area was 1.3 mm^2, including the trimming circuitry used to bring V_{ADJ} within the target accuracy of ±1%. As mentioned, the recommended input-voltage range of the LDO was between 4 V and 14 V, while the reference voltage was 1.25 V. The output voltage of the LDO could be externally programmed between 1.25 V and 12 V using two resistors.

The measurements show that good performance levels can be attained. Fig. 5, which represents VR_{EXT} versus V_{IN} for different IR_{EXT} current values, is almost exactly the same as the simulated graphs from Fig. 3. Furthermore, line regulation is in fact much better—reaching no more than 3 mV for V_{IN} between 4 V and 14 V. Load regulation is also close to that described in the simulations. Fig. 6 shows the measurement results of the LDO output short-circuit current I_{OUT-SC} versus V_{IN}, for different R_{EXT} values.

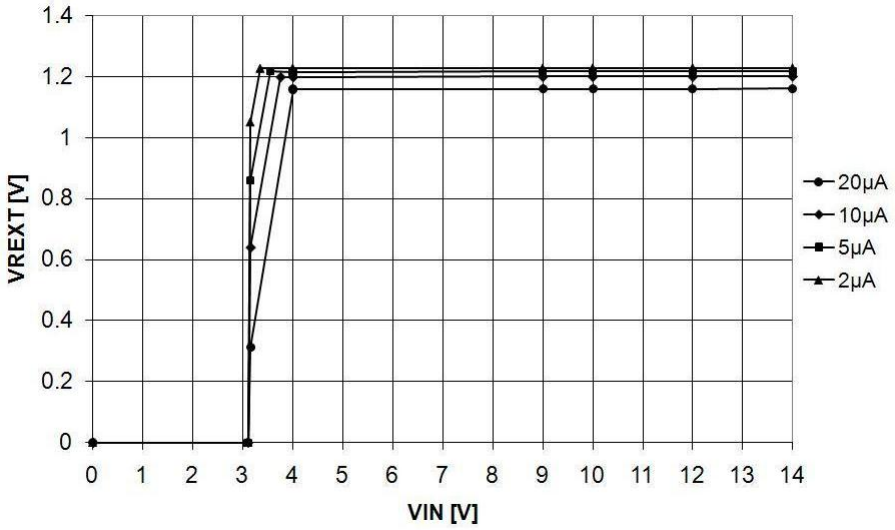


Fig. 5. Measured VR_{EXT} versus V_{IN} for IR_{EXT} values of 2, 5, 10, and 20 µA.

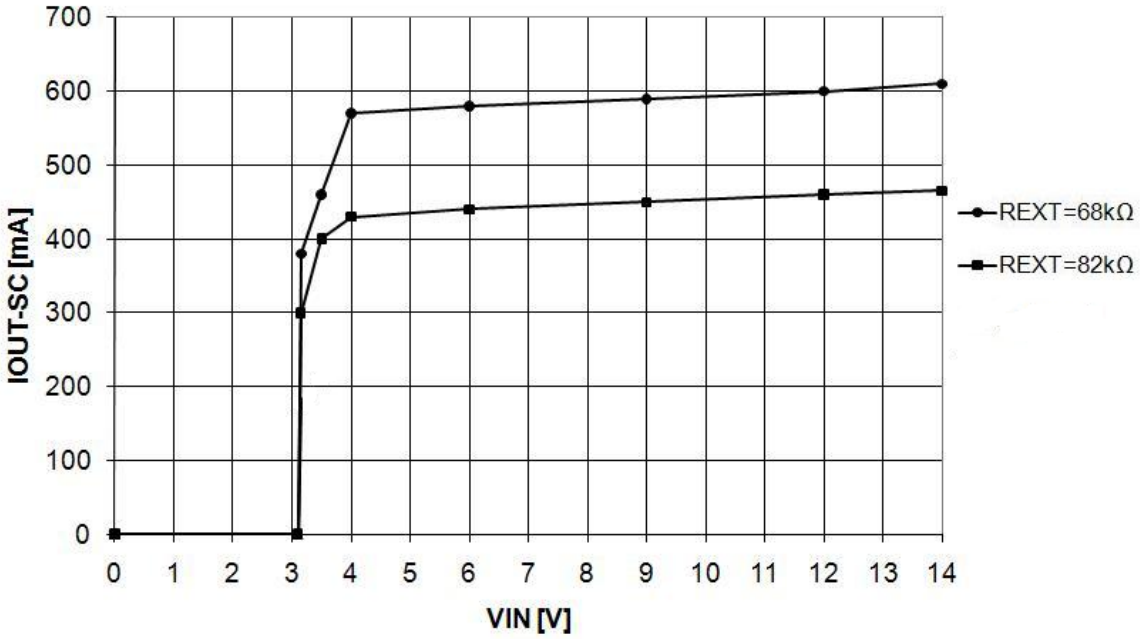


Fig. 6. Measured I_{OUT-SC} versus V_{IN} for R_{EXT} values of 68 kΩ and 82 kΩ.

For V_{OUT} = 6.5 V (obtained through the external feedback network), R_{EXT} = 82 kΩ, and V_{IN} = 7 V, the measured transient load regulation, at a full 1-mA to 300-mA load-current step with rise/fall times of 1 µs, is looking like that shown in Fig. 7, proving that the circuit is quite fast.

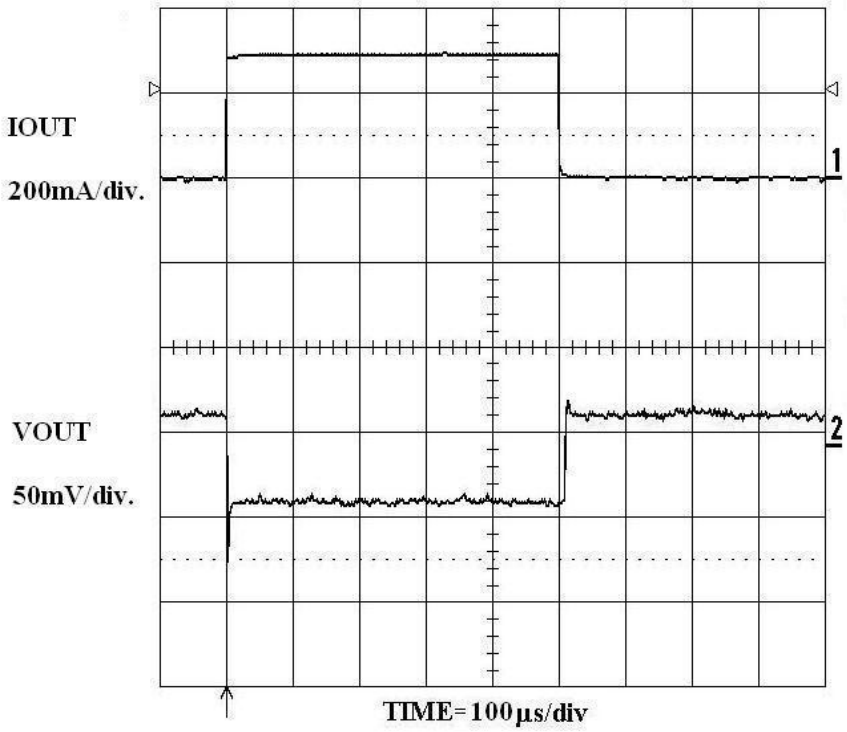


Fig. 7. Measured transient load regulation: I_{OUT} and V_{OUT} versus time.

Conclusions

Implementation of an external control technique for the current limiting of LDOs, such as the one described here, offers a high degree of flexibility to design engineers. This approach allows designers to choose the optimum current for their specific circuit design simply by changing the value of an external resistor.

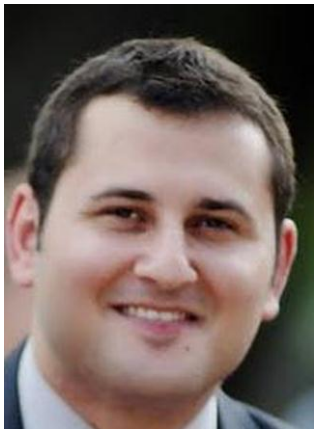
The voltage available at this additional pin on the LDO is regulated through a voltage buffer connected to the internal V_{REF}. When R_{EXT} = 68 kΩ, it establishes a current limit of up to 0.6 A. Meanwhile, for applications with 0.3-A maximum continuous current, the best choice is to have a current limit around 0.45 A, which can be obtained by using R_{EXT} = 82 kΩ.

Theoretical considerations, simulations and experimental results all indicate the validity of the proposed technique, that it is fully functional, and that the LDO has a fast load-transient response at a full 1-mA to 300-mA load current step. The proposed LDO consumes only 100 µA (160 µA at full load) and has a dropout voltage of 200 mV at 300 mA (for V_{OUT} = 6.5 V.)

Note: The current-limiting feature described in this article is available on two devices from ON Semiconductor—the CAT6201, a 300-mA LDO and the CAT6202, a 500-mA LDO.

About The Authors

Cornel Stanescu graduated in 1984 with a Master's degree from the Faculty of Electronics of the Politehnica University of Bucharest. In 1998, Stanecu obtained his PhD in Microelectronics. Between 1984 and 1996 he was with ICCE (Development Center for Electronic Components) being involved in analog design, mainly in bipolar technology, developing voltage regulators, precision operational amplifiers and thermal sensors. From 1996 to 1998 he was with SEMICONIX Design, as technical manager for analog ICs. Since 1998, he has been working with the Romanian Catalyst group (now part of ON Semiconductor) as a design manager or technical lead for digital potentiometers, LDOs and thermal sensors, all in CMOS technology. Since 1984, Stanecu has been a visiting lecturer at the Faculty of Electronics of "Politehnica" University of Bucharest, teaching, both in Romanian and English languages, Project and Seminary classes at Analog Integrated Circuits course. He is also the main author of five patents (one Romanian and four U.S.) and has more than 30 papers presented at the Romanian Annual Semiconductor Conference (CAS), many recognized with best-of-the-section awards. For the last 10 years, Stanecu has been a member of the Paper Review Board and chairman at the same conference. An IEEE member since 1994, he was also a reviewer for the IEEE Transaction on Circuits and Systems II: Express Briefs.



Cristian Dinca received his Diploma degree and Master's degree in electronic and engineering from the University Politehnica Bucuresti, Romania in 2006 and 2008. Cristian Dinca is currently working at ON Semiconductor Romania as an analog IC designer dealing with low dropout regulators.

Radu H. Iacob is a product design manager at ON Semiconductor, coordinating design and product engineering activities, from concept to market, on various products lines such as non-volatile memories, digital potentiometers and power management circuits. He has been with ON Semiconductor since 2008. Previously, he held the position of design manager at Catalyst Semiconductor, in charge of design and product introduction for EEPROM memories and other mixed-signal products. He was an employee of Catalyst Semiconductor since 1996. Prior to that, Iacob was a research engineer at the Institute of Micro-technology in Bucharest, Romania. Iacob has co-authored over 20 patents and scientific papers, and holds MS and PhD degrees from the Politehnica University of Bucharest.

Profirescu Ovidiu George is a design engineer at ON Semiconductor Romania, with seven years of experience in design, verification and validation of analog integrated circuits. He has actively participated in the development of several LDO product families. George is also involved in academic activities as an assistant professor at the University Politehnica of Bucharest, Electrical Engineering Department where he teaches Electronic Devices and Circuits, TCAD, Device and Process Simulation, using industry-standard simulators and equipment. George graduated from the University Politehnica of Bucharest in 2006 as an "Advanced Microelectronics" Master and also from the University Politehnica of Bucharest in collaboration with Infineon Technologies in 2008. Since 2007 George has been a PhD student.