ISSUE: October 2012

Frequency-Foldback Technique Optimizes PFC Efficiency Over The Full Load Range

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Environmental concerns lead to new efficiency requirements when designing modern power supplies. For instance, the 80 PLUS initiative and its Bronze, Silver or Gold derivatives[1] force desktop and server manufacturers to work on innovative solutions. An important focus is on the power factor correction (PFC) stage which, combined with the EMI filter, can consume 5% to 8% of the output power at low line, full load.

In general, however, power supplies for computing and other applications do not operate continuously at their maximum power. In actual use, these supplies are typically called on to deliver full load only for short periods of time. That's why "green requirements" such as 80 PLUS, which intend to maximize power savings, do not simply establish goals for full-load efficiency. Instead, they target the actual power supply operating conditions by specifying minimum levels for either the average efficiency or for the efficiency under different load conditions such as 10%, 20%, 50% and 100% of full power.

As a result, it has become critical that power supply designers address medium- and light-load efficiency. In terms of the design of the PFC stage, a popular approach to lowering losses under these load conditions has been to reduce the switching frequency—a method known as frequency foldback. While extremely efficient at very low power, this solution must be carefully implemented at intermediate power levels.

This article intends to clarify how the switching frequency should be managed in a PFC boost converter in order to achieve optimum efficiency. To that end, the converter's MOSFET losses are analyzed under critical conduction and discontinuous conduction modes of operation. This discussion then sets the stage for explaining the operating principles behind a relatively new method of frequency reduction known as current-controlled frequency foldback (CCFF).

The CCFF technique, which is of great help in optimizing PFC efficiency across the load range, has been implemented by ON Semiconductor in controllers such as the NCP1611. This article discusses the operation of these controllers and presents experimental results for CCFF with comparisons to other frequency-control methods. For further perspective on how the CCFF technique compares with existing methods for optimizing PFC efficiency, see "The Evolution of Current-Controlled Frequency Foldback" in the appendix at the end of this article.

Critical- or Discontinuous-Conduction Mode

Switching losses are difficult to accurately predict. However, we can assess the loss trend based on the operating mode as a PFC boost converter transitions from critical-conduction mode (CrM) to discontinuous-conduction mode (DCM).

Fig. 1 shows the MOSFET current in both modes for the same power and line conditions (i.e., for the same line current.)

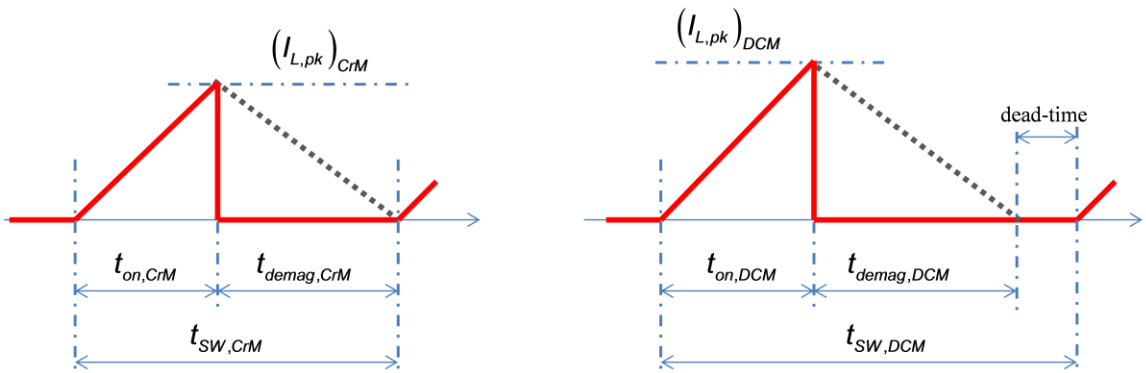

Fig. 1. MOSFET current in CrM (left) and DCM (right).

Whatever the mode is, the line current is the averaged value of the inductor current over the switching period, the averaging process being performed by the EMI filter of the PFC boost converter.

In CrM, the line current is simply (see note below):

$$I_{line} = \frac{\left(I_{L,pk}\right)_{CrM}}{2} \quad . \tag{1}$$

In DCM, the inductor current is zero for the dead-time. Its averaged value hence depends on the current cycle duration (on-time + demagnetization time) over the switching period as follows:

$$I_{line} = \frac{\left(I_{L,pk}\right)_{DCM}}{2} \cdot \left(t_{on,DCM} + t_{demag,DCM}\right) \cdot f_{SW,DCM} \quad . \tag{2}$$

The PFC circuit regulates the line current with respect to the power to be delivered and the line magnitude. Hence, whatever the mode, the same current is absorbed from the line. Frequency-clamped circuits increase the on-time and hence the peak inductor current when dead-times are necessary to clamp the frequency. If not, the averaged value of the inductor current would be reduced and the line current that results from the averaging of this inductor current would be distorted.

Hence, Fig. 1 shows a higher peak current in DCM to compensate for the dead-time when no current is absorbed from the mains. Let's write that when operating in DCM operation, the switching frequency is reduced by a ratio α:

$$\alpha = \frac{f_{SW,CrM}}{f_{SW,DCM}} \geq 1 \quad . \tag{3}$$

As previously mentioned, the on-time is multiplied by a factor m $\left(m > 1\right)$ compared to its CrM level to maintain the equivalent power delivery. Thus, both the inductor peak current and the current cycle duration are multiplied (on-time + demagnetization time):

$$\left(I_{L,pk}\right)_{DCM} = \left(I_{L,pk}\right)_{CrM} \cdot m \tag{4}$$

and

$$t_{on,DCM} + t_{demag,DCM} = m \cdot \left(t_{on,CrM} + t_{demag,CrM}\right) \quad . \tag{5}$$

Thus, equating the CrM and DCM averaged current values leads to:

$$\frac{\left(I_{L,pk}\right)_{DCM}}{2} \cdot \frac{t_{on,DCM} + t_{demag,DCM}}{T_{SW,DCM}} = \frac{\left(I_{L,pk}\right)_{CrM}}{2} \quad \Rightarrow \quad m^2 \cdot \frac{T_{SW,CrM}}{T_{SW,DCM}} = 1 \quad . \tag{6}$$

Note: At the end of the demagnetization time, the MOSFET drain-source voltage swings around the input voltage as a result of the oscillating network consisting of the inductor and the switching-node capacitor. For minimizing the switching losses, the MOSFET is generally not turned on as soon as the core is reset but delayed until the MOSFET drain-source is at its minimum (so-called valley switching.) For the sake of simplicity, we will neglect this delay in the upcoming analysis.

From (6), we can deduce that:

$$m = \sqrt{\alpha} = \sqrt{\frac{f_{SW,CrM}}{f_{SW,DCM}}} \quad . \tag{7}$$

Finally, we obtain the following DCM magnitudes:

$$\frac{f_{SW,DCM}}{f_{SW,CrM}} = \frac{1}{\alpha} \tag{8}$$

and

$$\frac{t_{on,DCM}}{t_{on,CrM}} = \frac{\left(I_{L,pk}\right)_{DCM}}{\left(I_{L,pk}\right)_{CrM}} = \sqrt{\alpha} \quad . \tag{9}$$

We can add the MOSFET duty-ratio that is the on-time multiplied by the switching frequency:

$$\frac{d_{DCM}}{d_{CrM}} = \frac{1}{\sqrt{\alpha}} \quad . \tag{10}$$

We can show that the MOSFET conduction losses (CrM) over one switching period are:

$$\left(P_{cond}\right)_{CrM} = R_{DS(on)} \cdot \frac{\left(I_{L,pk}\right)_{CrM}^{2}}{3} \cdot d_{CrM} \quad . \tag{11}$$

Similarly, the DCM conduction losses can be expressed as follows:

$$\left(P_{cond}\right)_{DCM} = R_{DS(on)} \cdot \frac{\left(I_{L,pk}\right)_{DCM}^{2}}{3} \cdot d_{DCM} = \left(P_{cond}\right)_{CrM} \cdot \sqrt{\alpha} \quad . \tag{12}$$

We can estimate the switching losses as the sum of the MOSFET turn-off losses (first term of below equation) and the MOSFET turn-on losses (discharge of the switching-node capacitor often designed as the lump capacitor attached to the drain of the MOSFET) as follows:

$$\left(P_{sw}\right)_{CrM} = \left(k_1 \cdot \left(I_{L,pk}\right)_{CrM} \cdot f_{CrM}\right) + \left(k_2 \cdot Q_{rss} \cdot f_{CrM}\right) \quad . \tag{13}$$

The switching losses depend on so many different parameters (MOSFET and diode choice, parasitic elements, gate-drive current capability, etc.) that in practice, the computation cannot be effectively made. K_1 and K_2 are constants that take into account these "unknown" parameters.

Similarly, we can define the DCM switching losses as follows:

$$\left(P_{sw}\right)_{DCM} = \left(k_1 \cdot \left(I_{L,pk}\right)_{DCM} \cdot f_{DCM}\right) + \left(k_2 \cdot Q_{rss} \cdot f_{DCM}\right) = \left(\frac{k_1 \cdot \left(I_{L,pk}\right)_{CrM} \cdot f_{CrM}}{\sqrt{\alpha}}\right) + \left(\frac{k_2 \cdot Q_{rss} \cdot f_{CrM}}{\alpha}\right) \quad . \tag{14}$$

In others words, the MOSFET turn-off losses are reduced by $\sqrt{\alpha}$ while the turn-on ones are reduced by α. As the relative importance of these losses cannot be predicted (even if the second ones are more dominant at light load since they are independent of the power level), we can consider for a worst-case analysis (worst case for DCM) that the DCM switching losses are reduced by at least $\sqrt{\alpha}$ compared to the CrM switching losses.

As a matter of fact, the DCM losses can be expressed as a function of the CrM ones:

$$P_{DCM} = \left(P_{cond}\right)_{DCM} + \left(P_{sw}\right)_{DCM} = \left(\left(P_{cond}\right)_{CrM} \cdot \sqrt{\alpha}\right) + \frac{\left(P_{sw}\right)_{CrM}}{\sqrt{\alpha}} \quad (15)$$

where $\alpha = \frac{f_{SW,CrM}}{f_{SW,DCM}} \geq 1$.

As we could expect, the frequency decrease leads to an increase of the conduction losses and to a decrease of the switching ones. There must then be optimal conditions to enter frequency foldback.

The derivative of the above P_{DCM} expression can help estimate this optimum as a function of the ratio $\left(\beta = \frac{\left(P_{cond}\right)_{CrM}}{\left(P_{sw}\right)_{CrM}}\right)$ according to:

$$\frac{d}{d\alpha}\left(P_{DCM}\right) = \frac{\left(P_{cond}\right)_{CrM}}{2 \cdot \sqrt{\alpha}} - \frac{\left(P_{sw}\right)_{CrM}}{2 \cdot \alpha^{3/2}} . \quad (16)$$

It then starts to be efficient to reduce the switching frequency when in CrM, the switching and conduction losses are equal, with an optimal benefit when α equates to the following α_{max} term:

$$\alpha_{max} = \frac{1}{\beta} = \frac{\left(P_{SW}\right)_{CrM}}{\left(P_{cond}\right)_{CrM}} . \quad (17)$$

In practice, the switching frequency can be reduced a bit more since a worst case is considered to express the DCM savings: the DCM gain on the turn-on losses has been purposely minimized to simplify analysis.

Fig. 2 displays the DCM losses as a percentage of the CrM losses obtained in the absence of frequency foldback. The DCM over CrM losses are computed based on equation (15), ratio α sweeping from 1 to 10. When α is unity, the frequency is not reduced and hence, the DCM and CrM losses are the same leading to 100%. For higher α values, the percentage rises when DCM worsens the efficiency and conversely, decays when frequency foldback improves the efficiency. In other words, frequency foldback is welcome when the ratio P_{DCM}/P_{CrM} is below 100%.

In Fig. 2, several cases are considered for the ratio of CrM conduction losses over CrM switching losses $\left(\beta = \frac{\left(P_{cond}\right)_{CrM}}{\left(P_{sw}\right)_{CrM}}\right)$:

- Conduction and switching losses are the same leading to a ratio of 1 (brown trace)
- β is 50%, i.e., the conduction losses are half the switching ones (green trace) and
- Three cases for which the conduction losses are small compared to the switching losses, resulting in the following low ratios:

- β = 20% (purple trace)
- β = 10% (blue trace) and
- β = 1% (orange trace).

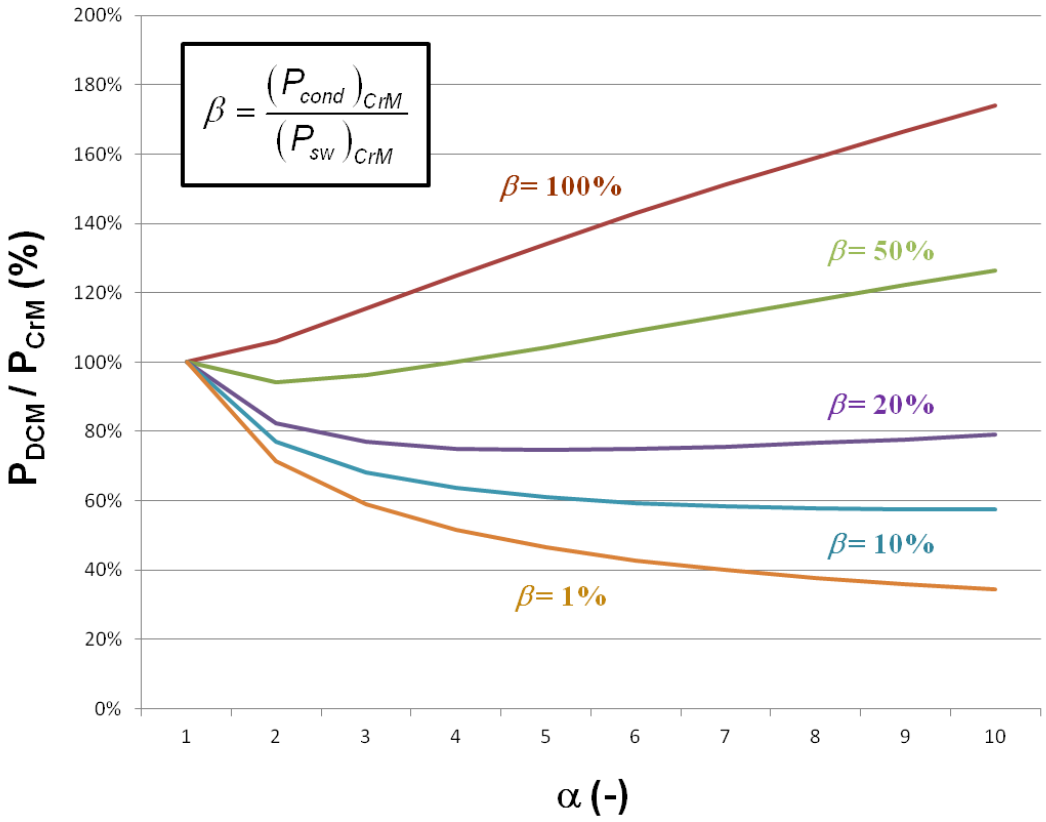

Fig. 2. DCM losses as a percentage of the CrM losses with respect to the $\alpha = f_{CrM}/f_{DCM}$ ratio.

Fig. 2 shows that:

- When the conduction losses are higher or in the same range, frequency foldback increases the losses (brown trace). This is what happens when large rms currents circulate through the converter as in the heavy-load, low-line conditions of a PFC stage.
- When the conduction losses are slightly smaller compared to the switching losses, a limited reduction of the frequency is desired. It must remain limited however. Otherwise the benefit with regard to switching losses is totally cancelled or cannot compensate for the increase in conduction losses (green and purple traces). This case corresponds to the line and load conditions leading to a medium current within the converter.
- When the conduction losses are very low compared to the switching losses (blue and orange traces), frequency foldback dramatically lowers the overall losses. The switching frequency must therefore be reduced when the line current is small.

It should be noted that the benefit of frequency foldback on the MOSFET switching losses was underestimated ("DCM switching losses are reduced by at least $\sqrt{\alpha}$ compared to the CrM switching losses").

Experimental Data

The following data was obtained using a 2-phase interleaved PFC stage driven by the NCP1631.[2] This controller operates in frequency-clamped critical-conduction mode (FCCrM) and further features a frequency-foldback capability. It should be noted that compared to CCFF (see next section), the clamp frequency does not depend on the current level but is constant at a given power over the current sine wave.

Fig. 3 shows the efficiency of the NCP1631 300-W evaluation board at 10%, 20% and 50% of the load, a 115-V line being applied. The foldback characteristic of the circuit was tweaked to measure the efficiency at three different operating frequencies at 20% of the load and at two frequency conditions for the two other working points under consideration. The data below confirms that the efficiency improves at light load when the frequency decays and degrades if the switching frequency is diminished at a heavier load.

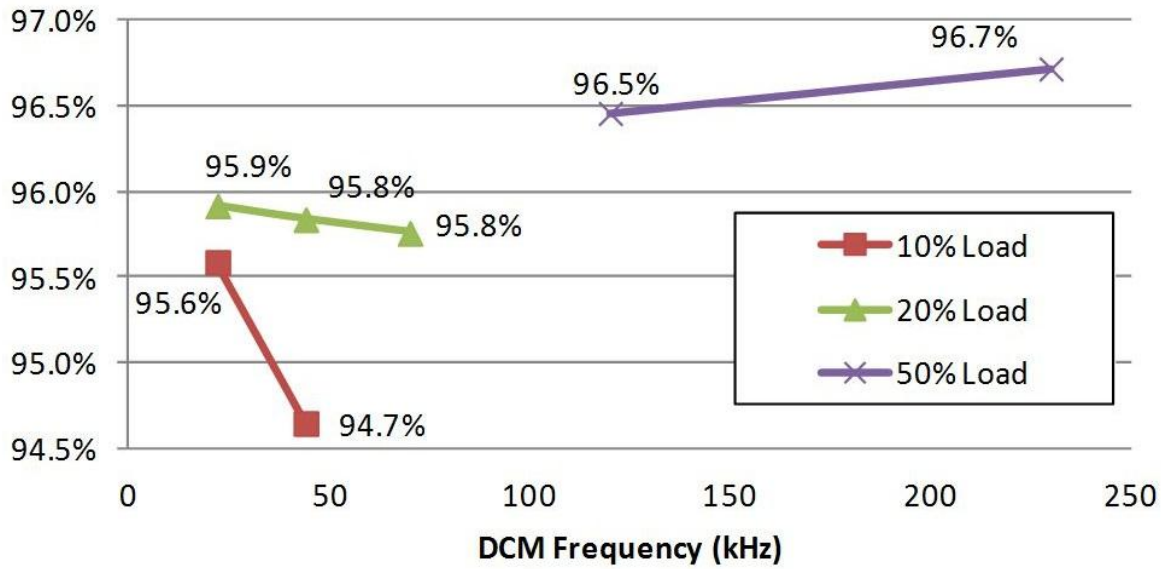

Fig. 3. Efficiency versus frequency at 115 V rms. The frequency clamp level influences efficiency.

Current-Controlled Frequency Foldback

Targeting light-load efficiency requirements, ON Semiconductor has released the NCP1611 and NCP1612, which are PFC boost controllers that operate in a current-controlled frequency foldback (CCFF) mode. In this mode, the PFC stage operates in traditional critical-conduction mode (CrM) when the line current exceeds a programmable value. Conversely, when the current is below this preset level, the switching frequency decays down towards about 20 kHz as the line current reduces to zero.[3,4]

In practice, the line current is measured indirectly. These controllers monitor the line voltage and an internal computation generates a current on an FFcontrol pin, which together with an external resistor builds a signal representative of the line current. When this voltage ($V_{FFcontrol}$) exceeds the internal 2.5-V internal reference (V_{REF}), the circuit operates in critical-conduction mode. Hence, the external resistor controls the minimal line current for CrM operation. Conversely, if the FFcontrol pin voltage ($V_{FFcontrol}$) is below 2.5 V, a dead-time is generated that approximately equals

$$\left(66\,\mu s \cdot \left(1 - \frac{V_{FFcontrol}}{V_{REF}}\right)\right).$$

In this way, the circuit forces a longer dead-time when the line current is small and a shorter one when the line current is larger. In addition, the circuit skips cycles whenever the FFcontrol pin is below 0.65 V to prevent the PFC stage from operating near the line zero crossing where the power transfer is particularly inefficient.

The CCFF operation is summarized by Fig. 4.

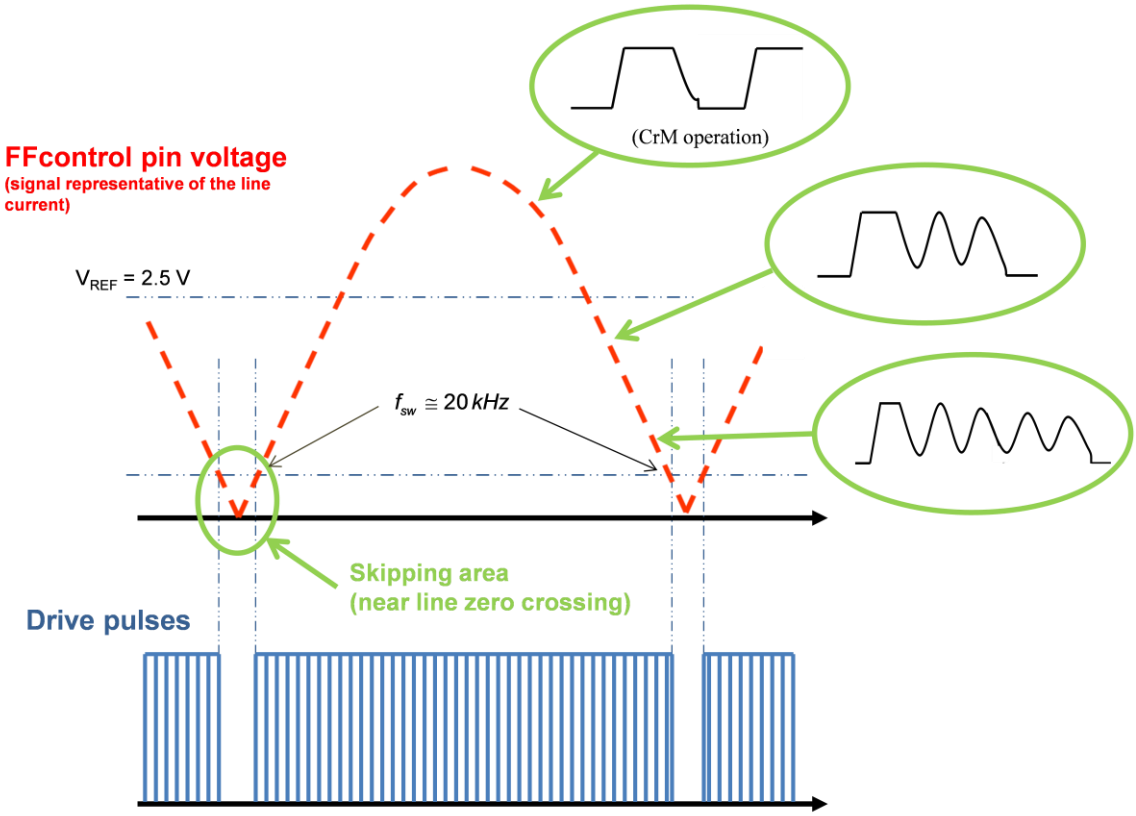

Fig. 4. Key waveforms for the PFC boost controller operating under current-controlled frequency foldback.

Clamping the switching frequency of a CrM PFC boost converter normally leads to a distorted line current since traditional current shaping schemes assume critical-conduction-mode operation. This traditional limitation is solved in the NCP1611 and the NCP1612 in the same way as in FCCrM circuits from ON Semiconductor (NCP1605 for instance): a circuit (designated as the V_{TON} processing block) is integrated that modulates the on-time to compensate for the presence of dead times. This block is based on an integrator (see data sheet for more details) whose time constant is nearly 100 µs for a proper filtering of the switching ripple.

As illustrated in Fig. 5, under heavy line-current conditions, a CCFF boost stage is intended to operate in CrM and as the line current reduces, the controller enters DCM operation. By the way, even in DCM, the MOSFET turn-on is stretched until its drain-source voltage is at its valley for optimal power savings.

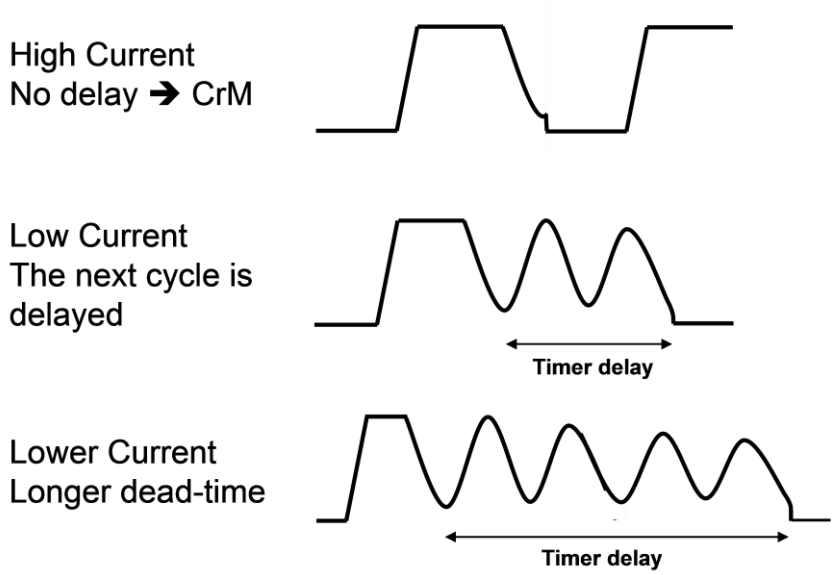

Fig. 5. CCFF operation.

The CCFF technique further leads to stable operation without hesitation between valleys (Fig. 6.)

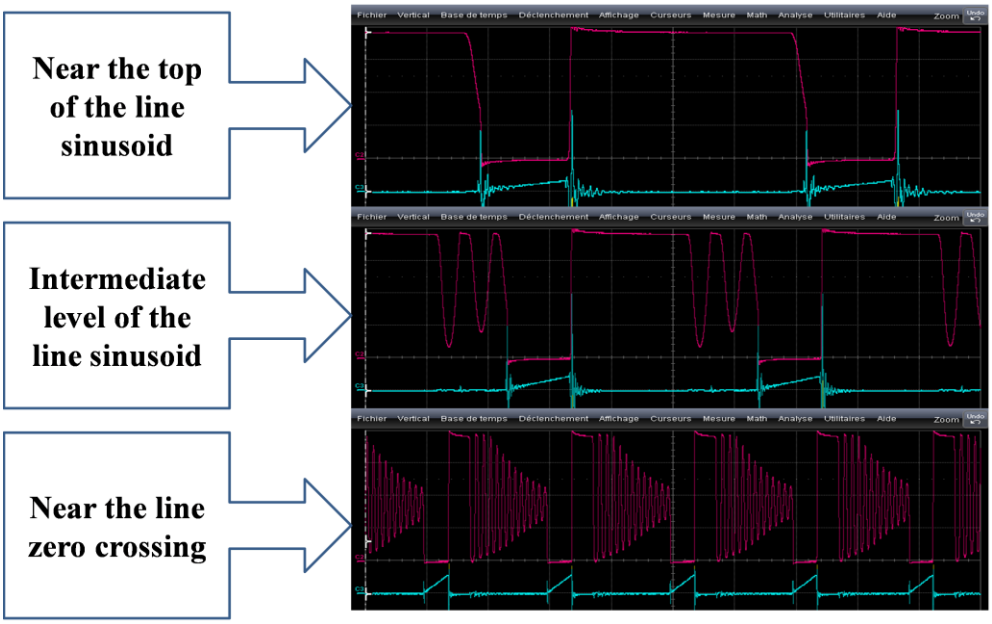

Fig. 6. Operation at 230 V, 160 W near the line zero crossing of the NCP1612 evaluation board. The MOSFET drain-source voltage is in red, while the MOSFET current is the blue trace.

CCFF Flattens The Efficiency Over Load Characteristics

Tests have been made on the NCP1611 evaluation board.[3] This is the slim (< 13 mm) PFC stage designed to provide 160 W while operating from a wide input-voltage range (Fig. 7.)

Fig. 7. Wide mains, 160-W PFC stage.

This board is designed to run in CCFF. However, it can be easily operated in CrM by forcing the signal representative of the line current above 2.5 V to disable the CCFF frequency-foldback characteristic. Also, the skip-cycle capability inherent to CCFF operation can be disabled by preventing the signal representative of the line current from dropping below 0.65 V. This versatility allows for testing operation of the PFC stage in three modes—CrM, CCFF and non-skipping CCFF—allowing perfect, apples-to-apples comparisons to be performed on the same application schematic with the same external power components.

A fair comparison also requires avoiding configurations that exaggerate the effects in one mode when a better tailored solution is possible. This board is designed to be either self-powered or powered by an external voltage source. For the efficiency measurements, the second option is preferred because the consumption of the charge pump implemented to feed V_{CC} in the self-powered option is proportional to the switching frequency. Keeping it would dramatically affect the light-load CrM efficency. For instance, when measured at high line and 20% load, this charge pump reduced efficiency by 1% in CrM even though it did not significantly affect CCFF performance.

When the PFC stage is plugged in, a large inrush current charges the bulk capacitor. The board includes an NTC protection device to limit this inrush current. However, this NTC has been shorted for the efficiency measurements.

Fig. 8 reports the efficiency measured at low and high line over a wide power range (from 5% to 100% of full load.) The right-hand side of the CCFF efficiency curves resembles that of a traditional CrM PFC stage. Then, on the left-hand side of these curves, the efficiency drops as it would under CrM operation because of the switching losses. However, unlike in a traditional CrM PFC stage, these curves reach an inflection point where they rise up again as a result of the CCFF operation.

As previously described, CCFF makes the switching frequency decay linearly as a function of the instantaneous line current when it goes below a preset level. The CCFF threshold was set to about 20% of the maximum line current at low line and to nearly 45% of the max line current at high line as confirmed by the aforementioned inflection points observed in Fig. 8.

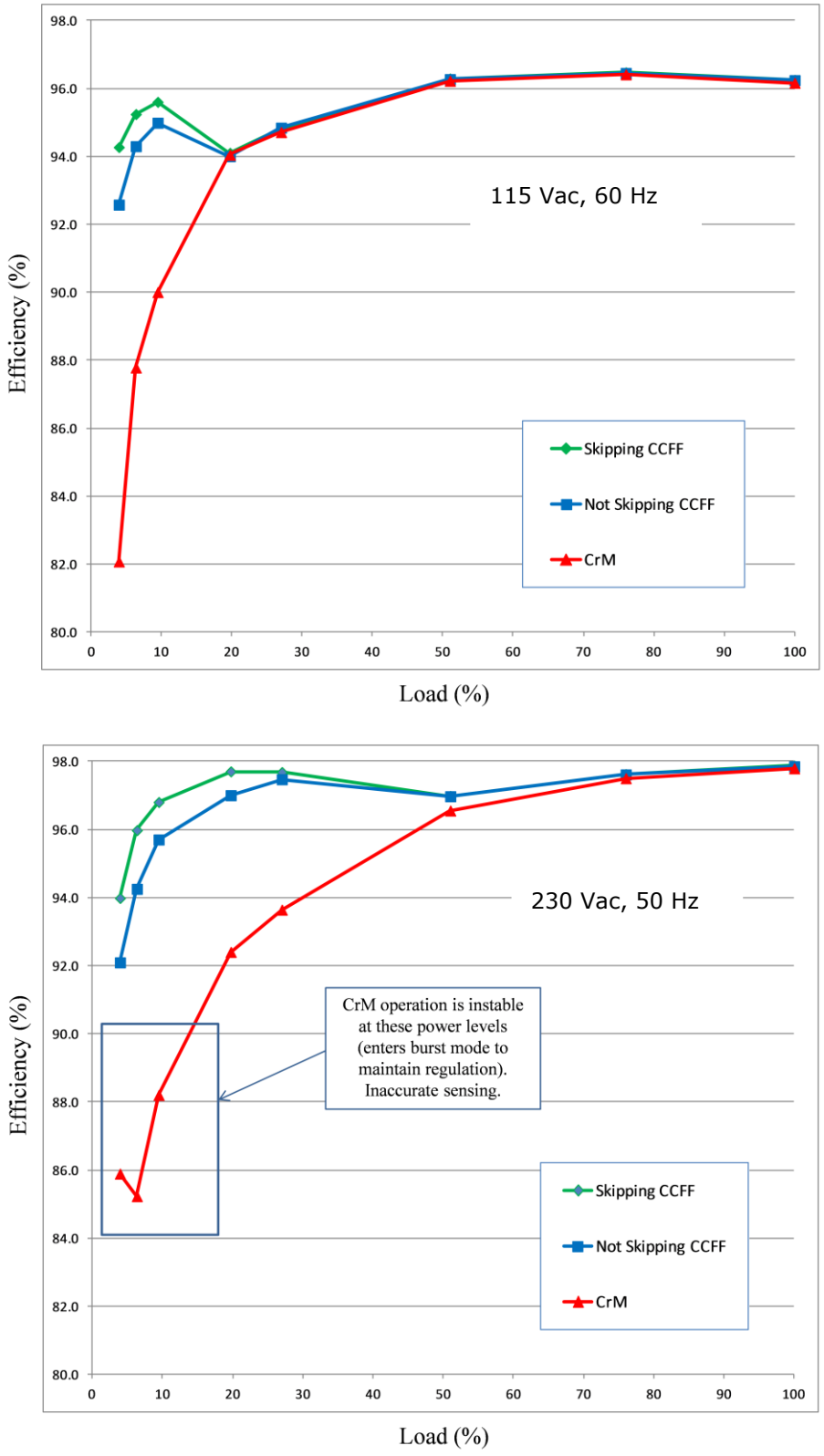

Fig. 8. Efficiency over the load range under low-line (top graph) and high-line (bottom graph) conditions.

Recall that CCFF works as a function of the instantaneous line current: when the signal representative of the line current (generated by the FFcontrol pin) is lower than 2.5 V, the circuit reduces the switching frequency. This is the case near the line zero crossing whatever the load is. Hence, the switching frequency reduces at the lowest values of the line sinusoid even under heavy-load conditions. That is why the efficiency is also improved when the load is high, at least at high line where CCFF has a higher impact since the line current is less.

When the instantaneous line current tends to be very low (below about 5% of its maximum level in our application—see reference 3), the circuit enters a skip-cycle mode. In other words, the circuit stops operating at a moment when the power transfer is particularly inefficient. Compared to CCFF operation without skipping, skip-cycle mode further improves the efficiency under light loads (efficiency increases by 2% at high line and 5% load.)

In general, Fig. 8 illustrates that CCFF significantly improves efficiency below 20% of the full load at low line input. But as the figure also shows, the benefit of CCFF is even more dramatic under high-line conditions. When the converter operates with 230-V input, the efficiency improvement produced by CCFF starts to occur at 50% of full load.

It should be noted that the total harmonic distortion is affected by the skip-cycle mode function. Even if it remains relatively low, skip mode should be inhibited when superior THD performance is desired. Refer to the NCP1611/2 evaluation board manual for PF and THD data.

It is well known that CrM systems generally fail to operate continuously at high line, light load because of the high operating switching frequency. Instead, they enter a burst mode. This often occurs in the 0% to 20% load range when operating at the highest line levels. Fig. 8 illustrates that reducing the switching frequency solves this limitation. Thus, in addition to its other benefits, CCFF offers the possibility that the PFC boost converter can achieve stable operation down to extremely low power levels.

Conclusion

Computing the switching losses of a PFC boost converter is a difficult exercise. Instead, this article has described a way to predict the trends in DCM losses as a function of CrM losses, with respect to the frequency reduction. The analysis and the experimental data show that frequency foldback is preferred when conduction losses are small compared to switching losses, that is, when the line current is low. Fig. 2 even suggests that the lower the line current, the lower the optimal frequency, making a connection between the "efficient frequency" and the line current as the CCFF technique does.

Experimental data confirms that CCFF maintains high efficiency over an extended power range under both low- and high-line conditions. More specifically, for loads ranging from 5% to 100%, efficiency remains above 94% if skip-cycle mode is enabled while the efficiency floor (obtained at 5% of the load) drops to 92% when skip-cycle mode is disabled.

References

1. 80plus program, http://www.plugloadsolutions.com/About.aspx
2. NCP1631 data sheet and application notes, http://www.onsemi.com/PowerSolutions/product.do?id=NCP1631
3. NCP1611 data sheet and application notes, http://www.onsemi.com/PowerSolutions/product.do?id=NCP1611
4. NCP1612 data sheet and application notes, http://www.onsemi.com/PowerSolutions/product.do?id=NCP1612

Appendix: The Evolution Of Current-Controlled Frequency Foldback

Energy regulatory agencies aim to limit the energy consumption of electrical devices under real-world operating conditions. Therefore, the so-called "green" specifications establish requirements for high efficiency not only at full load but over an extended power range. Therefore, in products where power factor correction (PFC) stages significantly contribute to system performance, the PFC stage must remain efficient under medium- and light-load conditions.

Normally, the efficiency of a PFC stage drops at light load. In the case of a multiphase PFC boost converter, selected PFC phases (or channels) can be disabled when the power demand diminishes so that the active branches operate in efficiency-friendly load conditions. As an example, some interleaving circuits feature a phase-shedding function that disables one out of the two channels in light load.

However, the approach is different with a single-phase PFC stage. In this case, the PFC boost converter generally clamps the switching frequency to limit the switching losses that dominate under light-load conditions. With the continuous-conduction mode (CCM) circuits preferred in high-power applications, this is inherent since they generally operate in fixed frequency. But in critical-conduction mode (CrM), a clamp is added to prevent the switching frequency from soaring. Named frequency-clamped critical-conduction mode (FCCrM) within ON semiconductor, this capability is enhanced by decreasing the clamp value as the load decreases (frequency foldback.) For example, this high-efficiency solution is used in NCP1631-driven interleaved PFC stages.

An evolution of this technique is the current-controlled frequency foldback (CCFF) scheme where, instead of the output power, the line current controls the frequency characteristic. The line current is representative of the rms current flowing through the PFC stage and hence its conduction losses. Thus, the lower the line current is, the more dominant the switching losses are and the lower the frequency level is to be set for maximum efficiency. On this basis of this idea, CCFF forces CrM operation when the line current is above a preset value and gradually reduces the frequency when it drops below this threshold (including at heavy load near the line zero crossing) for optimal power savings.

About The Author

Joel Turchi holds an engineering degree from the ENSEEIHT school, which is part of the National Polytechnic Institute of Toulouse. With 20 years of power supply design experience at Motorola and ON Semiconductor, Joel is a regular contributor of application notes for ON Semiconductor as well as articles for trade magazines. He holds 12 issued U.S. patents pertinent to control techniques, whereas six others are pending. Joel has originated several new concepts in the power conversion arena through the introduction of PWM and PFC controllers. Among these circuits are notable devices such as the MC44608 controller for flyback converters with secondary reconfiguration, the NCP1653 CCM PFC controller and the NCP1631 interleaved PFC controller.

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