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Process, Packaging Combine To Advance High-Voltage Power MOSFETs

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There's a significant amount of design activity today in power management involving voltages between 400 V and 1700 V, with the bulk of interest around 600 V at 2 kW. Applications include switched-mode power supplies (SMPSs), motor control, industrial machines, electric and hybrid electric vehicles (EVs/HEVs), backup power systems and, of course, renewable power sources such as photovoltaic and wind generators.

To make these designs attractive and viable to the market, the end products have to be smaller and more efficient, which places tremendous demands on the power-handling components, especially the MOSFETS. Semiconductor vendors are using two primary approaches to meet these requirements.

First, they are improving their process technology, which reduces on-resistance (R_{DSon}) and thus loss. Such I^2R loss is inefficient and obviously an immediate waste of input (source) power. However, it has another critical consequence: it also results in heat, which must then be dissipated. Thus, I^2R loss impacts overall product design and packaging, often requiring heat sinks, fans, cooling assemblies, operating restrictions, and a larger enclosure.

The other way semiconductor vendors are improving MOSFET performance is through the development of better packaging. New packages allow for smaller MOSFETs than existing standard packages, while offering comparable or better critical characteristics. These packages offer improvements in physical, electrical, and thermal parameters, thus giving system designers more flexibility along with superior performance.

This article discusses two examples of recent advances in MOSFET process technology and packaging by STMicroelectronics—the MDmeshV process and the HV PowerFLAT 8×8 package. Data is presented to illustrate the improvements in device performance made possible by these process and packaging innovations.

Planar Vs. Nonplanar FETs

Most MOSFETs in this power range use a planar structure (see Fig. 1), where the device structure is built in a single plane with the source and gate on top, and the drain below.

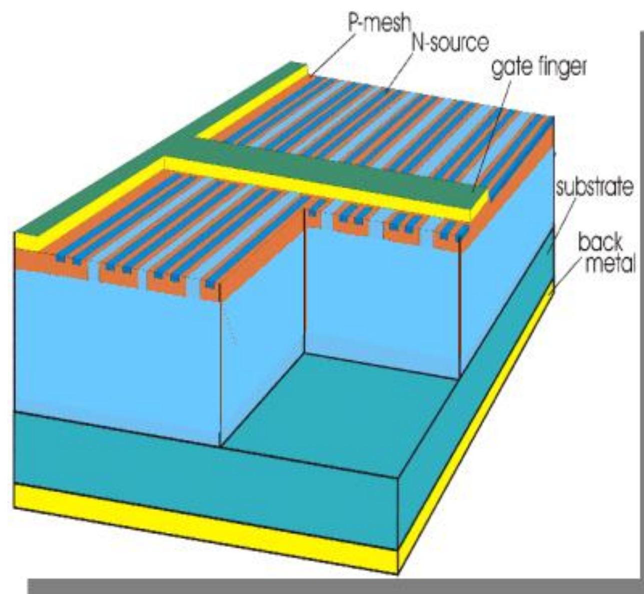

Fig. 1. A cross section of the conventional MOSFET structure shows its planar, layered construction.

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In contrast, the superjunction structure (first introduced in the late 1990s) is a multilayer process where the junction is inside the silicon (Fig. 2.) This structure introduces extra charge carriers, and reduces the channel resistance dramatically.

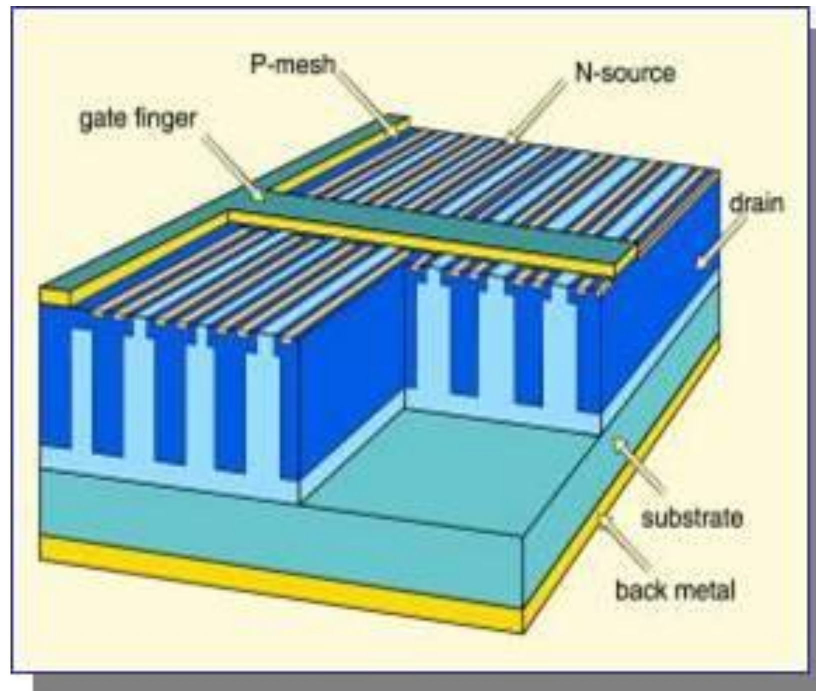

Fig. 2. A cross section of the superjunction MOSFET structure shows its vertical construction. Note how the drain reaches down towards the substrate.

The performance of this vertical structure is seen in the STW88N65M5, a 650-V n-channel device fabricated in the MDmeshV process, the newest improvement of the superjunction process. In the standard TO-247 package, $R_{DS(ON)}$ is just 0.029 Ω (maximum) at a drain current I_D of 84 A, versus 0.037 Ω for the closest comparable competitive device. Similar reductions in on-resistance are achieved in the D^2PAK (220 mΩ versus 250 mΩ) and the TO-220 (63 mΩ versus 74 mΩ.)

The lower on-resistance of MOSFETs manufactured in MDmeshV is attributed to a combination of enhancements in the technology. A reduction in drain-column pitch by means of a more-effective diffusion process and improvement in the body-column structure have led to an improvement in the $R_{DS(ON)}$ x area product for MdmeshV compared to previous generations.

Meanwhile, gate charge is also reduced, with a corresponding improvement in switching time and performance. The typical Q_g of the STW88N65M5 is 204 nC, compared to 330 nC for the nearest competitive device. The gate charge number, while impressive, is not as revealing as the actual turn-on and turn-off energy, which is depicted in Figs. 3a and 3b, respectively.

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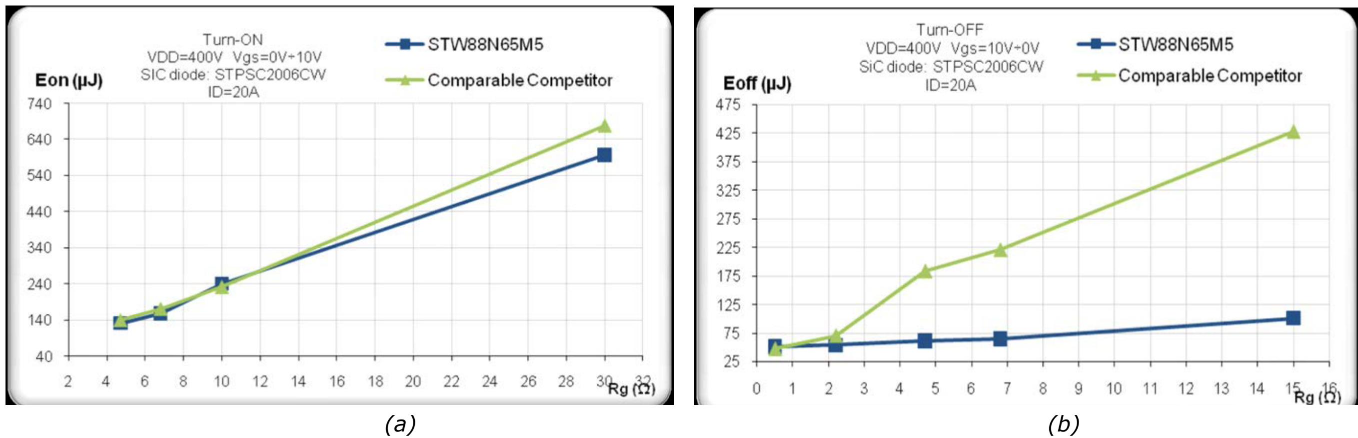

(a) *(b)*

Fig. 3. The turn-on energy (a) and turn-off energy (b) for the STW88N65M5, compared to the closest competitor in this class, shows the improvement in these vital switching-related parameters.

Although the superjunction MOSFET is more complicated to manufacture, it's static and its switching characteristics result in a better MOSFET for the designer.

Packaging Plays A Major Role

The most-common surface-mount packages for MOSFETs in this 2-kW power range are the D^2PAK and DPAK. A newer package, the HV PowerFLAT 8×8, offers major benefits compared to these existing packages (Fig. 4.)

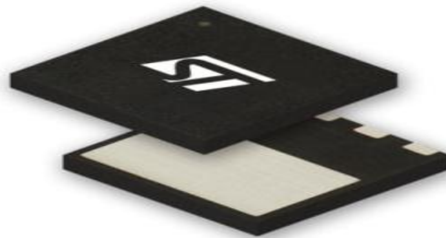

Fig. 4. The HV PowerFLAT 8×8 package is a newer alternative to the standard D^2PAK and DPAK MOSFET housing, with multiple virtues.

First, the new package is thinner, as illustrated in Fig. 5—just 1-mm thick, compared to 4.5 mm and 2.3 mm for the D^2PAK and DPAK, respectively. This thinner profile is a tangible benefit as pc boards are now being spaced closer together, and also intermingled with heat sinks and transformers.

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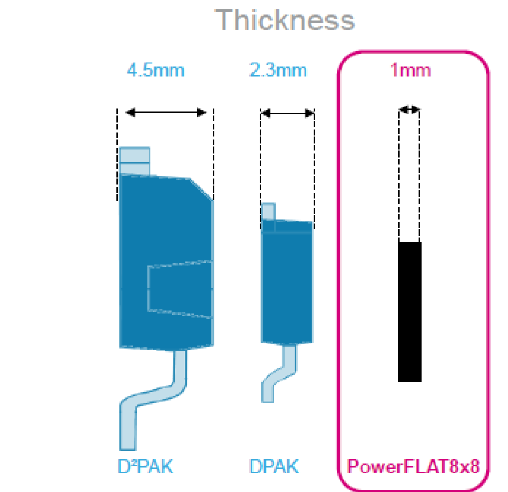

Fig. 5. The 1-mm thickness of the HV PowerFLAT 8×8 is substantially less than existing packages for comparable MOSFETs. Package thickness is increasingly important with today's tight pc-board layouts and spacing.

More significantly, the 8-mm x 8-mm package occupies less than half the PCB footprint of the D^2PAK, requiring just 64 mm^2 in contrast to 150 mm^2 (the DPAK is between those two packages), as shown in Fig. 6. The PowerFLAT package can be handled and placed on the board just like any other surface-mount component, and wave soldered along with the other components. To ease switchover to this package, its contact footprint is compatible with the D^2PAK and DPAK, even as the footprint is smaller (Fig. 6, again.)

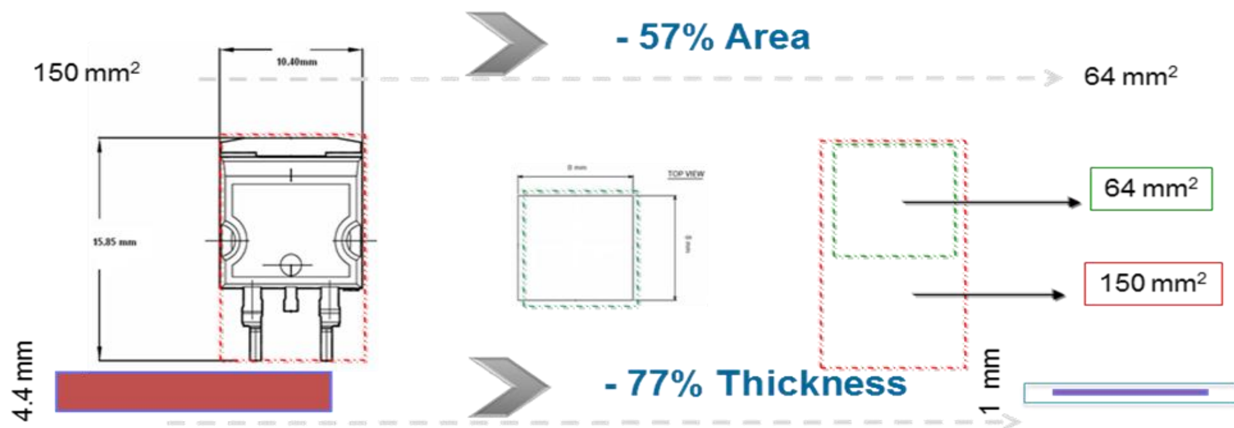

Fig. 6. In addition to being much thinner, the pc-board footprint for the HV PowerFLAT 8×8 is less than half that of the D^2PAK, yet it has a compatible contact footprint.

The PowerFLAT does have a characteristic that may cause difficulties for some users, at least initially. Unlike the D^2PAK and DPAK packages with their exposed leads, the contacts of the HV PowerFLAT 8×8 are partially underneath the package. Thus, once it is mounted and soldered, the traditional visual-inspection procedure is not feasible, and existing test fixtures (which assume easy access from above) may have to be redone. However, the industry has successfully used low-voltage MOSFETs in the similar PowerFLAT 5×6 package for several years.

The benefits of the HV PowerFLAT 8×8 package are more than physical. The package's internal die-to-lead bonding and associated pinout configuration have greatly reduced parasitic inductances. This reduction results in cleaner waveforms and signal-transition characteristics, critical when switching high currents at the higher slew rates associated with faster switching.

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Thermally, the HV PowerFLAT 8×8 is comparable to the D^2PAK, with $R_{\Theta j(amb)}$ of 45°C/W. It is also important to note that creepage and clearance distance is 2.7 mm between the drain and the source-gate area. This value will meet spacing requirements of the various safety agencies.

Process + Package = Major Step Ahead

The challenges for design engineers of achieving greater efficiency, improved thermal performance, and smaller product size can be addressed with the right combination of power MOSFET process and packaging. Innovations such as superjunction MOSFETs and HV PowerFLAT packages will help designers meet these goals in the many kilowatt-level applications where power conversion plays a critical role.

About The Author

Vipin Bothra is product marketing manager at STMicroelectronics based in Schaumburg, Ill. Over the years Vipin has held many roles at ST in application, marketing and technical marketing. He holds an MBA from the Kellogg School of Management and a Bachelors degree in Electrical Engineering from VNIT, India.

Vipin's technical experience includes designing various applications in power conversion such as digital power supplies, drivers for LED lamps, high-efficiency solar inverters and PFCs. The Triac-dimmable offline LED driver was developed by Vipin and his team and received a patent in 2008. Vipin has authored many publications in technical publications around the world and has actively participated in many regulatory and standard-setting bodies in the U.S.

For further reading on power MOSFETs, see the How2Power Design Guide, select the Advanced Search option, go to Search by Design Guide Category, and select "Power Transistors" in the Component category.

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