Understanding The Breakdown Characteristics Of Lateral GaN-Based HEMTs

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Recently, there has been much discussion surrounding the production release of GaN-based power devices. Within the deluge of commentary, there have been several propositions put forth that suggest there are outstanding issues the industry must address. One such issue involves the breakdown mechanism for GaN based n-channel high electron mobility transistors (HEMTs). For lateral GaN-based HEMTs formed on silicon substrates, it has been suggested that the breakdown of these devices through catastrophic, non-recoverable, dielectric failure is both unexpected and undesirable. However, this behavior is neither unexpected nor essentially undesirable.

Lacking a spatially resolved PN junction, lateral GaN-based HEMTs do not exhibit recoverable breakdown behavior and have no avalanche capability. Their primary breakdown mechanism is dielectric breakdown of the overlying insulating layers in the device. In that regard, they resemble ceramic capacitors more so than silicon power semiconductor devices. This major difference in breakdown behavior affects how the new GaN-based devices should be designed, rated, and specified in power electronics applications. In addition, there are secondary breakdown mechanisms such as leakage that will influence device design and ratings. All of these issues will be discussed in this article with an eye toward giving the power system designer a clearer understanding of how to compare the new lateral GaN-based HEMTs with existing silicon and silicon carbide-based devices.

The Missing P-N Junction

One of the greatest deviations of the GaN-based HEMT device structure from the incumbent silicon-based power device technologies is the absence of a spatially resolved p-n junction in the lateral GaN-based HEMT. The p-n junction has been a core element of nearly all widely adopted power devices over the last 40-plus years. This basic structure provides for remarkable capabilities, which have been thoroughly exploited in, for example, silicon- and silicon carbide-based devices.

Bipolar action provides conductivity modulation in diodes and transistors, making these devices capable of effectively handling high current density. This is a major reason why insulated gate bipolar transistors (IGBTs) are currently the preferred device structure when forward voltage drop and not fast switching transition is the main performance metric of interest, especially at voltages above 400 V. However, it is another characteristic of the p-n junction that is critical to the current discussion.

The p-n junction provides for recoverable breakdown behavior. Specifically, the generation of electron-hole pairs across the effective bandgap under the high electric fields established across the relatively short depletion region of the junction provides the necessary current density to effectively clamp the externally applied voltage. The p-n junction breakdown condition, which involves multiplicative ("avalanche") generation of conduction or near-conduction charge carriers, is reversible when the (excessive) applied voltage is removed. This characteristic of the p-n junction can be contrasted with the irreversible and catastrophic breakdown of an insulator, which occurs through a percolation mechanism of broken electronic bonds.

In addition, the p-n junction provides two- and sometimes three-dimensional field plating, reducing the maximum applied field in the bulk semiconductor and surface regions. This clamp is inherently incorporated in a MOSFET. It is the "avalanche" breakdown of such p-n junctions, often near the planar limit, which are used to determine the x-axis values of the common figure-of-merit plot of specific on-resistance (Rdson) vs. material device breakdown voltage limits.

Such a p-n structure is not natively present in an n-channel GaN HEMT. This is not only due to the majority carrier nature of the two-dimensional electron gas (2DEG) that provides conduction in what is essentially a voltage-controlled resistor. Nor is the missing p-n structure due to the fact that the wide bandgap and extended valence band edge contour make holes rare and extremely slow (heavy). Rather, a major reason why lateral GaN-based HEMTs do not generally incorporate a source-drain clamping p-n junction resides in the inherent nature of the III-N material itself.

GaN, as well as the 16% to 25% Al-containing AlGaN layers, typically used as barrier layers in HEMTs, are compositionally unstable above temperatures of about 900°C. The film decomposes as nitrogen leaves the surface and the gallium pools when the surface vapor pressure exceeds the available ambient partial pressures.

Even with the presence of a passivating film, such as silicon nitride, the stoichiometry of the surface and near-surface regions of the III-N films severely degrades above about 1000°C. Meanwhile, to form viable low-leakage p-n junctions, temperatures much greater than 1000°C are required. Such temperatures are necessary to obtain the slow, solid-state diffusion and high binding energies, which in turn are required for effective annealing of implantation damage and/or the diffusion and incorporation of dopant species.

To be sure, GaN-based light emitting diodes (LEDs) incorporate functional p-n junctions. However, in such cases, the junction is formed as a blanket, laterally homogeneous combination of doped layers during epitaxial layer growth. Such a uniform vertical junction will not serve the purpose of a source–drain clamp in high-voltage (>300 V) switching power devices using lateral HEMTs.

In any case, incorporation of a p-n junction across the source-drain of the GaN-based HEMT would add switching charge as well as the minority-carrier-recombination-induced tail in the reverse recovery characteristics. In general, both of those side effects would be undesirable in a power switch. In fact, it is the absence of these minority-carrier-induced reverse recovery characteristics that provide GaN-based HEMTs with an overwhelming advantage over silicon alternatives in applications where switching fidelity and low noise are critically important such as class-D audio amplifiers.

Think Dielectric Breakdown, Not Avalanche Capability

The consequence of the lack of effective reduced surface field (RESURF) effects from a laterally resolved p-n junction in GaN-based HEMTs is that the peak surface fields are determined by the nature of conductive field plates present above the III-N epitaxial layers, as well as the epitaxial substrate properties. The maximum fields present in the device are therefore not found in the semiconductor material, rather they exist in the overlying insulators. The highest fields in the semiconductor are present at the edge of the depleting 2DEG and are found in the AlGaN barrier, not the GaN channel layer.

Therefore, the applicable material properties that define the figure-of-merit tradeoff between standoff, reverse voltage capability and on-state resistance of a lateral GaN-based HEMT are those of the overlying (gate/field) dielectrics and to some extent the AlGaN barrier, not GaN, in contrast to what is commonly found in the literature on the subject. Therefore, the applicable critical fields are 700-1000 V/cm for typical insulators of Si_3N_4 and SiO_2, compared to about 300 V/cm typically assigned to GaN. That being said, the different breakdown mechanism in insulators requires considerations different than those of p-n junction-based device design in semiconductors.

Since the p-n junction breakdown is recoverable, devices using this mechanism can be designed to actually break down in operation. If, however, the current density during such a condition should cause the related semiconductor regions to become intrinsic, the associated power density will quickly lead to a thermal runaway condition and catastrophic device failure. The capability of the clamping p-n junction to process current is referred to as the avalanche capability of the device.

The avalanche rating has been used extensively by circuit designers in the selection of power device components, especially when large voltage spikes from noise or inductive-load-switching-induced back EMF conditions are expected. This has been useful, as such voltage spikes are effectively clamped by the p-n diode. As lateral GaN-based HEMTs do not generally incorporate p-n junctions, there is no avalanche capability that can be associated with these devices. This reality will require some new approaches in the design and use of these near-ideal power switches.

First, in order to provide robust reliability, the device design must account for the time-dependent dielectric degradation of the overlying insulators. This means that the time-weighted average maximum fields produced across the dielectrics should be designed to be less than about two times the dielectric breakdown field strength. This requires that a 600-V rated device have a surface instantaneous dielectric field limited breakdown voltage of at least 1200 V.

It is important to recognize that the magnitudes of the fields in the overlying dielectric films are essentially inherent to the near surface nature of the 2DEG conduction channel, including the gate-drain drift region. One consequence is that the dimensions of the device (e.g. gate to drain) will likely be greater than those calculated using a p-n junction breakdown-based model, and therefore the associated on-resistance will be higher than otherwise anticipated.

At first glance, this may be referred to as "over design," when it simply reflects the governing device physics. A redeeming consequence of such a robust design is that there is significant headroom between the rated device operating voltage and the actual breakdown of the device, unlike the 5% to 10% often present in modern silicon-based power devices. In this way, the concerns of handling noise or back-EMF-induced voltage spikes across the lateral GaN HEMT are resolved. In fact, this is very much the same consideration that has been applied to the specification and use of ceramic capacitor components. This is reasonable since the underlying physical constraints are so similar.

Another Breakdown Mechanism: Leakage Currents

Of course, it is important to discern the surface-limited breakdown from other breakdown mechanisms, for example, that which occurs across the epitaxial layer between the drain and substrate. Fig. 1 shows four-terminal leakage measurements for a 600-V rated device using International Rectifier's GaNpowIR platform for a) the case of grounded silicon substrate and b) the case of floating silicon substrate. As can be seen, grounding the silicon substrate produces a measured epitaxial-layer-limited breakdown voltage of some 950 V, while "floating" the substrate demonstrates a surface-limited breakdown of more than 1400 V.

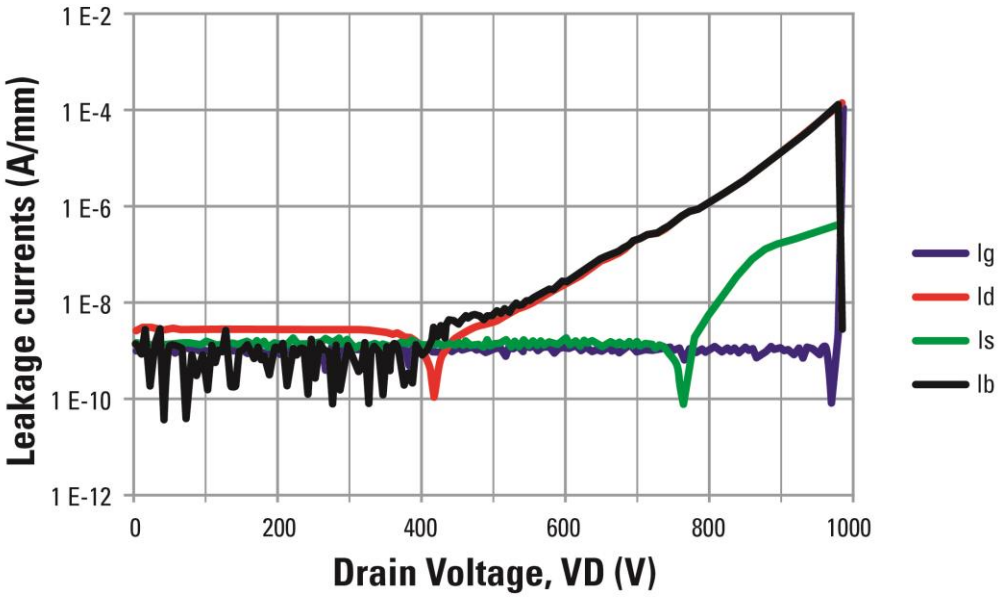

Fig. 1a. Four-terminal room temperature leakage currents for 600-V rated GaN-based HEMT using IR's GaNpowIR technology platform as a function of drain bias with substrate grounded.

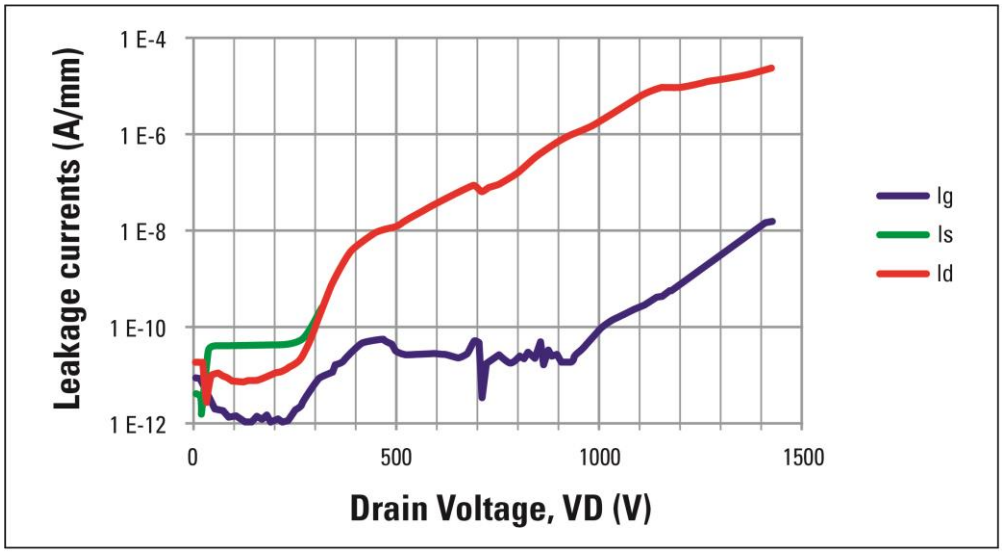

Fig. 1b. Three-terminal room temperature leakage currents for 600-V rated GaN-based HEMT (same design as Fig. 1a) using IR's GaNpowIR technology platform as a function of drain bias with substrate floating.

Both results confirm the capability of the device to support an operating withstand rating of 600 V. Furthermore, the long-term stability shown in Fig. 2 demonstrates the capability for reliable operation at the standard condition of 80% of the rated voltage at 150°C for over 5000 hours. It is imperative that such long-term studies include longer periods than the silicon-based standard 1000 hours, as the applicable activation energy for time-dependent dielectric breakdown in these GaN-based HEMTs is much less than the 0.8 eV commonly associated with silicon-based device failure mechanisms.

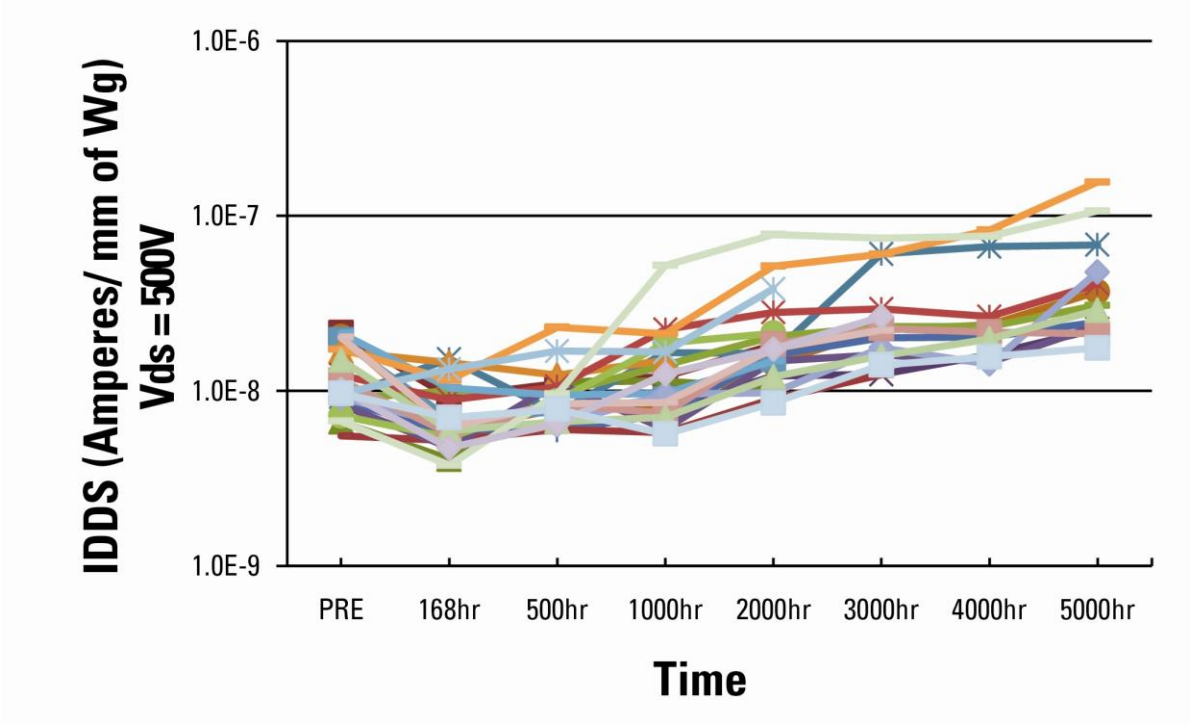

Fig. 2. Source-to-drain leakage current, Idss, measured with 500-V drain bias on 600-V rated cascode switch for a population of representative devices with Wg = 120 mm, under a drain bias of 480 V for up to 5000 hours at 150°C.

Therefore, it can be seen that the non-recoverable breakdown of lateral GaN HEMTs is a natural consequence of the absence of a clamping p-n junction. Avoiding the deleterious switching behavior due to the minority carrier effects associated with the p-n junction, the GaN-based HEMT achieves superior performance to silicon-based power devices while requiring the same disciplines currently employed in using a common component in the same power conversion circuits, namely ceramic capacitors.

The same design margin that is required to provide long-term reliability from the time-dependent dielectric breakdown of the overlying insulating layers, necessitated by the high electric fields present due to the surface nature of the lateral HEMT construction, also provides adequate headroom for voltage spikes caused by noise and back EMF found in typical application conditions. The different breakdown-voltage-determining mechanism for GaN HEMTs should be taken into consideration when comparing these power devices with those based on bulk semiconductor behavior using p-n junctions such as silicon or silicon carbide.

Reference

For more information on International Rectifier's GaNpowIR technology, see http://www.irf.com/product-info/ganpowir/.

About The Author

Michael A. Briere, former executive vice president of research and development and chief technology officer, joined International Rectifier in November 2003. Prior to his promotion in September 2007, he served as the executive vice president, research and development, and prior to that, vice president of integrated circuit development. Among his duties, Briere was responsible for IR's GaN development between 2005 and 2007. Before joining IR, Briere held technical and leadership roles at IBM, Cherry Semiconductor, ON Semiconductor, and Vicor, where he led a start-up IC subsidiary, Picor. In addition to his time in the semiconductor industry, Briere has performed research at leading research institutes including Hahn-Meitner-Institute (HMI) in Germany and Lawrence Livermore National Laboratory (LLNL) in the United States.

Currently, Briere has formed his own executive scientific consulting company, ACOO Enterprises. Briere earned his Dr. rer. nat. (Doctorate of Natural Studies) in Solid State Physics from the Technical University of Berlin and his MS in Physics and BSEE from Worcester Polytechnic Institute in Massachusetts. He served as associate adjunct professor in physics at the University of Rhode Island. Briere is an active member of the IEEE and served on the program committee of the International Symposium for Power Semiconductor Devices and ICs (ISPSD).

For further reading on GaN power devices, see the How2Power Design Guide, select the Advanced Search option, go to Search by Design Guide Category and select "Silicon Carbide and Gallium Nitride" in the Popular Topics category.