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Demystifying PSRR Specifications For LDOs

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The quest for lower-noise feedthrough over frequency in low-dropout regulator (LDO) circuits is driving designers of mobile devices, tablets, and portable instruments to seek LDOs specifying ever-higher levels of power supply ripple rejection ratio (PSRR). While an LDO PSRR figure at higher frequencies often relates to improved system performance due to increased bandwidth in noise rejection, its popularity has overshadowed the device's native performance. A PSRR specification of ~ 10 MHz is often confusing, distorted, and unqualified.

This article aims to clarify the LDO PSRR specification across the user application's frequency range of interest and dislodge common myths to help designers make intelligent LDO selections. In addition, proven solutions in the form of circuit recommendations and LDO device options are provided to help engineers achieve their design goals.

The PSRR Specification And LDO Performance

To understand the need for an LDO with high PSRR over a broad frequency range, let's examine some system design concerns. For example, consider an efficient switcher powering a system. If used to power low-bandwidth circuits such as string gauge or temperature sensors with a bandwidth of a few hertz, there is no issue. In contrast, if the switcher powers sensitive circuits like a low-noise amplifier (LNA), data converter or phase-locked loop (PLL), an LDO will be required to post regulate the switcher.

Because switching noise can be a prime contributor of aliasing, interference and jitter, significant attenuation is necessary to prevent system failure. Through mechanisms such as system amplification, sympathetic mixing, and up conversion, noise can manifest itself in modulation and distortions that interfere with data transceiver and radio transmission. Moreover, noise can "gain up" as undesirable electromagnetic interference (EMI). LDOs are routinely used to mitigate these ill effects.

Unfortunately, circuit designers sometimes select the wrong LDOs, possibly as a result of misleading product marketing in which designers are lead to believe that the LDO with the highest PSRR specification is the device of choice for solving all their noise problems. This idea is neither accurate nor valid as will be explained.

A wider-bandwidth LDO improves PSRR because it enables the feedback loop to track a broader frequency range of ripple noise and allows faster transient response. Yet, commercially available LDO ICs are generally designed with a loop bandwidth between ~ 10 Hz to ~ 200 kHz and a crossover frequency (f_c) from ~ 1 kHz to 2 MHz, with a recommended output capacitor (C_{OUT}) value and equivalent series resistance (ESR). Hence, most LDOs alone cannot support usable rejection merits beyond a megahertz.

As illustrated in Fig. 1, an LDO consists of a voltage reference, an error amplifier, a MOSFET, feedback resistors, and compensation networks. A low-bandwidth active low-pass filter serves as a low-noise supply source to power sensitive circuits. Fig. 2 depicts a plot of PSRR response over frequency for a typical LDO.

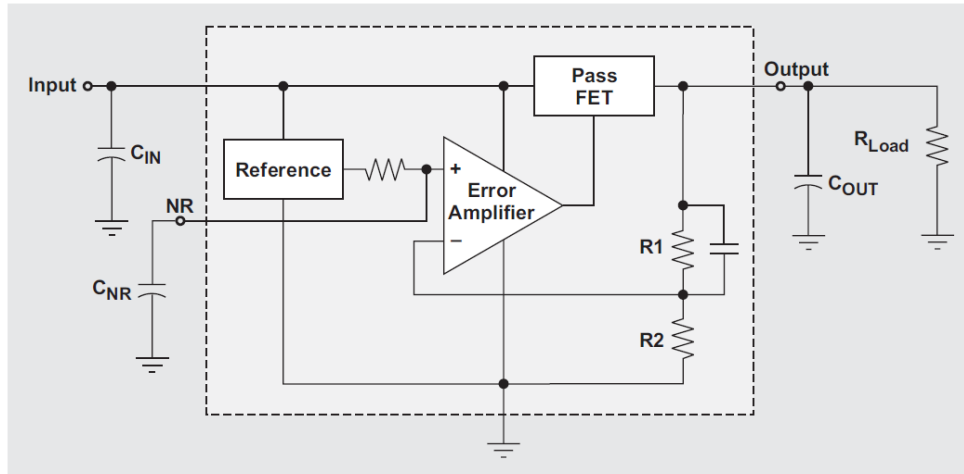


Fig. 1. Simplified block diagram of a typical LDO.

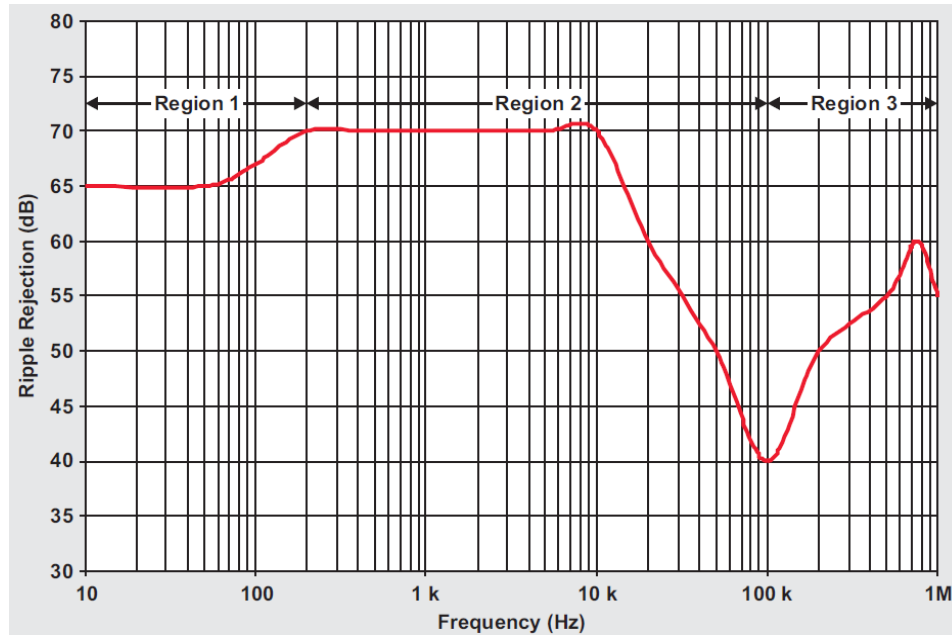


Fig. 2. Typical LDO PSRR over a wide frequency range.

In Fig. 2, the low-frequency spectrum from dc to ~100 Hz of the PSRR graph (Region 1) depicts the bandgap filter's roll-off frequency. It is dominated by both its open-loop ac gain and the bandgap PSRR. The dominant internal source of PSRR in an LDO is the bandgap reference. Bandgap noise propagates noise to the gain, control, and output stages. To manage reference noise, employ large RC filters and use a pre-regulated source to power the reference.

The midband (~200 Hz to 10 kHz, Region 2) is from the bandgap filter roll-off frequency to the control loop's unity-gain frequency where PSRR is dominated by the LDO's open-loop gain. Note that the loop gain is also modified by changing load, which alters the pass FET impedance. For example, as increased loading loop gain decreases PSRR declines. Reduced headroom also decreases PSRR as this condition and heavy loading both bring the pass FET out of saturation into the triode region. This results in no-loop gain. The converse is also true where light-loading and copious headroom can boost PSRR.

Beyond the crossover frequency from about 100 kHz to 2 MHz (Region 3), the bandwidth-limited loop starts showing little to no effect on PSRR. C_{OUT} dominates along with the LDO output impedance. Any substantial parasitics from V_{IN} to V_{OUT} can have a profound influence on PSRR.

These are some of the fundamental particulars not covered by LDO datasheets. The PSRR figure of merit is actually attributable to the supporting components, rather than to the LDO itself. New classes of LDOs like those with low noise, low power, high PSRR and wide bandwidth make data sheet specifications further convoluted with conflicting requirements and few references about tradeoffs and selection. Ultra-low noise and very low-power LDOs may issue performance compromises such as startup time, transient response, and solution size/cost.

Achieving PSRR Levels At Higher Frequencies

How can useful PSRR levels be achieved at higher frequencies? Fig. 3 illustrates the relationship between bandwidth and PSRR. Basically, gain falls and PSRR declines over frequency. The PSRR action beyond 1 to 5 MHz is primarily attributable to the feedback *divider* associated with the pass FET and to the output impedances on the printed circuit board (PCB) design—not the LDO.

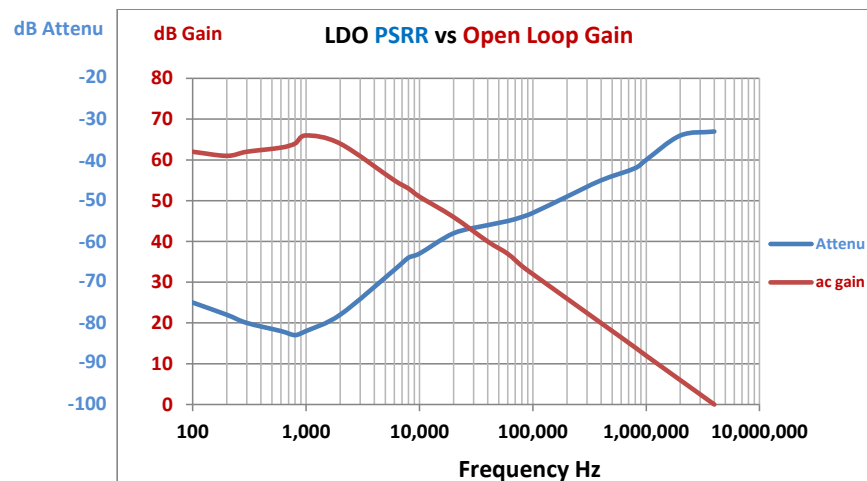


Fig. 3. Sample plots of LDO PSRR and open-loop gain over frequency.

Traditionally, LDO datasheets graph PSRR up to 1 MHz. Consider the impedances of the pass FET, R_{LOAD} , C_{OUT} , and any significant parasitics on the PCB that form a divider network (Fig. 1). The network also functions as an ac-scaler, attenuating the amount of noise ripple traversing from the input to the output.

In practice these components contain more elements. For example, there are metal interconnect inductances in the LDO and on the PCB. The pass FET consists of terminal capacitances plus inductance and resistance. C_{OUT} has inductance and ESR that can modify the ac loop gain. These elements play an important role in determining the high-frequency PSRR profile. Fig. 4 is a typical model of the voltage divider formed by the various impedance components at the LDO's output.

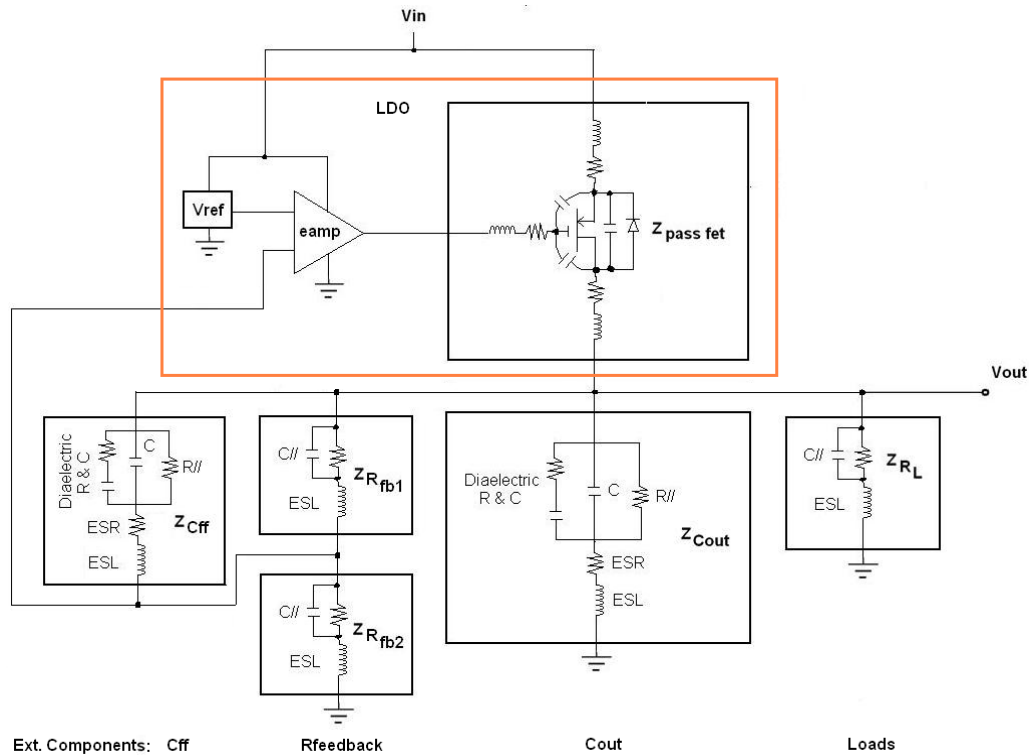


Fig. 4. Output divider formed by the impedance elements in an LDO application.

The effective ripple noise voltage impedance divider ratio (impedance blocks in Fig. 4) can be expressed as an attenuation factor (AF) as shown in Equation 1:

$$AF = \frac{(Z_{COUT}) // (Z_{RL}) // \{[(Z_{RFB1} // Z_{FF})] + (Z_{RFB2})\}}{Z_{COUT} \cdot Z_{RL} \cdot [(Z_{RFB1} // C_{FF}) + (Z_{RFB2})]} + Z_{PASS_FET}$$

(Eq. 1)

Since Z_{RL} parallels with Z_{COUT} , it has a much lower impedance than the Z_{PASS_FET} and feedback resistors at high frequencies. The attenuation factor provides substantial attenuation of the supply ripple noise from V_{IN} to V_{OUT} . For LDOs with less significant parasitic effects from integrated internal feedback resistors (R_{FB}) and compensation, Equation 1 can be further simplified as:

$$AF = \frac{(Z_{COUT}) // (Z_{RL})}{(Z_{COUT} // Z_{RL}) + Z_{PASS_FET}} \quad (\text{Eq. 2})$$

At high frequencies C_{OUT} experiences lower impedance than R_L , offering effective ripple suppression. Z_{COUT} can be viewed analogously as efficient low impedance, shunting high-frequency noise to ground. Because C_{OUT} has such a dominant effect on PSSR, its size and make can influence its impedance and companion parasitics.

Beyond its resonance frequency, C_{OUT} becomes less capacitive and more inductive. Consequently, PSRR degrades at higher frequencies. C_{OUT} must perform as a capacitor over the required frequency range.

As mentioned, on-board parasitic capacitance, resistance, and inductance also affect PSRR. Some LDO designs require small C_{OUT} on the order of a picofarad, which may approach the PCB parasitic capacitance. When C_{OUT} ESR becomes significant in small capacitors, PSRR may be compromised. Increasing C_{OUT} may improve PSRR, but can change the loop gain, transient response, and stability margin. Its value cannot be arbitrarily chosen favoring one parameter while ignoring the consequences of others. Good design practice when selecting C_{OUT} capacitance, its material, and construction is needed to balance the priority of the overall design objectives.

PSRR plots beyond 1 MHz on many LDO datasheets can be perplexing. Are these so-called advanced wide-bandwidth LDOs truly capable of suppressing supply noise out to 10 MHz and beyond, given their relatively low-loop bandwidth? Are vendors measuring PSRR properly and accurately? The truth is that practically all LDOs on the market are incapable of rejecting supply noise effectively beyond a few megahertz. Above the device's loop bandwidth frequency, vendors are not really measuring the LDO's ability with respect to PSRR, but that of the C_{OUT} and companion impedances of the pass FET, plus circuit board parasitics.

Consider the LM317 voltage regulator, an old industrial workhorse. Though not an LDO, its PSRR plots are interesting. It has a crossover frequency of $f_c = 1$ MHz. Its PSRR characteristic rolls off rapidly beyond 10 kHz, with the recommended output capacitor value of 1 μ F. The LM317 datasheet PSRR plots (solid lines in Fig. 5) show the ripple rejection versus frequency up to 1 MHz. No misleading claim or inflated figures on PSRR beyond 1 MHz are shown because, beyond that, it's no longer a measure of the native device characteristics.

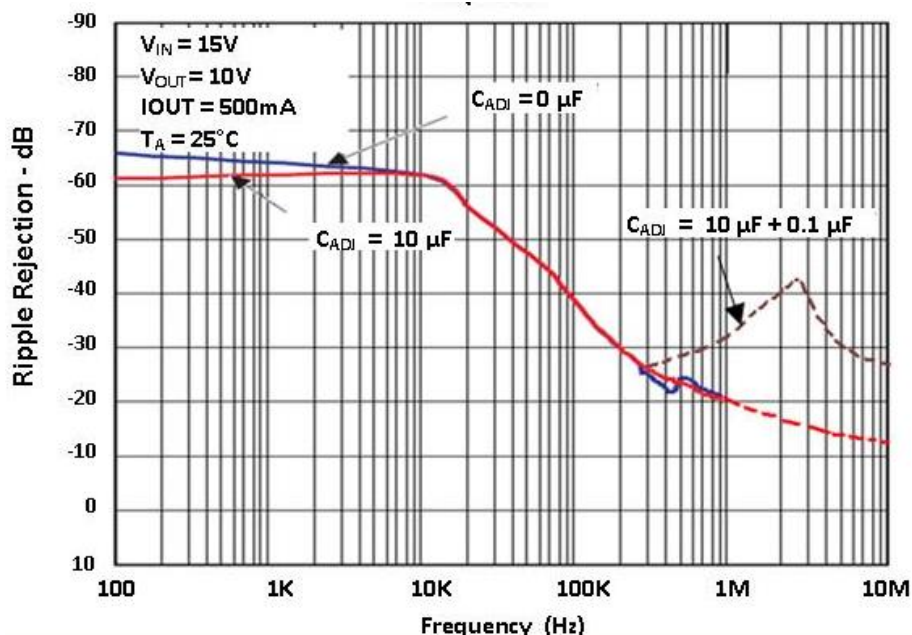


Fig. 5. LM317 datasheet PSRR plots with extended frequency graphing.

However, if you want to achieve moderate attenuation out to 10 MHz, you can parallel C_{ADJ} with a 0.1- μ F capacitor. The smaller shunt capacitor has lower impedance at high frequency, thus, it makes a better impedance divider. The result (dotted line in Fig. 5), demonstrates that an added capacitor can improve PSRR characteristics equal with advanced LDOs designed decades later!

PSRR Testing And Setup Challenges

Unlike trivial voltage and current measurements, a PSRR test is delicate and time-consuming. This is because they are easily affected by parasitics from test apparatus and components, and setup conditions. Moreover, PSRR is sensitive to noise, whether coupled or induced. Mechanical or electrical perturbation from ambient or measurement setup can corrupt PSRR data.

Several methods are employed in the industry to ascertain the noise voltage output divided by noise input over frequency. Some use a function generator, a power amp or equivalent supply source, and oscilloscope. Lately many PC-based Bode, network, and frequency response boxes are used because they are inexpensive, self-calibrating and portable, versus bulkier network and spectrum analyzers. An accurate PSRR test setup for modern LDOs may involve a network analyzer and power/signal source (Fig. 6.)

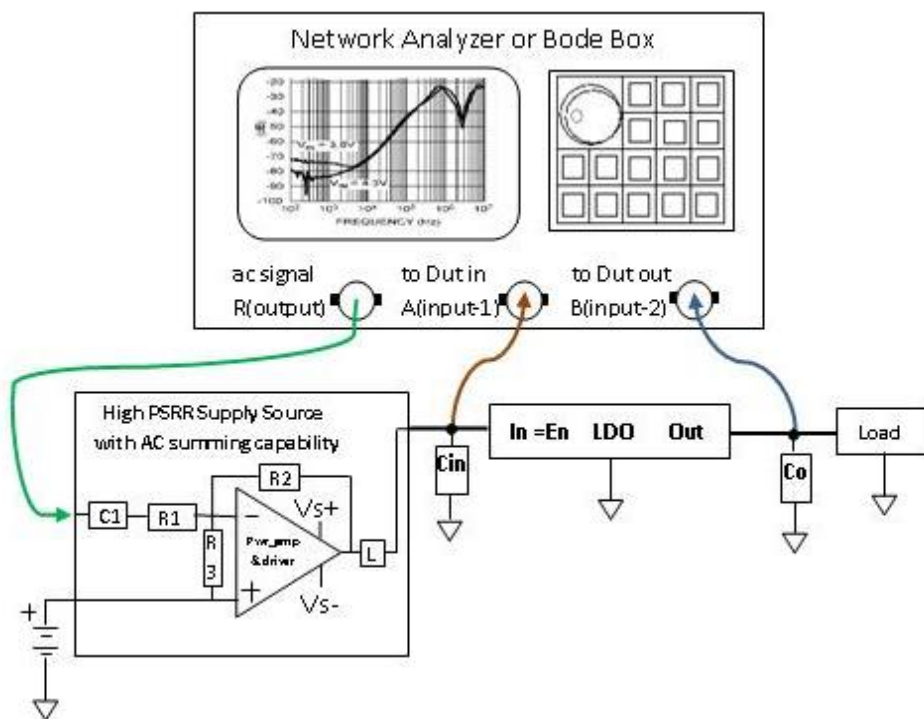


Fig. 6. Sample PSRR test setup using network analyzer and low-noise supply.

Besides adhering to good RF and noise-abatement practices, the clean dc supply and ac test signal injector combination is the most critical component in the setup. To achieve an optimal PSRR test setup, build it with your best low-noise audio amplifier that responds down to sub-hertz frequencies. Use an immaculate amplifier with excellent midband to low RF frequency response, and/or a custom-wound transformer and capacitor pair as the line signal injector.

You can buy an off-the-shelf transformer-LC signal injector contraption, or order custom signal transformers for the job. (Note that transformers tend to be easily magnetized and can be permanently damaged due to overcurrent, so buy some spares.) There are commercial line injectors like the Picotest J2120A, a high headroom supply that sums an ac test signal.

The active injector, whether built in-house or purchased from a commercial source, is a good test tool for general use because the component makes it a pseudo-standard test jig for suppliers and manufacturers as reference PSRR validation platform. On the analyzer setup, use slow sweep times because fast sweeping can cause subtle discontinuities and erroneous data.

LDO Selection

Assuming that you have arrived at the desired dropout and input/output voltages; output, inrush, and bias currents, etc., the focus next is on PSRR and noise as the key criteria for LDO selection. Two classes of LDOs are available today for portable applications: low- and wide-bandwidth devices. There are several tiers of noise and PSRR LDOs among them. From the earliest LDOs to nearly all those made in the last three decades, the LDOs' 3-dB bandwidth has ranged from about 100 Hz to 10 kHz. These lower-bandwidth devices offered good noise performance and transient response tradeoffs.

Today, as highly integrated and compact systems are designed and faster transient response is demanded, a newer class of LDO has emerged: the wide-bandwidth or high-PSRR LDOs. The fundamental difference between these older and newer classes of LDOs is the slightly broader loop bandwidth of the newer LDOs.

In some cases, vendors may use f_c as the gauge, instead of F_{3dB} for bandwidth comparison. Datasheets for the new, wide-bandwidth devices may indicate f_c values that are 10 times higher than the 1 MHz specified on conventional LDO datasheets. Despite the broader bandwidth, the loop gain of these devices becomes low approaching f_c , such that the augmented rejection span and magnitude are less significant. Still, some LDOs are redesigned with higher bandwidth, such as a nested loop to aid transient response. Other enhancements may include internal high-frequency bypassing and cascade structure to further increase the rejection ratio. The net result issues a flatter gain over the low-to-midband frequency range, improving PSRR.

These newer devices target the appreciable improvement in noise and/or PSRR for use with switchers operating between 2 and 6 MHz. Of course, the highest-frequency PSRR performance remains the principal job of C_{OUT} and adjoining impedance. This class of LDO can be recognized from its PSRR plot, which exhibits a relatively flat rejection characteristic in the midband.

In contrast, conventional LDOs generally show their best PSRR hugging a narrower plateau at low frequencies. As with any device family, one LDO cannot be a jack of all trades. For example, in RF applications, an LDO needs both low noise and high PSRR. The oscillator demands high PSRR in the hundreds of hertz bandwidth, while audio requires high PSRR up to 20+ kHz. For digital blocks, the PSRR is not relevant.

Subtleties and tradeoffs between noise and PSRR among LDOs are illustrated in Fig. 7, which highlights a high PSRR, low-noise LDO exhibiting broadband high PSRR with distinct low-noise characteristics.

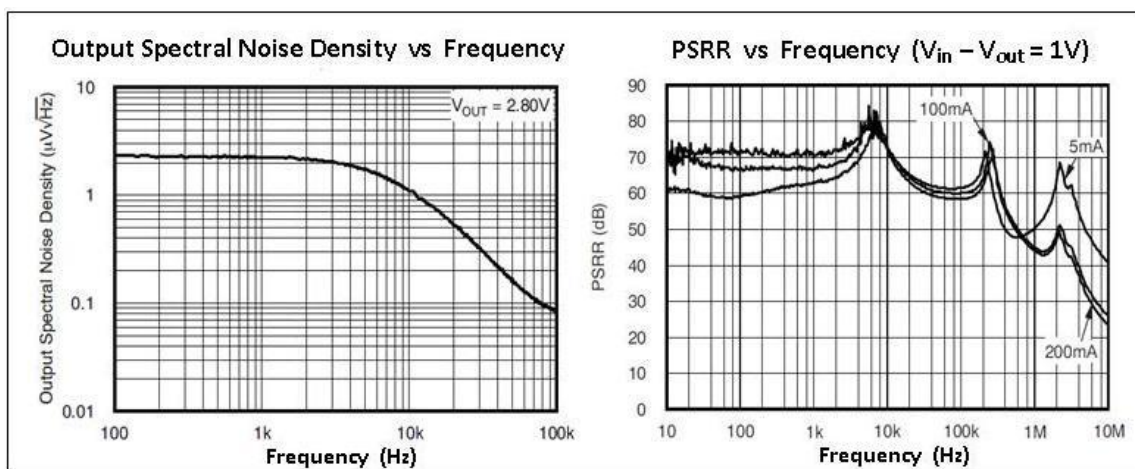


Fig. 7. Output noise and PSRR plots for a high-PSRR, low-noise LDO, the TPS718XX.

Fig. 8 shows a high-bandwidth LDO with very high and very flat PSRR out to the midband. However, the noise spectrum at the low-frequency corner is comparatively higher than most other types of devices. This illustrates a notable tradeoff.

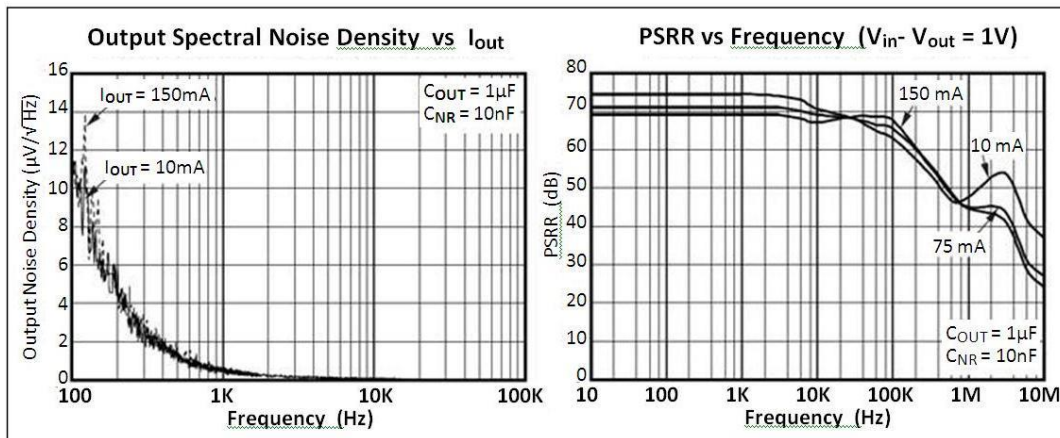


Fig. 8. Output noise and PSRR profiles for a high-bandwidth PSRR LDO, the TPS717XX.

Fig. 9 is a low-noise high-PSRR, high-voltage RF LDO that employs a bipolar pass-PNP and requires several milliamps of quiescent current. Nevertheless, its tradeoff is with excellent low-noise spectral attributes. It displays high-and-flat PSRR characteristics in low frequencies and maintains relatively high PSRR through midband to high frequencies.

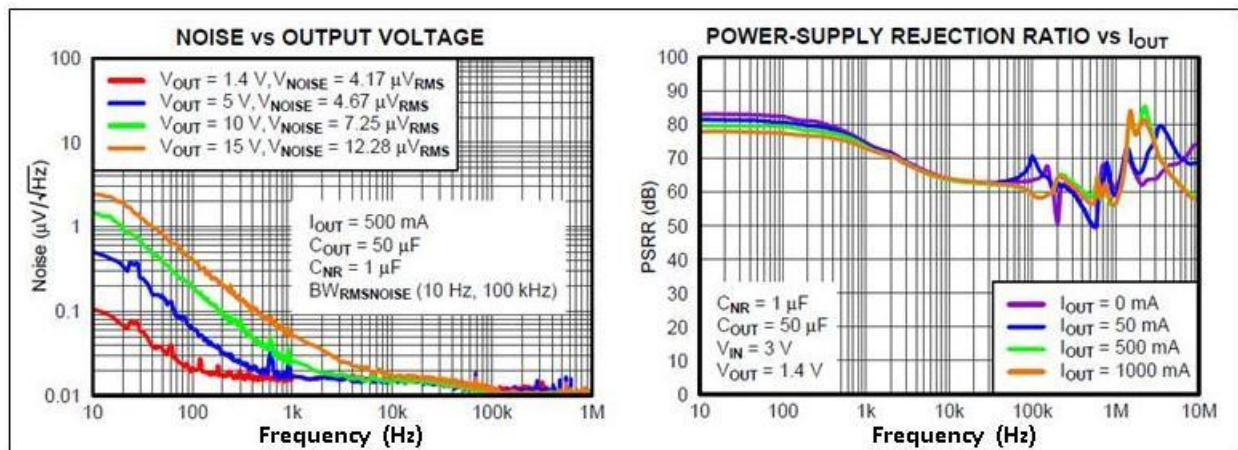


Fig. 9. A low-noise, high-PSRR RF LDO (the TPS7A47).

Fig. 10 depicts a typical ultra-low noise, high-PSRR LDO. This type features low-noise spectral density characteristics, which are significantly better than those of the typical high-bandwidth and high-PSRR LDOs. Meanwhile, its PSRR is quite good, and remains relatively high out to the midband frequencies.

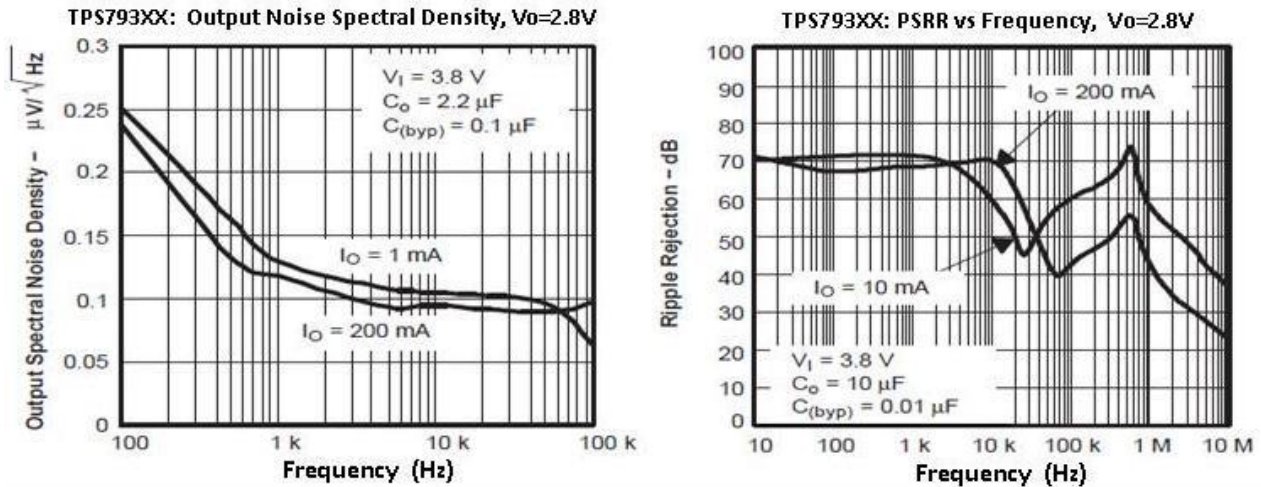


Fig. 10. An ultra-low noise, high-PSRR, and fast LDO (the TPS793XX).

Lastly, Fig. 11 pitches in another ultra-low noise, high-PSRR LDO. This device displays even more outstanding noise spectral characteristics, and its PSRR is comparable to the previous LDO, albeit a bit less stellar. In a nutshell, the foregoing examples outline some of the noise, PSRR specifications, and power tradeoffs involved in choosing among different categories of LDOs. Moreover, be aware that devices within the same class or type may show their noise and PSRR characteristics very differently.

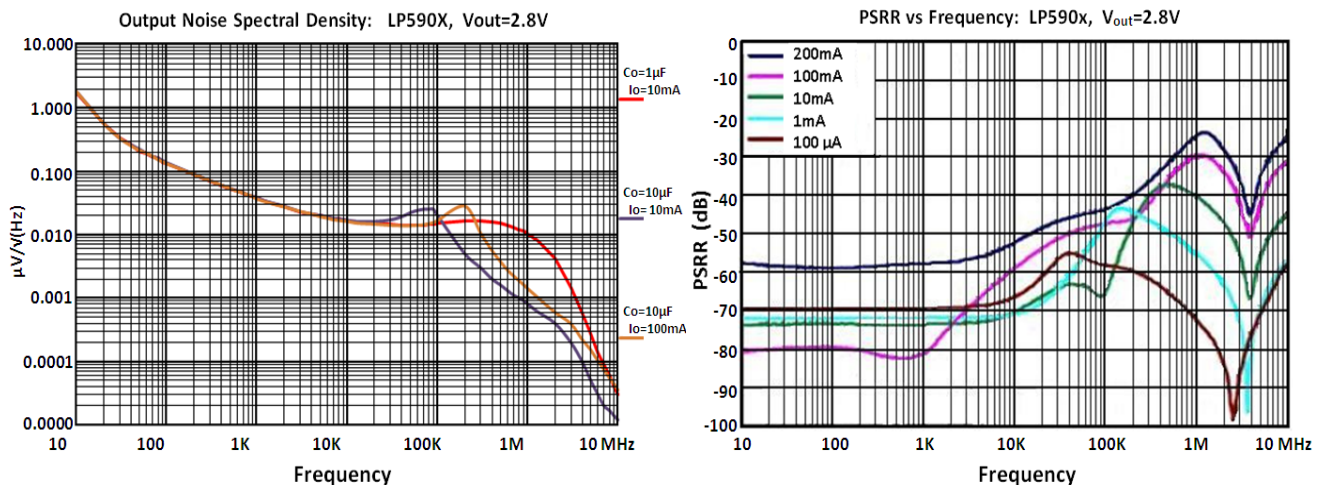


Fig. 11. An ultra-low noise, high-PSRR LDO (the LP5904/LP590X).

Which LDO is a good choice for your system needs? Are those advertised as high PSRR suitable for your design, or would the ones having a relatively high PSRR over broader frequencies be the better options? Or perhaps the ones that exhibit higher PSRR under lower headroom and higher loading conditions? Or is the very low-noise LDO right for your application, versus those with the highest PSRR at lower frequencies?

These questions require a clear understanding of system design priorities in order to make judicious selections. Unfortunately, PSRR and noise are often confused as a similar figure of merit. For example, low noise is generally perceived as being synonymous with high PSRR. The subtlety between noise rejection ratio and output noise voltage (spectral noise density) is that PSRR is defined as the ratio of output noise to injected input noise.

Two different LDOs with similar PSRR profiles but dissimilar circuit designs can have different noise characteristics. A higher noise ratio mechanism does not necessarily translate to a lower-noise device. Review the most critical design requirements, then consider whether the very high PSRR LDO or the ultra-low noise one makes the most sense. Perhaps, all that is needed for your requirement is an improved bypassing technique and/or capacitor selection on a conventional LDO! If the design priority is weighted more on noise performance than PSRR capability, scrutinize the LDO's specification on its noise dynamics against its PSRR attributes and vice versa.

There are some convenient remedies to adverse tradeoffs. For example, if a system cannot tolerate slower startup due to noise suppression schemes, choose an adjustable LDO. The external feedback/feedforward networks can be user optimized, reducing the noise amplification. This can improve noise while retaining decent startup time.

Finally, what if you must have superior noise and PSRR specifications and opt for no compromise? While this can be achieved, it depends on how much you are willing to sacrifice in other areas, or spend on the extra resources required to accomplish these goals.

Ultra-High PSRR Solutions

For demanding applications such as instrumentation, medical, or mil-aero applications, a wide-bandwidth LDO with the prescribed C_{OUT} or the lowest-noise device is inadequate. So additional decoupling capacitors and LC filters may be required, versus the active LDO circuitry and suggested C_{OUT} to roll off excessive device-plus-system noise. If you have decided on the PCB layout and selection of C_{OUT} , C_{IN} , and possibly C_{BYPASS} for $V_{REFERENCE}$, you are almost there.

In very critical and sensitive applications you can cascade two LDOs in tandem. With chip-scale-packaged components, this can be a cost-effective solution with a real advantage. Another robust solution is incorporating an external LRC filter, at either the LDO V_{IN} or V_{OUT} port. This technique can improve noise to less than 10 nV/ $\sqrt{\text{Hz}}$ and PSRR figures to higher frequencies with fewer compromises in performance.

Summary

System designers should not be swayed merely by graphics presented in LDO datasheets exhibiting PSRR improvement beyond f_c . LDO PSRR generally performs best at the low-to-mid band frequencies out to a few hundred kilohertz. Beyond its loop bandwidth the gain becomes so low that it has no ability to track noise signals effectively.

We presented a detailed discussion with examples to demystify the perceived and often erroneous PSRR specification. Noise rejection at higher frequencies is rendered dominantly by the impedance of C_{OUT} in conjunction with the pass FET and other on-board parasitic impedances.

Don't be misled by an LDO with exceptional PSRR at high frequency. To realize robust PSRR to meet your demanding system needs ensure the LDO has adequate drive, operates within a suitable V_{IN} range, limit loading from its maximum rating, and optimize the PCB layout plus bypass capacitors. LDO noise attributes are not identical to PSRR, and there are tradeoffs between them. LDO selection requires an attentive review of design goals and priorities.

References

1. Sanjay Pithadia and Scot Lester, "[LDO PSRR Measurement Simplified](#)," Application Report (SLAA414), TI, July 2009.
2. John C. Teel, "[Understanding power supply ripple rejection in linear regulators](#)," Analog Applications Journal (SLYT202), TI, 2Q 2005.
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4. For more information on TI's LDOs, visit www.ti.com/lido-ca.

About The Author



Kern Wong is a principal applications and design engineer for advanced power management unit (PMU) ICs and regulators in Texas Instrument's Silicon Valley Analog Mobile Devices Power Group (formerly National Semiconductor). Wong has over three decades of experience working with analog circuits, bipolar logic ICs, CMOS mixed signal ICs and microprocessor-based systems. He holds over a dozen patents in a variety of electronic technologies, including bandgap reference, PLL_clock gen and PMU ICs. Wong received his BSEE and MSEE from UC Berkeley and Washington University, respectively.

For further reading on LDOs, see the [How2Power Design Guide](#), select the Advanced Search option, go to Search by Design Guide Category and select "Voltage regulators" in the Power Supply Function category. For more on PSRR, go to Search by Design Guide Category and select "Noise Performance" in the Design Area category.