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At BiTS, Engineers Can Address Burn-In And Test Challenges One-on-One

by Kevin Parmenter, Contributor, Phoenix, Ariz.

Earlier this year, it was my distinct pleasure to attend this year's Burn –In & Test Strategies (BiTS) Workshop. The workshop, which is held annually in Mesa, Arizona, covers burn–in and test strategies mainly from the perspective of semiconductor manufacturing, yet much of what is discussed here is broadly applicable to many areas of electronics manufacturing.

Of course with everything needing power to be considered and the fact that reliable power sources are required for effective burn in to take place, power electronics was an interwoven theme at BiTS. Many of the discussions dealt with the challenges of providing power to the latest generation of semiconductor products. As semiconductor device lithography becomes more advanced, the required supply voltages continue to drop, while the precision and signal integrity issues become even more critical.

At BiTS, many of the presentation topics concerned interconnection and test sockets. Other presentations focused on sharing of best practices for test techniques. (A list of the BiTS 2014 presentations appears at the end of this article.)

Looking ahead to the next workshop in 2015, it is expected that a portion of the conference will be devoted to high-power testing and burn in. This is especially exciting when we consider that alternative energy inverters and electric drives in both industrial and vehicular applications are increasing in popularity and becoming more commonplace. This means that burn in and testing will need to consider higher voltages and currents in the overall test plan and how to deal with this situation in a safe manner in production testing environments.

Beyond its technical content, BiTS is very refreshing in terms of its atmosphere. The tone of the conference is very collegial and the scale of the event seems just right. It's large enough to be relevant and highly useful, yet not so large that you feel lost or overwhelmed. Excellent opportunities are available to network with others and discuss projects one-on-one with the attendees and exhibitors. It's also possible to see every paper presented as the conference format is set up to enable this.

When planning your list of events to attend, the BITS Workshop should be top of mind for consideration. Next year's event will be held March 15-18, 2015, once again in Mesa, Arizona.

The following presentations were given at BiTS 2014. For more information, see the BiTS Workshop 2014 Event Archive. By signing in as a guest, you can access these presentations per the instructions on the archive page.

TechTalk

"The Most Common Mistakes in Test"
Speaker: Jeffrey L. Roehr, Test and Data Analyst, Texas Instruments

During the process of test program development, characterization, and limit setting, there are some common mistakes that can be made by Product and Test engineers. Issues like 'data that is too good to be true', not understanding the limitations of using a Standard Deviation, passing devices with "0" values, and limits that allow for the 'physically impossible' such as negative supply currents. Examples of real products and real issues (including those with test tooling), with how limits were set, or how data was interpreted, are used to highlight some of the most common (and 100% avoidable) mistakes.

Distinguished Speaker – Brandon Prior

"Packaging And Interconnect Trends: QFN, WLCSP, Fine Pitch And Modular/3D Solutions"
Brandon Prior, Senior Consultant, Prismark Partners

Mr. Prior shared an overview of the global packaging market, with a focus on emerging and fast growth package solutions. In his presentation he reviewed where package miniaturization and modularization has taken us so far, and where it will lead in the next 5 years. Teardowns of high density boards and packages were used to illustrate key points.

Keynote – Simon McElrea

"Interconnectology – The Road to 3D"
Simon McElrea, President, Invensas Corporation

Interconnectology is everything involved with getting "Silicon into Systems": a holistic approach describing both technical interconnection and supply chain partnership interconnection. Nowhere does this concept apply more than in the commercialization of 2.5D and 3D integration technologies. From design, to processes, and equipment and material development, to manufacturing and test, 2.5D interposer products and 3D ICs require collaboration across the value chain to achieve high yielding devices, optimum cost-of-ownership and rapid time-to-market: all critical elements for today's consumer-driven market. Further, the middle-end-of-line (MEOL) processes require engineering knowledge that spans front- and back-end processing through to packaging, assembly and test. Consumer trends that are bringing about the need for Interconnectology to be adopted as a concept industry wide were discussed.

Session 1 – A Clean Start

"Contamination Mechanisms of Contact Probes"
Jon Diller, Kevin DeFord, Smith Connectors | IDI

"Special Coating Cleans-Up a Mess"
Paul Ruo, Aries Electronics, Inc; Erik Orwoll, Contact Coatings, LLC

"Unique Methodologies for Investigating On-line Cleaning Process Parameters and Recipe Optimization"
Jerry Broz, Soheil Khavandi, Bret Humphrey, International Test Solutions, Inc.

"Yield and Test Time Improvement via Automated Online Cleaning"
Brent Edington, TriQuint

Poster Session 1

"One-Piece Stamped and Formed Probe Pin"
Ichiro Fujishiro, Yamaichi Electronics

"Correlation and Measuring Techniques for ±5% Impedance"
Tom Bresnan. R&D Altanova

"Compliance Grounding – The Mechanical Importance of Grounding"
Shamal Mundiyath, JF Microtechnology Sdn Bhd

Session 2 – Doing the Heavy Lifting

"Kelvin Contactors for Wafer-Level Test"
Jim Brandes, Multitest – LTXC

"Temperature Characterization of High Power Switching Regulators"
Paolo F. Rodriguez, Analog Devices

"LIGA Precision Microfabrication for Electromechanical Applications"
Frank Schonig, Innovative Micro Design

Session 3 – Show Them What We're Made Of

"The Stuff We're Made Of: An Examination of the State of the Art in Socket Materials"
Jon Diller, Smiths Connectors | IDI

"Rising to the Challenge: Material Evolution to Enable Reliable Performance at Tighter Pitches and Higher Temperature"
Mike Gedeon, Materion

"180 Deg. C BGA Burn-in, Is It Doable?"
Kenji Ichihara, Masaru Sato, Noriyuki Matsuoka, Yamaichi Electronics Co., Ltd.

"Palladium Alloy Hardening and Wear Away Characteristics"
Takuto Yoshida, Craig Hudson, Test Tooling Solutions Group

"In-Situ Debug Techniques of SATA Connectors in Storage Servers – and Connector Degradation Phenomena"
Trent Johnson, Cleversafe, Inc.

"Investigation of Micro Spring Performance"
Jiachun (Frank) Zhou, Hui Liu, Smiths Connectors – IDI

"Testing Elastomer for HTOL"
Ila Pal, Meghann Fedde, Sultan Faiz, Ranjit Patil, Ironwood Electronics, Inc.

Session 4 – The Market is Open

"The Technical and Market Forces Shaping the Future of Test and Burn-In Sockets"
John West, VLSI Research, Inc.

"Socket Marketplace Report"
Fred Taber, Taber Consulting

"Manufacturing Readiness of Bond Via Array (BVA) Technology for Fine-Pitch Package-on-Package (PoP)"
Rajesh Katkar, Rey Co, Wael Zohni, Invensas

Session 5 – Sockets With Integrity

"High Bandwidth Sockets For SERDES Applications On ATE Load Boards"
Don Thompson, R&D Altanova

"Signal and Power Integrity Impact of Ground Slugs in Sockets"
Gert Hohenwarter, GateWave Northern, Inc.

"Building Blocks and Predictors for Good Contactor Signal Integrity"
Jeff Sherry, Johnstech International

Session 6 – Interconnectology: It's What We Do

"Long Life/Stamped Spring Probe Development"
Samuel Pak, A.J. Park, IWIN Co. Ltd.

"Validation Interconnect Socket – Application and Future Challenges"
Ashok Kabadi, Intel Corporation

"Crosstalk Mitigation in ATE Socket-Device Interface Boards"
Thomas P. Warwick, R&D Altanova, Inc.

Session 7 – Feel the Burn-In

"Massively Parallel Burn-in Test using IC Serial Buses"
Billy Fenton,OLAS Consulting, Pat Mitchell, Accutron

"Challenges of Increasing Parallelism in Burn-in Testing"
Yeow Hock Low, Infineon Technologies Asia Pacific

About The Author

Kevin Parmenter has over 20 years of experience in the electronics and semiconductor industry. Kevin is currently vice president of applications engineering in the USA for Excelsys Technologies. Previously, Kevin has served as director of Advanced Technical Marketing for Digital Power Products at Exar, and led global product applications engineering and new product definition for Freescale Semiconductors AMPD - Analog, Mixed Signal and Power Division based in Tempe, Arizona.

Prior to that, he worked for Fairchild Semiconductor in the Americas as senior director of field applications engineering and held various technical and management positions with increasing responsibility at ON Semiconductor and in the Motorola Semiconductor Products Sector. Kevin also led an applications engineering team for the start-up Primarion where he worked on high-speed electro-optical communications and digital power supply semiconductors.

Kevin serves on the board of directors of the PSMA (Power Sources Manufacturers Association) and was the general chair of APEC 2009 (the IEEE Applied Power Electronics Conference.) Kevin has also had design engineering experience in the medical electronics and military electronics fields. He holds a BSEE and BS in Business Administration, is a member of the IEEE, and holds an Amateur Extra class FCC license (call sign KG5Q) as well as an FCC Commercial Radiotelephone License.