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Topology Twists And Circuit Tricks Improve Performance Of Multi-Output Converters

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SEPIC, Ćuk, Zeta, flyback and inverting buck-boost converters are some of the most common "go-to" topologies when the buck and boost cannot quite do what is needed. After allowing for turns ratios and voltage inversion, they are all governed by the same relationship between voltage and duty cycle.

While there are many useful variations for producing one output, the group is particularly well suited for generating two or more outputs. The author has been working with these converters for many years, and in the process has developed some topology variations and techniques that can improve performance. This article describes some common and some less-well-known multiple-output buck-boost topologies, along with three favorite "tricks" that improve their performance. It also explains why these tricks work.

This article is intended for engineers with some power conversion experience. It is not intended to provide a complete design manual or a complete method for choosing or designing a power conversion topology. However, the information provided here may affect a designer's choice in topologies by showing ways to gain significant performance improvement.

For example, it may be possible to eliminate a switching voltage regulator (and avoid producing frequency "beats") by replacing two single-output types with one dual-output type. Obviously, this can also reduce cost or lower parts count. We will present five complete designs with test data and BOMs, as well as some other designs for which the concepts apply.

Tricks And Topologies

The three "tricks" discussed in this article can be summarized as follows.

1) Take at least *some* feedback to the control loop from all outputs.

2) Series connect the dc, don't just tap the winding.

3) Apply SEPIC (or Ćuk or Zeta) capacitor coupling to output windings.

The first trick is aimed at the control loop, while two and three are aimed at the "plant." We may think of the control loop as being analogous to the controlling "brains," while the plant is the "physical" capability of the power components. In general, neither can substitute for the other. A good power converter needs to be well-designed in the plant as well as the control loop.

Let's dive into the subject material with an ac-input isolated flyback design, which may be at least partially familiar to many experienced designers.

Fig. 1 is a tested triple-output flyback power supply. The blue shaded areas highlight "tricks" one and two as applied to this converter.

First, a couple of circuit notes:

- The ADuM3190 is an accurate secondary-side reference, error amplifier, and feedback isolator, which improves on the "old standby" combination of TL431 and optocoupler. R31 is the upper feedback divider for the +5-V output. It senses the output from a point before the output filter to help improve the feedback loop phase margin.

- Snubber R32-C29 is connected with the opposite orientation of R18-C13 and R19-C15 as shown in Fig. 1. This is because the snubber capacitors are 0603 chips while the snubber resistors are 1206 chips. The orientation should not affect performance; it was chosen for best fit in the PCB layout.

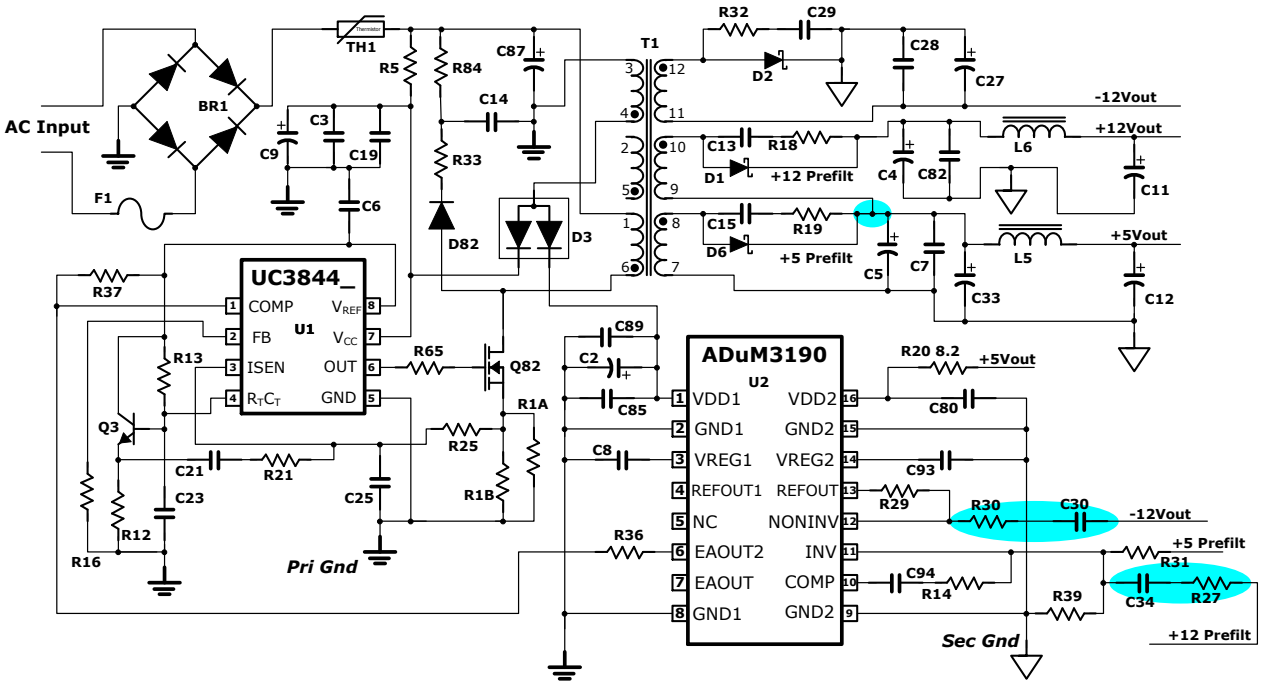

Fig. 1. Demonstration (it has no input EMI filter) flyback power supply as designed for 100- to 250-V ac input and triple outputs of +5-V and ±12-V and 25-W total output power. This converter runs at about 75 kHz. Blue shading highlights two (one is applied twice) of the three "tricks" used in this converter.

Trick #1: R27 and C34 (highlighted) couple ac feedback from the +12-V output while C30 and R30 couple ac feedback from the -12-V output. Why do we do this? Figs. 2 and 3 illustrate the reasons.

Fig. 2. shows measurements of the switch-node and +12-V output. In making these measurements, the loading on the power supply was very unfavorable. The -12-V output was loaded, the +5-V main output was unloaded and the +12-V output had a load varying between 0 and 2 A. Despite these severe loading conditions, the converter is stable as pictured. This stability can be attributed to the use of trick #1.

In Fig. 3, we see what happens when the feedback required for trick #1 is removed. In this case, the power supply becomes severely unstable.

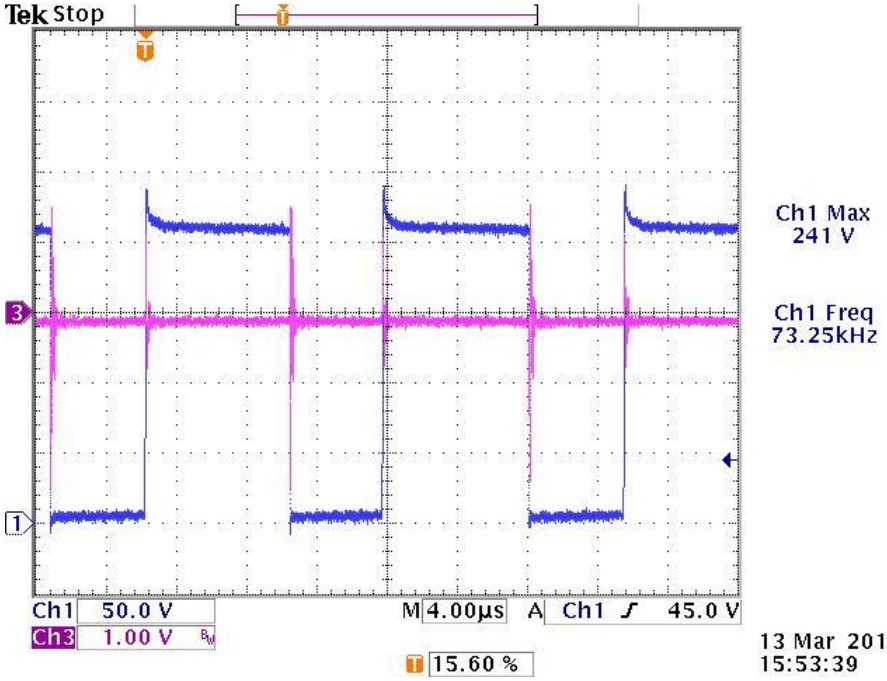

Fig. 2. In this photo, Ch1 is the drain of the main switch (Q82) and Ch3 is the +12-V output. This oscilloscope measurement does not show much; the point is that the converter is stable, built as shown, with some very unfavorable load conditions: The –12-V output is loaded, the +5-V main output is unloaded, and the +12-V output load current is anywhere from 0 to 2 A. If this converter did not include trick #1, these conditions would cause operation to become severely unstable as shown in Fig. 3.

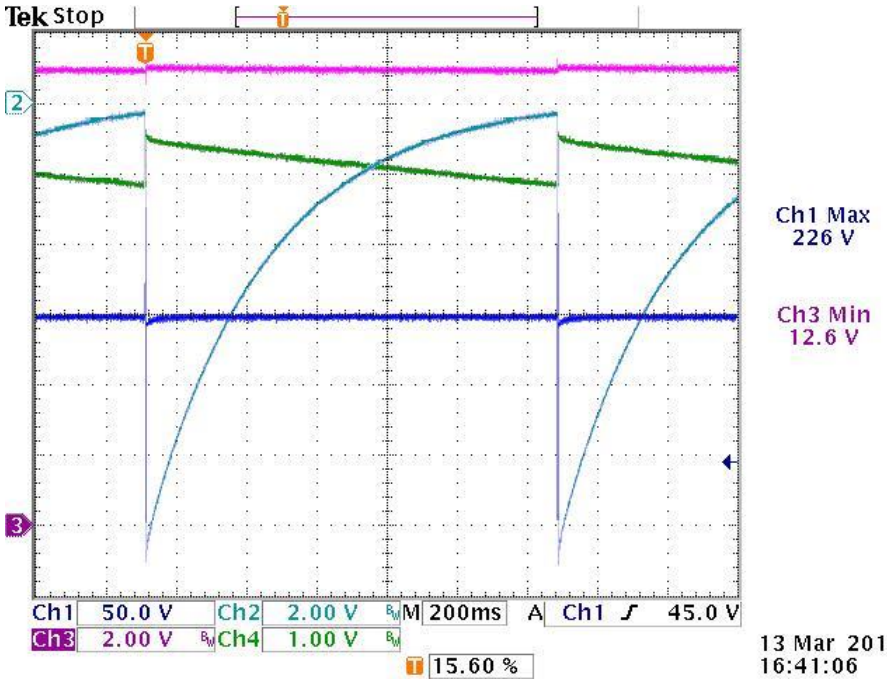

Fig. 3. After capturing the waveform in Fig. 2, I removed R27 and R30. Ch1 is the main switch drain, Ch2 is the -12-V output, Ch3 is the +12-V output, and Ch4 is the +5-V output. This is a severe example of what I call "multiple-output instability;" for this offline flyback, it is exacerbated by the hiccup/restart of the controller IC. Notice that we have about 12-V p-p oscillation of the -12-V output. For this measurement, the +12-V is unloaded. But with R27 and R30 disconnected, loading the +12-V does not resolve the instability.

Later in the article I will offer a diagnosis of this malfunction. But I will offer some key points here:

- You may have a converter that will seem to work acceptably with a severely imbalanced loading condition such as I have described, with little or no load on the "main, regulated" output. However, the important question is not whether the converter can run in a stable manner, but whether such operation is *assured*. The "acid test" is to try to induce instability and be unable to do so under any foreseeable load conditions. For this purpose, I recommend operating with "in-spec" full load on all outputs, and then *suddenly* disconnecting the load from the main output. It is common to find that a design that you thought was OK can be "kicked" into instability by this method.

- If you want to assure stability with any one output loaded alone, you probably need to provide feedback (ac or dc) from that output. If the output in question uses a linear post regulator, take your feedback from a point *ahead* of that regulator. When it is regulating, a linear regulator will decouple its output from changes at its input. You want to couple those changes into the switching converter's feedback loop.

- The usefulness of this technique is not subtle. Once you have identified it, it is clear and convincing for those many (not all) cases where it is applicable.

- Ac-coupled (as opposed to dc) feedback can be much easier to apply when working with negative outputs. Regardless of the output polarity, it is very helpful if you do not want to compromise the dc accuracy of the main output.

- Synchronous rectification with forced continuous-conduction mode (CCM) can also prevent multiple-output instability and eliminate the need for this added feedback. I will elaborate on this later.

Trick #2: I have highlighted the connection of transformer pin 9 (the +12-V winding) to the cathode of D6, which is the +5-V rectifier. This means that instead of connecting the two windings in ac series, we are essentially connecting a +7-V dc rectified output in series with a +5-V dc rectified output. The +12-V output current is passing through both the +5-V and +12-V rectifiers.

The reason for doing this is to get improved dc cross regulation between the two outputs.

Figs. 4 and 5 depict the relationship between +12-V output voltage and +5-V output current. In both figures, the blue line shows test results with the +12-V winding connected to the cathode of D6, while the red line shows test results with the +12-V winding connected to the anode of D6. (Fig. 4 is limited because with 2 A on the +12 V, we cannot draw much +5-V load before running into our 25-W power limit.)

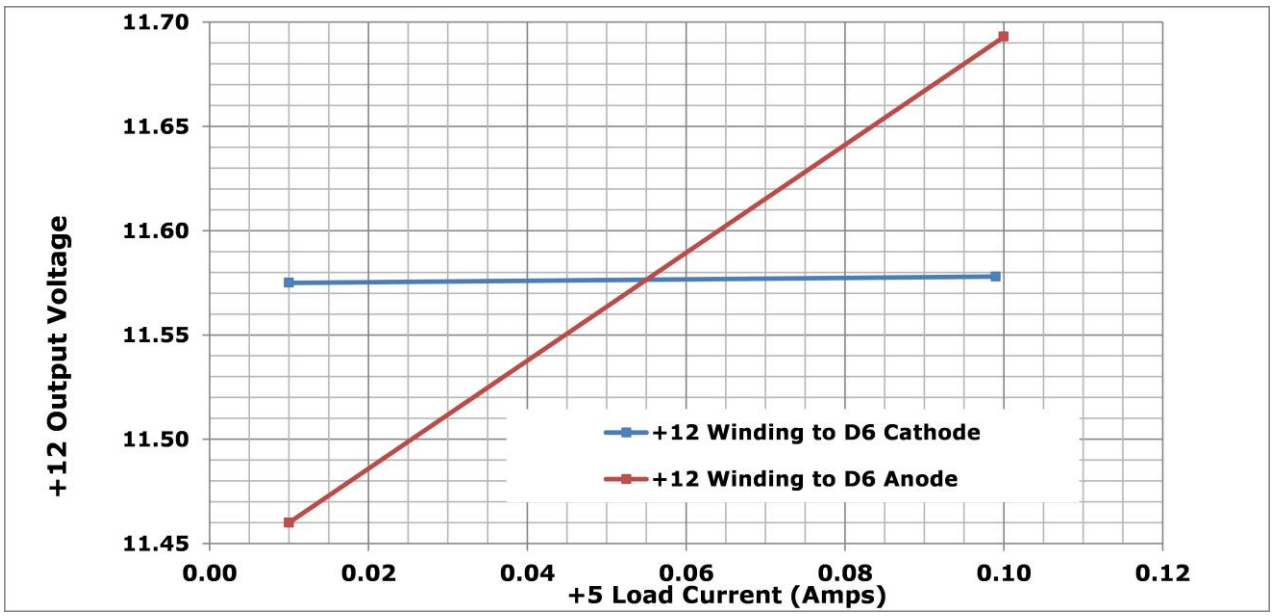

Fig. 4. Variation in +12-V out versus +5-V load current with 2-A load on the +12-V out, using two different connections of the +12-V winding.

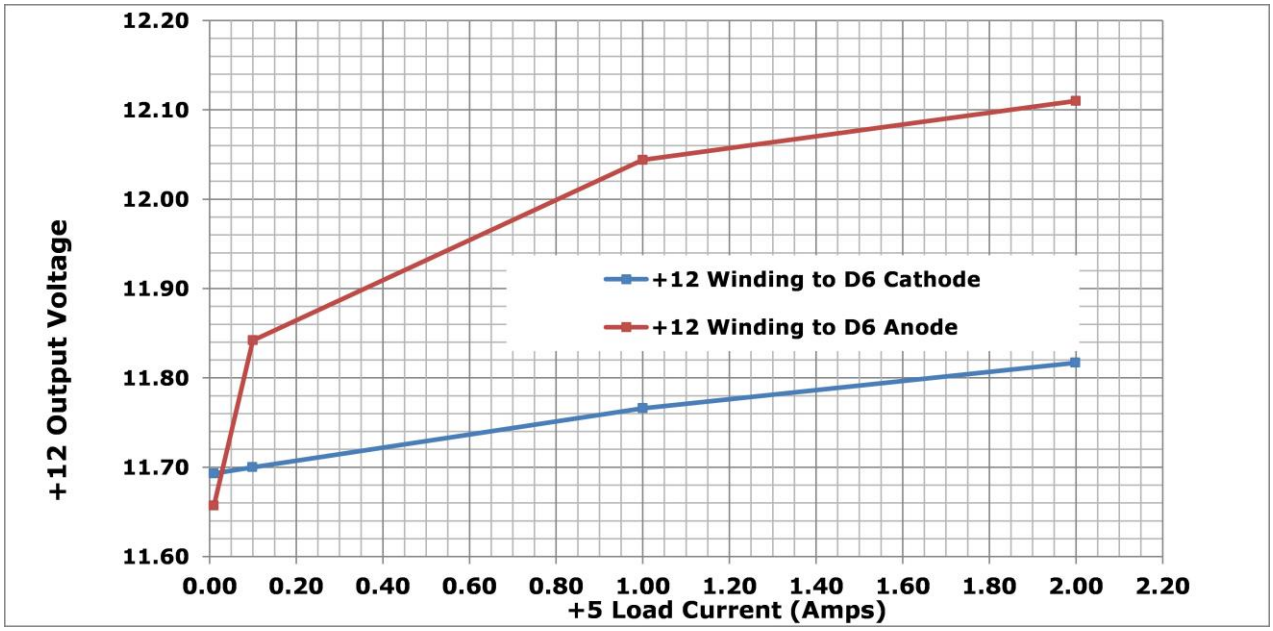

Fig. 5. Variation in +12-V out versus +5-V load current with 1-A load on the +12-V out, using two different connections of the +12-V winding.

Notice that the +12-V output voltage is much flatter for both +12-V load current values. Counterintuitively, the winding-to-cathode connection in Fig. 4 (blue line) actually delivers more +12-V output voltage (than does the winding-to-anode connection) when the +5-V output current is very low. This is because with the "usual" (anode) connection, the voltage drop through D6 is low when its forward current is low due to low +5-V current.

Because of this small voltage drop, the feedback loop can hold the +5-V output in regulation with reduced volts per turn out of the transformer. This reduced volts per turn out of the transformer causes the +12-V output to sag. With the +12-V winding connected to the cathode of D6, all of the +12-V output current flows through D6 and D1 thus increasing current and the voltage drop in D6. The converter needs to produce more volts per turn

out of the transformer in order to regulate the +5 V, thus causing an increase in the output from the +12-V winding.

If you need to maintain a minimum value of +12-V output under such adverse load conditions, the winding-to-anode connection (or stated otherwise, a tapped winding) might require a higher +12-V/+5-V turns ratio. This modification would increase the +12-V output voltage higher than desired for other, more-balanced load conditions, which would degrade efficiency.

The result is that the +12-V winding to +5-V cathode connection could help the designer to achieve a more-efficient design in spite of the +12-V output having two series diode forward voltage drops. I do not assert that this will always be the best approach, but rather that it is worth considering when trying to produce multiple outputs such as these.

Let's have a look at the next circuit example. Fig. 6 is a dual-output power supply that is built on the same PCB as that of Fig. 1. For purposes of clarity, most of the unpopulated component locations are not shown.

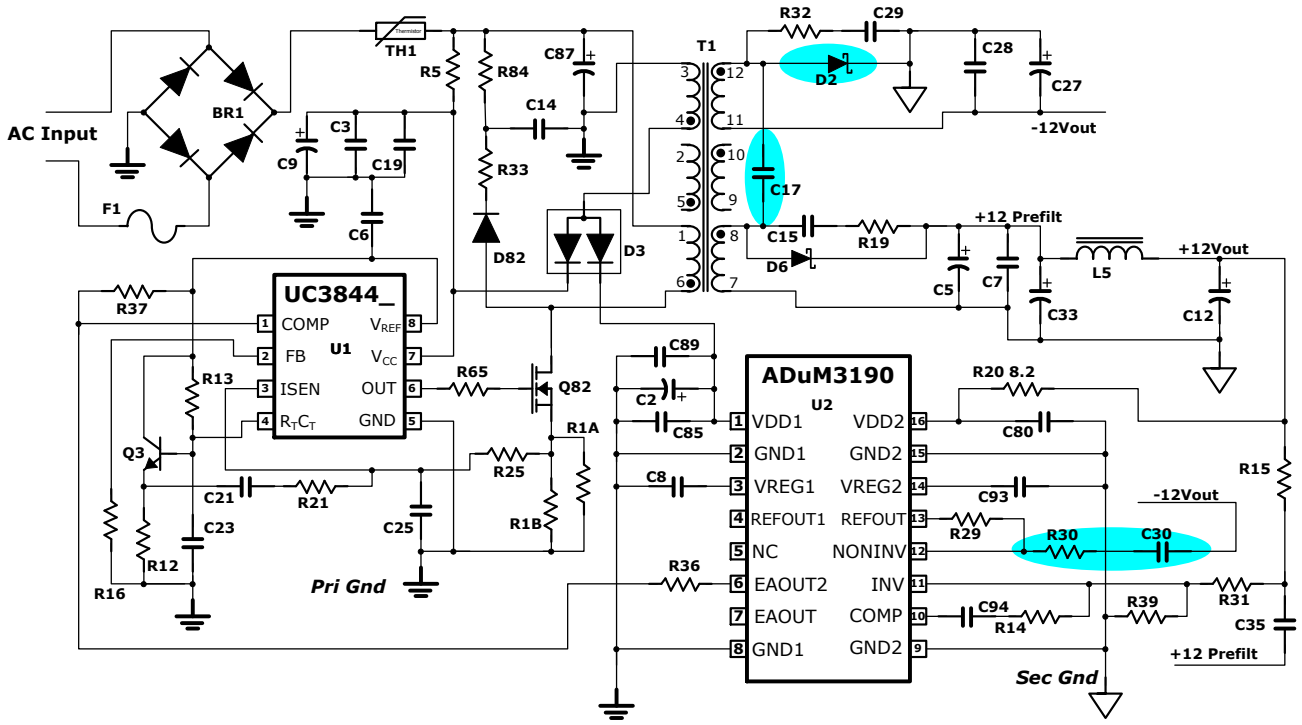

Fig. 6. Demonstration 100-V to 250-V ac input flyback power supply, producing ±12-V outputs of 36-W total output power. Blue shading highlights two of the included tricks. R30 and C30 implement trick #1, while C17 and the connection of the -12-V rectifier D2 implement trick #3. This converter runs at about 120 kHz.

This converter includes tricks #1 (obvious once you see it in the triple-output version) and #3. Similar to #2, the objective of trick #3 is cross regulation.

With its plot of load combinations listed in the table, Fig. 7 illustrates that we get much better voltage regulation out of the -12-V output when C17 is connected. (The windings and D2 must be connected as shown in order to use C17.) So, why do we see better regulation?

Ideally, a multiple-output flyback converter drives its multiple outputs with proportional voltage sources. Unfortunately, real circuits give us stray impedances, which serve to decouple this proportionality. These impedances intervene between the outputs and usually introduce load dependence.

Table. Load combinations used in testing the ±12-V flyback converter. Results are shown in Fig. 7.

Load Combination Number	+12-V out (A)	-12-V out (A)	Load Combination Number	+12-V out (A)	-12-V out (A)
1	0.01	0.50	7	0.50	0.01
2	0.01	0.02	8	1.00	0.01
3	0.10	0.02	9	2.00	0.02
4	0.10	0.01	10	2.00	0.01
5	0.20	0.01	11	3.00	0.02
6	0.50	0.02	12	3.00	0.01

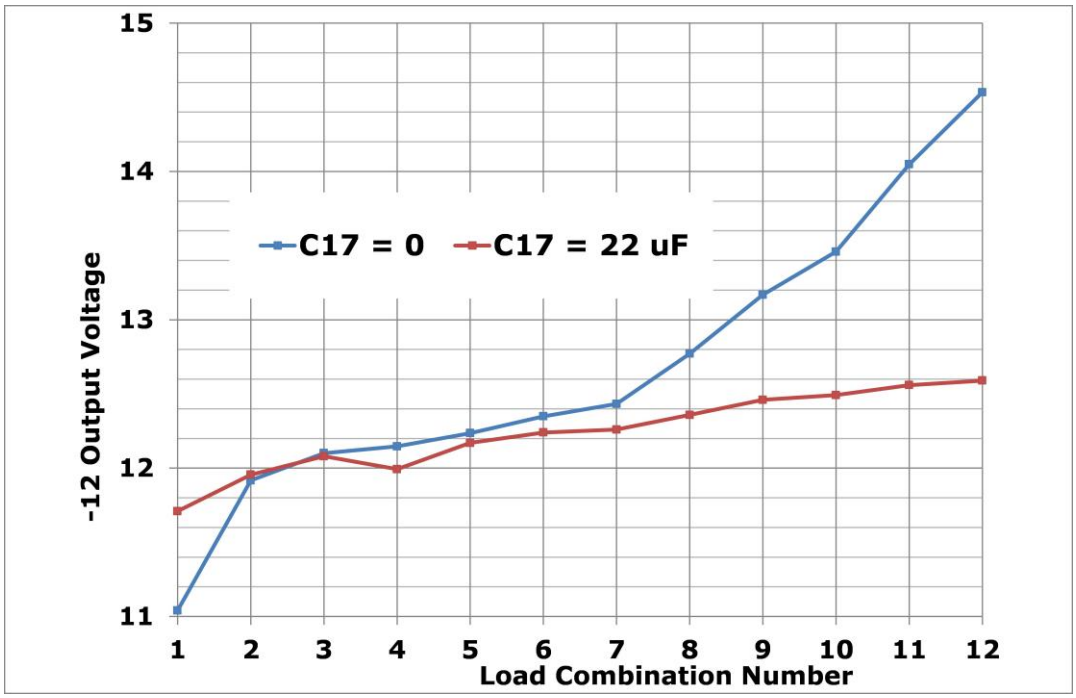

Fig. 7. For this graph, we tested the ±12-V output flyback converter using 12 different output load current combinations (listed in the table above), both with and without coupling capacitor C17. Because the dc feedback is tightly closed around the +12-V output, that output stayed within an 8-mV window and all significant dc voltage variation was in the -12-V output. We sorted the results without C17 in order of increasing negative 12-V readings. Then we plotted Vout versus the same load combinations for the data taken with C17 connected.

The sources of these stray impedances include ESR and ESL of the diodes, ESR and ESL of the PCB layout, and ESR of and leakage inductance between the transformer windings. In most typical multiple-output flyback designs, the winding leakage inductance is the largest contributor of error. It resonates with winding and diode capacitance to cause overshoot and ringing, and the output diodes feeding lightly loaded outputs peak-rectify the resulting overshoot. The result is that lightly loaded output voltages rise relative to the more heavily loaded ones and the voltage proportionality is degraded.

In fact, this modification involving D2 and C17 is a significant topological change. In the original design, the two outputs are transformer coupled. We require dc + ac fidelity in the voltage waveform produced by the transformer winding. The magnetic coupling needs to be tight for this to work well; winding leakage inductance will degrade the cross regulation. But if we apply a large enough value of C17 with sufficiently low impedance,

we could insert a large amount of leakage inductance in series with the -12-V winding and have the output regulate well.

In fact, we could replace the -12-V winding with (a discrete inductor with no magnetic coupling to the transformer; equivalent to infinite leakage inductance) and have it work well. The -12-V output then works like that of a Ćuk converter, which is what it is. With both windings on one transformer core, you have a coupled-inductor Ćuk output.

In a coupled-inductor Ćuk, the magnetic-coupled waveform on both windings should be identical, so that the capacitor has no (ideal and simple analysis) ac voltage across it. In other words, the turns and the phase of the two windings should be the same so that the ac voltages match and they are not trying to drive significant ac current through the coupling capacitor. The -12-V winding conducts the dc current and the coupling capacitor conducts the ac current.

In order to keep LC resonant frequencies low enough, very low leakage inductance can require a large value capacitor, so the tightest possible coupling (lowest possible leakage inductance) is not necessarily ideal. This point is not likely to be a big design problem, any more than adding leakage inductance between transformer windings is likely to be difficult.

The triple-output converter (Fig. 1) cannot use trick #3 when the +12-V winding is connected to the cathode of D6. This is because the +12-V winding is working as a 7-V winding with a +5-V dc offset, while the negative 12-V winding is working as a 12-V winding. The two windings have different turns and different ac voltages, so coupling the +12-V and -12-V rectifier anodes with a capacitor would place an ac short across the transformer.

For our next example circuit; let's do another ±12-V output; but this time it is a nonisolated SEPIC/Ćuk combination (Fig. 8.)

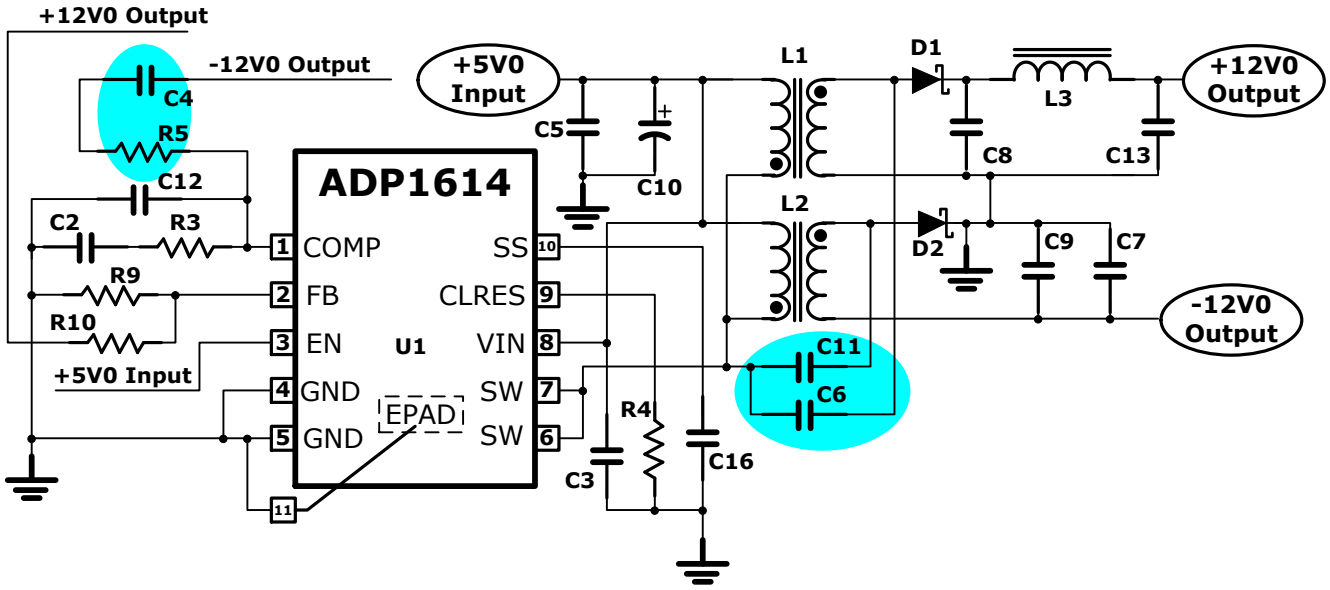

Fig. 8. 5-V input to ±12-V 250-mA output SEPIC-Ćuk converter. C4 and R5 implement trick #1 by ac coupling the negative output into the compensation pin. C6 and C11 implement trick #3 (which is included in any SEPIC or Ćuk.) A bill of materials for this circuit is included in the appendix of this article.

Fig. 8 is the schematic for a SEPIC/Ćuk converter with ±12-V outputs. This takes a +5-V dc input and converts it to ±12-V dc at up to 250 mA. R9 and R10 are the feedback divider for the main (+12-V) output. In theory, our converter could alternatively sense either the -12-V output alone or the total 24-V output differential, but these options would require some added parts such as an op amp. Barring instability, the dc load regulation on the unregulated output of a well-designed SEPIC/Ćuk is adequate for many purposes, and a single control loop can *tightly and directly* regulate only one output anyway, regardless of the converter topology.

In this topology, the main switch (internal to the ADP1614) is subjected to (adding magnitudes; forget about polarity) Vin plus (either Vout). With 5-V input and 12-V output we have 17-V peak on the main switch, which in the ADP1614 is rated at 20 V.

With this design, trick #1 uses ac feedback from the "unregulated" negative output to the compensation pin. Doing this provides the correct feedback polarity for this negative output but requires that the IC's error amplifier be a transconductance type.

Because there is no accurate dc reference associated with the error amplifier output at the compensation pin, dc errors would be difficult to avoid if we used dc coupling. This ac-coupled signal tells the feedback loop in which direction the unregulated output is headed at any moment but does not affect the dc regulation point. If the unregulated output is falling or climbing rapidly while the regulated output is relatively stable, that output voltage slope information turns out to be very useful.

Fig. 9 is an illustration of multiple-output instability with the SEPIC-Ćuk. Unlike the similar misbehavior shown in Fig. 3 of the UC3844 ac-input flyback, the IC is continuously "awake" with no hiccup-restart cycle to contribute to the malaise. R5-C4 was disconnected in order to produce this instability. An initial perturbation *may* be required in order to upset the feedback loop, so a designer might miss seeing the malfunction if testing is not thorough. The perturbation can be a sudden application of the load on the unregulated output or a sudden removal of the load on the regulated output for example.

For the oscilloscope shot shown in Fig. 10, operation is stable. All conditions are the same as Fig. 9, except that the R5-C4 pair is connected as shown in Fig. 8. With these components providing feedback from the -12-V output, the control loop can no longer be upset with load current or input voltage perturbations. Although the test conditions and the oscillation are severe, there is no exaggeration here. The improvement from adding a small RC pair as shown can be dramatic. Figs. 11 and 12 show more details of the oscillation.

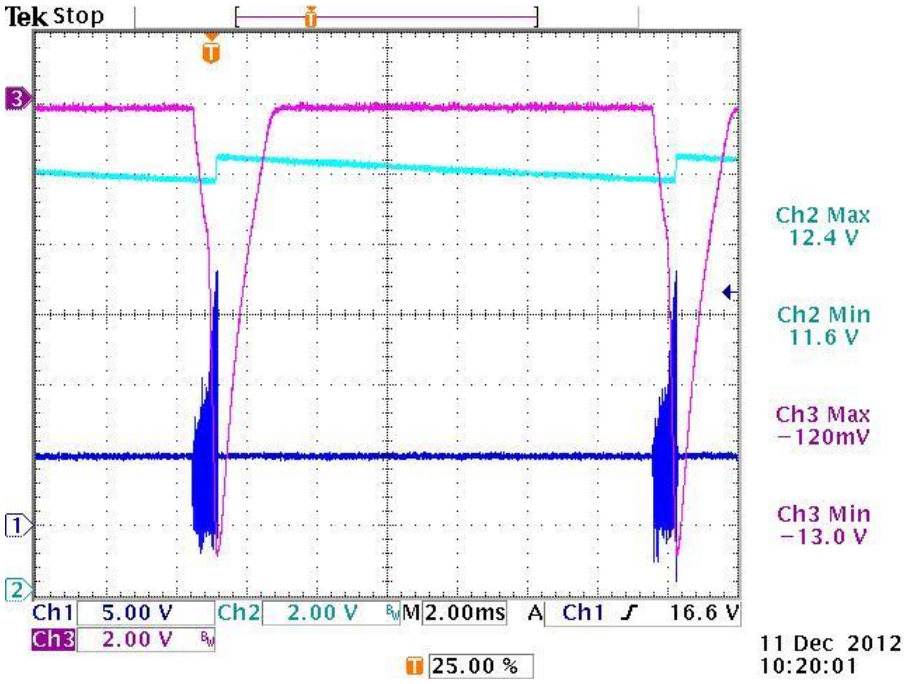

Fig. 9. This is a measurement of multiple-output instability in the SEPIC-Ćuk converter, which was induced by disconnecting C4 and R5. We are testing with a severe "corner condition": 150-mA load on the unregulated -12-V output and no load applied to the +12-V output. Ch1 is the main switch node, Ch2 is the unloaded +12-V output, and Ch3 is the negative output with 150-mA fixed, constant-current load.

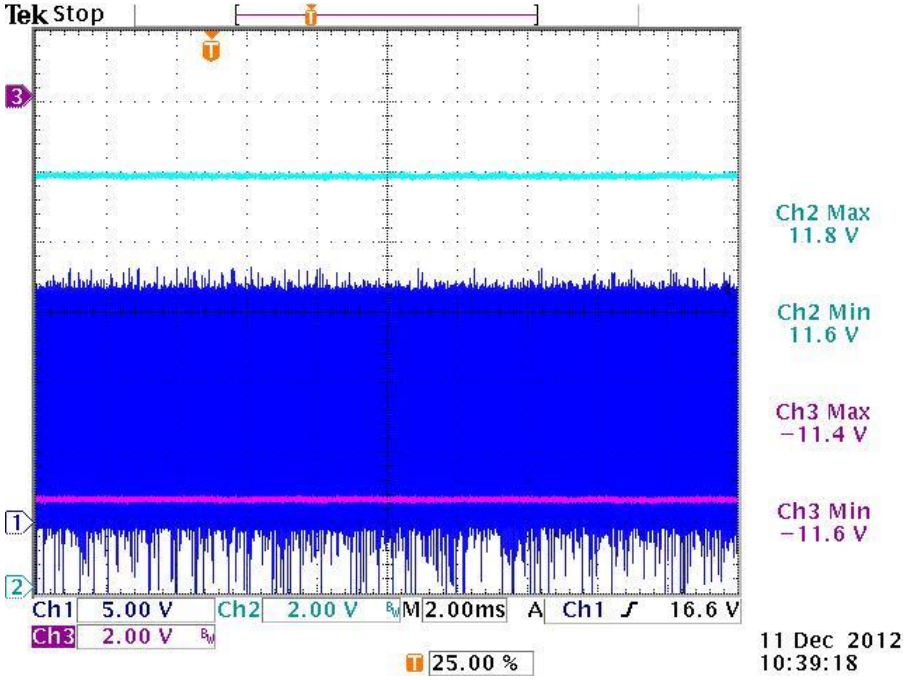

Fig. 10. This measurement was taken under the same conditions as Fig. 9, except that C4 = 1 nF and R5 = 100 kΩ are connected as shown in the schematic diagram. The output is now stable and cannot be upset by momentary load-current or line-voltage perturbations. Positive Vout = 11.993 V and negative Vout = 11.230 V, which is 6.4% low. This is reasonably good in light of a severe worst-case "corner condition" loading and an unregulated output.

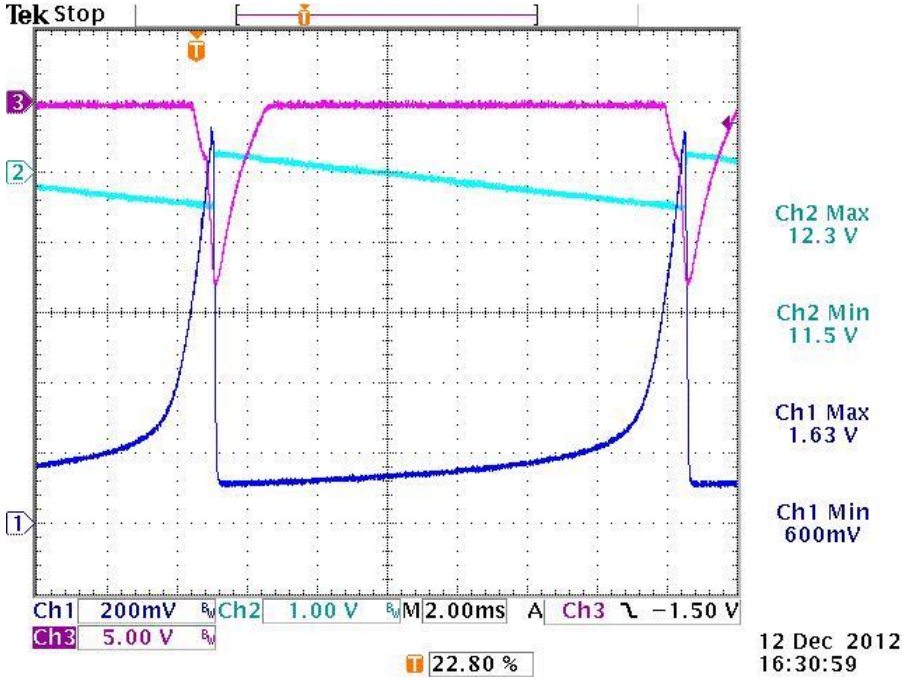

Fig. 11. Similar to Fig. 9 but oscilloscope Ch1 is connected to the COMP pin of the controller IC; also the scale factor on Ch3 (-12-V output) has been changed to make Ch1 more visible. Ch2 still indicates the +12-V output.

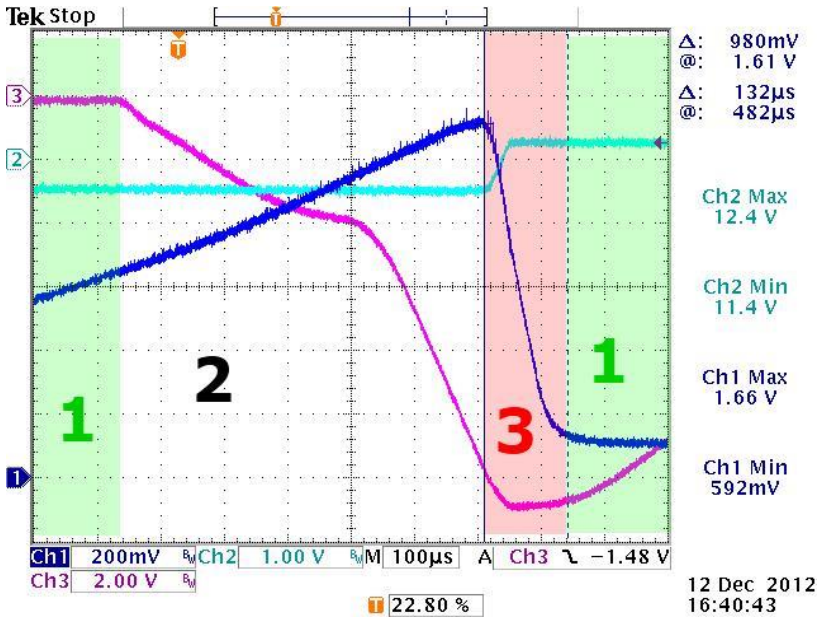

Fig. 12. This is a faster-timebase acquisition of Fig. 11 , with shaded areas to indicate phases of the oscillation waveform. These phase numbers are explained below.

Multiple-output buck boost converters achieve their slaved-output regulation due to fixed ratios of voltage sources connected via the rectifiers to the outputs. These fixed ratios result from regulated volts-per-transformer-turn in a flyback or the identical ac driving waveform coupling through a capacitor in a SEPIC or Ćuk for example. However, during a "pulse skip," this ac voltage momentarily collapses and the multiple outputs become unlinked as the rectifiers become reverse biased. If the voltage on the unregulated output drops way below the expected regulation band during this time, the control loop will typically not know about it and will not quickly respond to correct the error.

The following describes the chain of events causing the oscillation shown in Fig. 12.

Waveform section 1. The control loop and the regulated output have overshot for some reason and a pulse skip has initiated. The unregulated output is fully loaded so that its voltage magnitude drops rapidly when it is unsupported by the converter output. Meanwhile the main output has a very light load so its output capacitor sustains the overshot output voltage, which is still slightly above the feedback regulation point, and the controller does not quickly resume pulses. The feedback loop is telling the controller "output is too high; deliver no power." Remember that our unregulated output is negative so the flat top of Ch3 towards the left side of Fig. 12 is its minimum magnitude.

Waveform section 2. Eventually the main output voltage sags enough (and the COMP voltage inside the IC rises enough) to command a resumption of pulses, but by this time the fully loaded unregulated output has dropped far under the regulation band. In our example it has decayed to nearly zero. When energy transfer resumes, the unregulated output clamps the transformer output to its (now lower magnitude) voltage so that the main output rectifier remains reverse biased. The unregulated output's filter capacitor gets all of the output energy and none is delivered to the main output. The main output drops further as the control loop commands "more power" and it charges the unregulated output filter capacitor as fast as possible.

Waveform section 3. By the time the unregulated output approaches the normal regulation band, the converter is delivering full power and may be in current limit. At this point, the converter begins to deliver energy to the main output, but because the error amplifier output is at its maximum, it cannot swing back to a stable point fast enough and the main output voltage overshoots. The control loop then reacts by swinging to its minimum and shuts down the PWM output. This initiates another pulse skip, and the cycle repeats.

Another observation: This oscillating scenario takes us outside the realm of linear systems. We have one disconnect between the main output–plus-feedback loop and the unregulated output during a PWM skip, and a second such disconnect when the unregulated output magnitude is rising rapidly. These discontinuities give us a nonlinear system, so an analysis which is limited to linear systems will not explain it properly. However, as is often the case with unstable feedback loops, there is a causal relationship, which involves a phase lag between the output voltage and the feedback. The additional feedback that is provided by C4 and R5 bypasses most of that phase lag.

Synchronous rectifiers are capable of conducting current in both directions. Some synchronous-rectified control ICs (such as the ADP2442) are capable of operating in "forced CCM" so that you get no pulse skipping (thus no significant time when the outputs are decoupled from each other.) The bidirectional conduction can permit a large conduction interval to the "main" output without the need to pass significant dc current. So ICs with synchronous rectification and forced CCM can often avoid multiple-output instability without the need for feedback from the additional outputs.

Our "subject" approach to eliminating this instability is to inform the feedback loop as soon as possible that the output voltage magnitude is changing. In linear terms, this would reduce the feedback lag, which is an essential component of the severe oscillation. Applying a small amount of ac feedback from the unregulated output accomplishes this goal without affecting the dc accuracy of the main output.

Some engineers may observe that taking feedback from two points in the output makes it difficult to analyze the resulting linear network stability. I do not want to argue that issue here. However a *relatively small amount of ac coupling* added from the secondary output can make this undesirable mode completely vanish. Seldom have I seen such a small and inexpensive remedy (one small series RC) so dramatically resolve a problem.

This added feedback coupling will typically have some effect on the transient load response waveform. However, using very light coupling (small-value capacitor and high-value series resistor) can minimize any conceivable deleterious effects without sacrificing the desired stability. The effect on transient load response may in fact be favorable.

It is possible that if you have a very good simulator with excellent models, the circuit values may be calculated with that. But if you do not have adequate faith in your simulation then resolving it on the bench may well be better. Just be sure to margin your component values so that normal variation will not send your design into trouble. Plan on minimizing the added feedback coupling from the unregulated output.

Given that defining and measuring the feedback loop response with two or more feedback points is not straightforward, I use the following methodology to insure stability.

Step 1. With only main feedback connected, design the feedback loop as would normally be done, assuring good gain and phase margins. Use high dI/dt speed load switching to measure and record the converter load transient response. Our purpose in this test is to observe the converter as a linear system; not to push it into multiple-output instability.

Be careful here; many electronic loads are not capable of switching fast enough to excite the loop at frequencies near unity gain crossover, so a discrete test circuit using a square wave or pulse generator to switch a MOSFET and load resistor may be required. With the transient load applied to only one output at a time, perform this testing on all outputs. Measure all outputs for every test, and try different static load combinations as this may turn up some surprises.

Step 2. Test to see whether the converter is vulnerable to multiple-output instability. Most often a full load on an unregulated output together with an unloaded main output is most likely to trigger the issue. You may need to suddenly disconnect the load on the main output.

Step 3. Experimentally determine how much coupling from the nonregulated output is required to prevent the problem. Start off coupling with a relatively high capacitor value and low valued resistor. In the circuits, which I have been using; sample starting values would be 20 kΩ and 100 nF. Assuming this combination fixes the problem, first start increasing the resistor value to find the maximum effective value; then cut that by about half to provide some margin. Second, do the same with the capacitor; start decreasing to find the minimum effective value; then double it.

Step 4. Now repeat the dynamic load response tests. You may find improvements in the response waveforms as I often see. I have never seen evidence of significant degradation of the gain or phase margin.

Figs. 13 through 16 show the measured response (on both outputs) of dynamic loads applied individually to both outputs of the SEPIC-Ćuk converter, both with and without trick #1.

Figs. 17 and 18 show the measured output dc load and cross regulation of the SEPIC-Ćuk Converter.

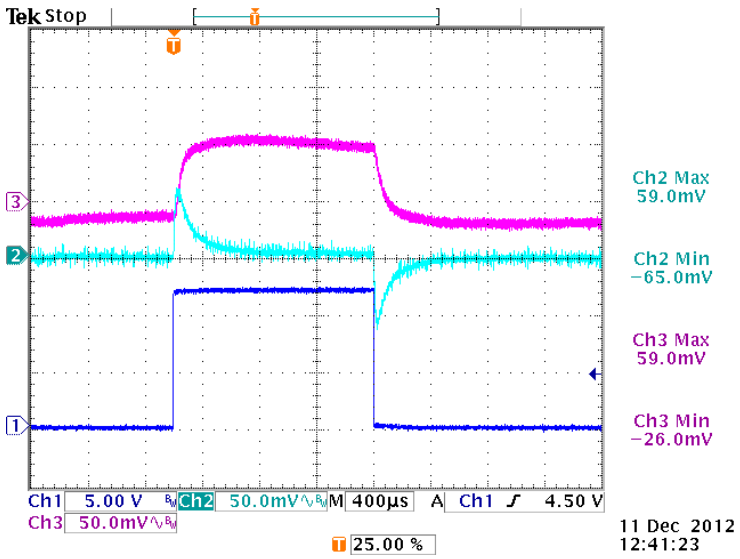

Fig. 13. Here we are switching a 207-Ω load (about 58 mA) to ground from the positive output of the SEPIC-Ćuk converter. R4-C5 are connected for this test. Ch1 indicates the drain of the load switch FET. Ch2 shows the +12-V output voltage and Ch3 shows the -12-V output voltage. The +12-V output has an additional fixed 20-mA load and the -12-V output has a fixed 150-mA load.

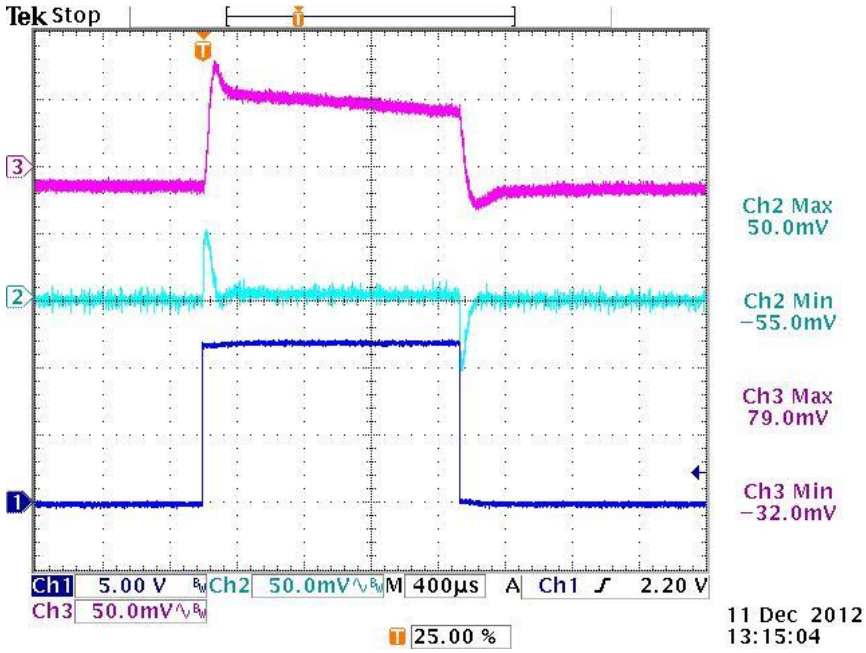

Fig. 14. In this measurement, we have duplicated the test shown in Fig. 13, but R4-C5 are disconnected.

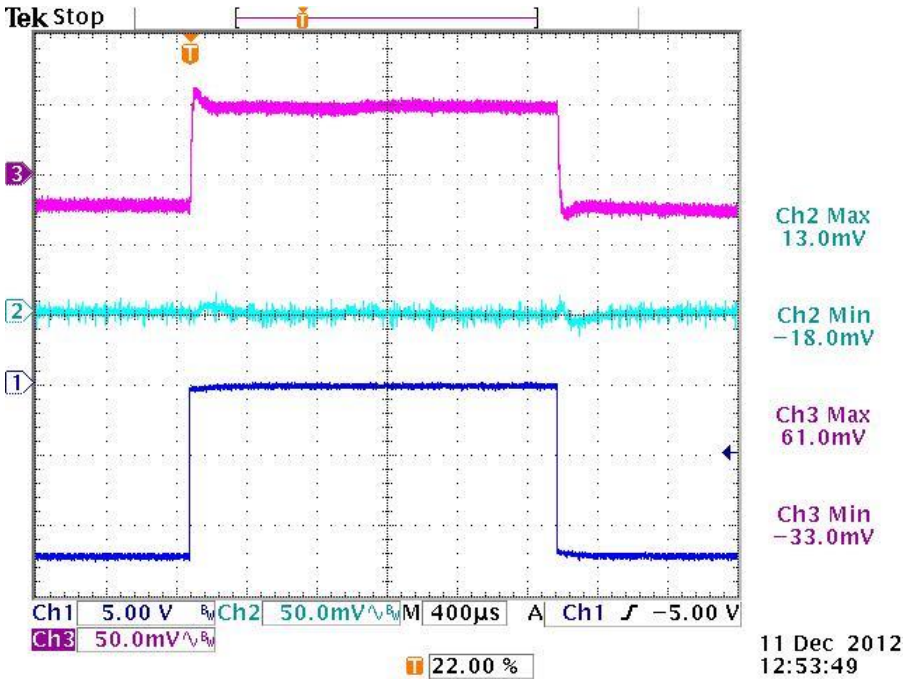

Fig. 15. Here we are switching a 207-Ω load (about 58 mA) to ground from the negative output of the SEPIC-Ćuk converter. The R4-C5 pair is connected for this test. Ch1 indicates the drain of the load switch FET. Ch2 shows the +12-V output voltage and Ch3 shows the -12-V output voltage. The -12-V output has an additional fixed 20-mA load and the +12-V output has a fixed 150-mA load.

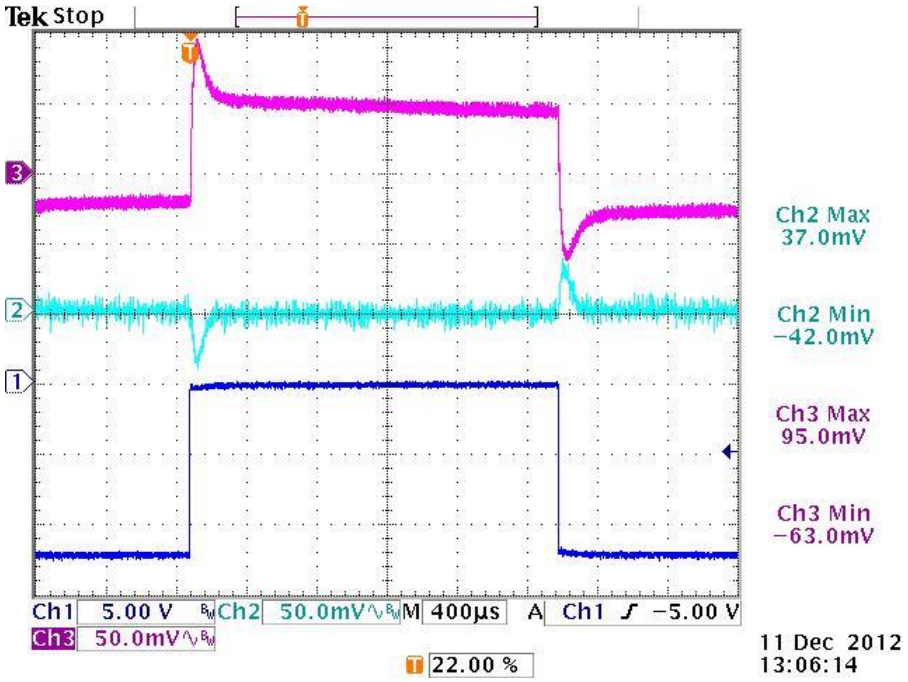

Fig. 16. This measurement repeats the test shown in Fig. 15, but with R4-C5 disconnected.

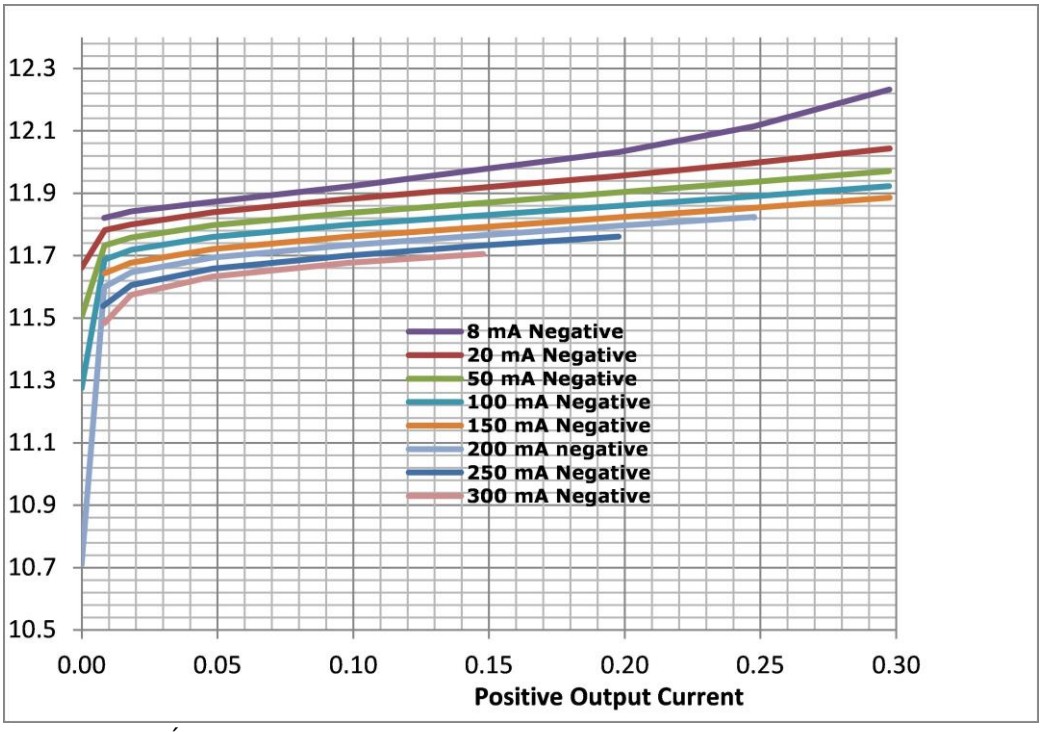

Fig. 17. SEPIC-Ćuk measured negative Vout versus positive Iout, for different values of negative Iout.

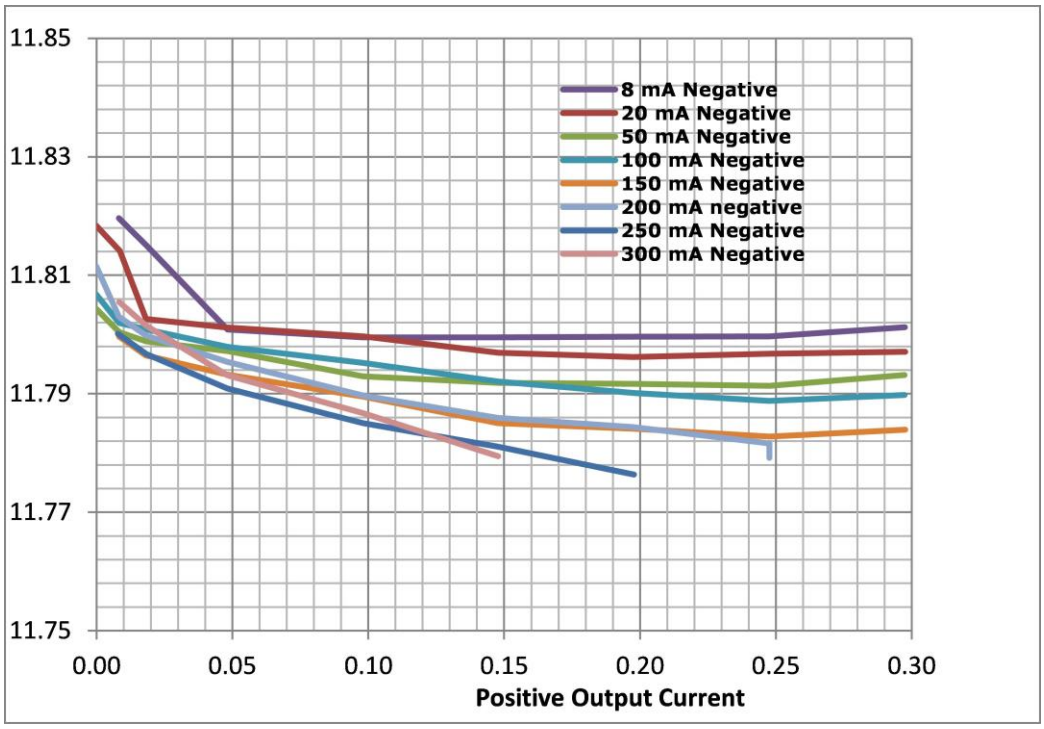

Fig. 18. SEPIC-Ćuk measured positive Vout versus positive Iout, for different values of negative Iout.

Next is a brief detour in the direction of multiple-output buck-boost converters, which can be built similar to the SEPIC-Ćuk (such as with an ADP1614 IC.) The converters shown in Figs. 19 and 20 both lend themselves to all three "tricks." Both produce output voltages with a 2:1 ratio. In exchange for these rigid voltage ratios, you get

better voltage regulation than you would get from a design that sets output voltage according to transformer turns.

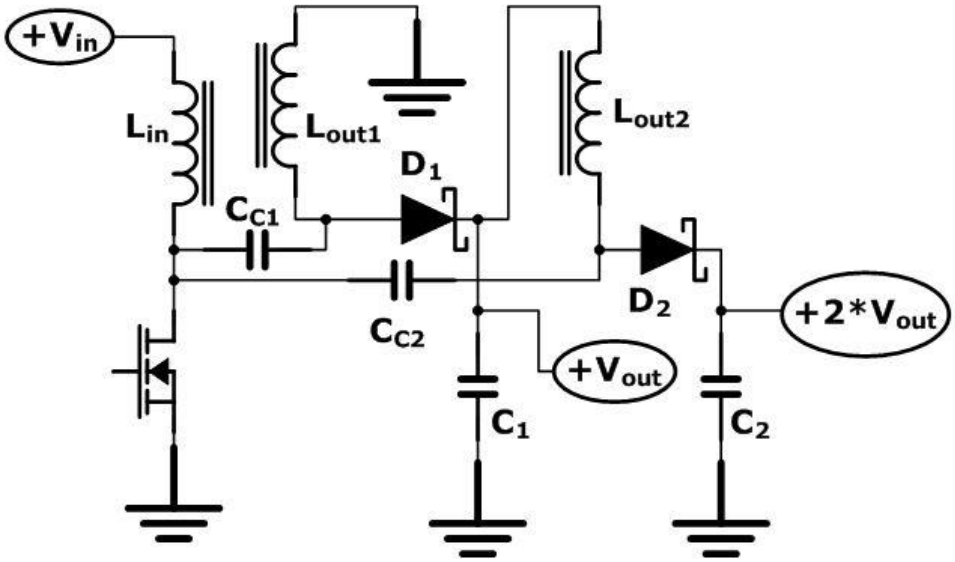

Fig. 19. This is a dual-output SEPIC. This happens to be built with three inductors but it could alternatively be built with two coupled inductors. It could take 4- to 7-V dc input (for example) and produce +6-V and +12-V dc outputs. Once we include an appropriate control loop, we can implement all three "tricks."

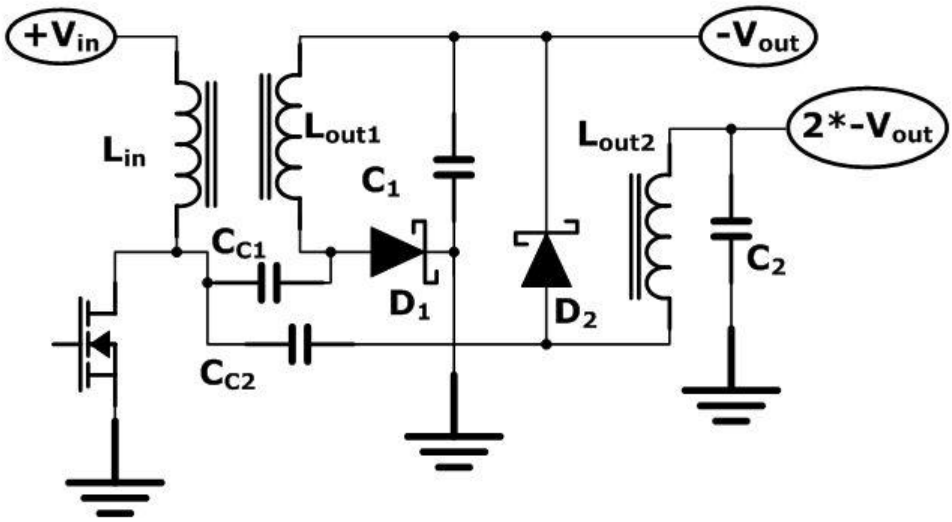

Fig. 20. This is a dual-output Ćuk with capabilities roughly comparable to the dual-output SEPIC shown in Fig. 19, but output voltages are negative. This topology can also use all three "tricks."

Now back to our subject of multiple-output converters producing symmetrical positive and negative output from positive input, here is another way. As shown in Fig. 21, it is a combination inverting buck-boost/Zeta.

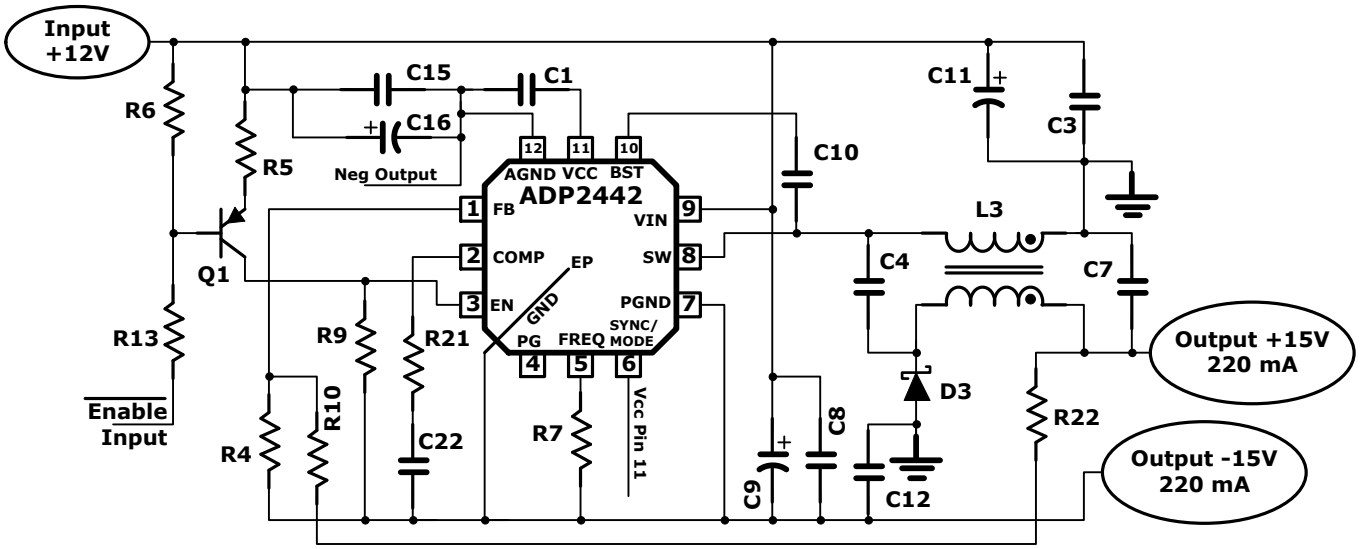

Fig. 21. A combined inverting buck-boost/Zeta converter based on the ADP2442 produces two symmetrical rails using only one dual-winding coupled inductor. This design uses trick #1 by taking feedback from the difference between the two outputs, and trick #3 thanks to its Zeta converter design.

In the Fig. 21 circuit, the ADP2442 provides synchronous rectification for the main (-15-V) output. With pins 6 and 11 connected as shown, we have forced PWM operation. As a result, this converter should be well protected against multiple-output instability. Further insurance is provided by the R10-R4 feedback divider sensing the +15-V to -15-V differential. The control loop is really regulating 30 V. If we reconnect R10 to ground (instead of +15 V) and adjust the divider ratio accordingly, then the -15 V will be tightly regulated and the +15 V will be the "added" output, which is slaved to the -15 V.

Figs. 22 and 23 show the measured load/cross regulation of the two outputs. There is a symmetry to these two sets of graphs; this is due to the fact that the differential between the +15 V and -15 V is tightly regulated by the feedback loop. If one output climbs by 100 mV, the other must fall by a similar amount when the feedback loop is working properly.

In this type of converter, the IC ground pin is not connected to system ground; rather it slews to -15 V as the converter starts up. Q1, R5, R6, and R13 scale and level shift the IC "precision enable/UVLO" function so that the R13 enable responds to the +12-V dc input level and/or an inverted, ground-referenced enable signal. If the R13 input is wired to ground, you get a simple input undervoltage lockout. If it is switched to ground, you get the input UVLO function combined with a low-going enable control.

The ADP2442 is rated for 36 V maximum, measured from its Vin pin to its ground pin. In this application, the IC Vin pin is at +12 V and the ground pin is at -15 V, so it is subjected to a 27-V differential. This is well within its ratings.

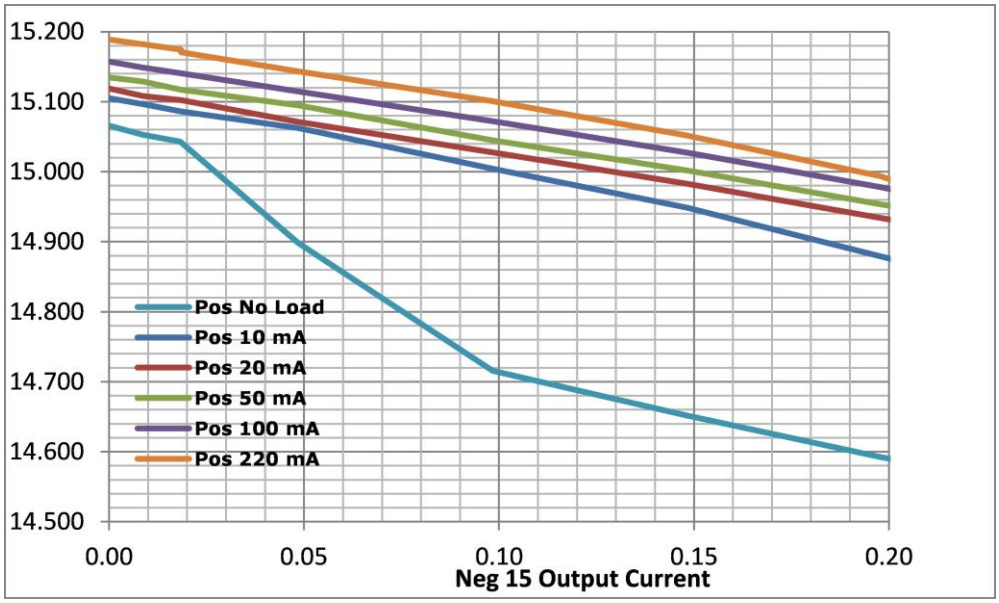

Fig. 22. The ADP2442 inverting buck-boost/Zeta measured negative Vout versus negative Iout, for different values of positive Iout.

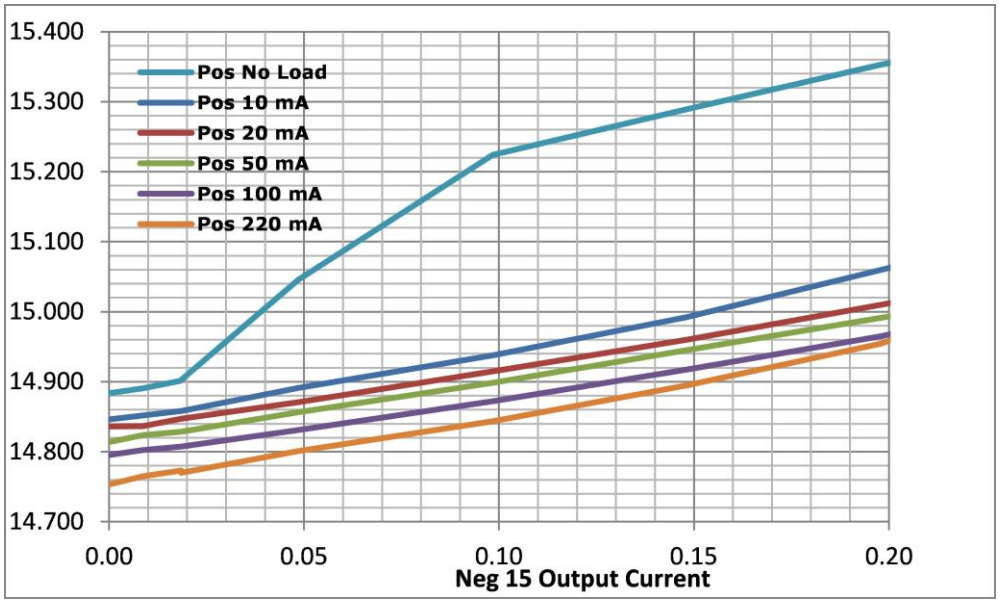

Fig. 23. The ADP2442 inverting buck-boost/Zeta measured positive Vout versus negative Iout, for different values of positive Iout.

Fig. 24 shows another inverting buck-boost/Zeta, similar to Fig. 21 but using the ADP2301. In this circuit, freedom from multiple-output instability is assured by feedback from the 24-V output differential. (Trick #1, feedback is taken from both outputs.) The Zeta output uses trick #3. The ADP2301 is capable of handling 20 V so this conversion fits it nicely.

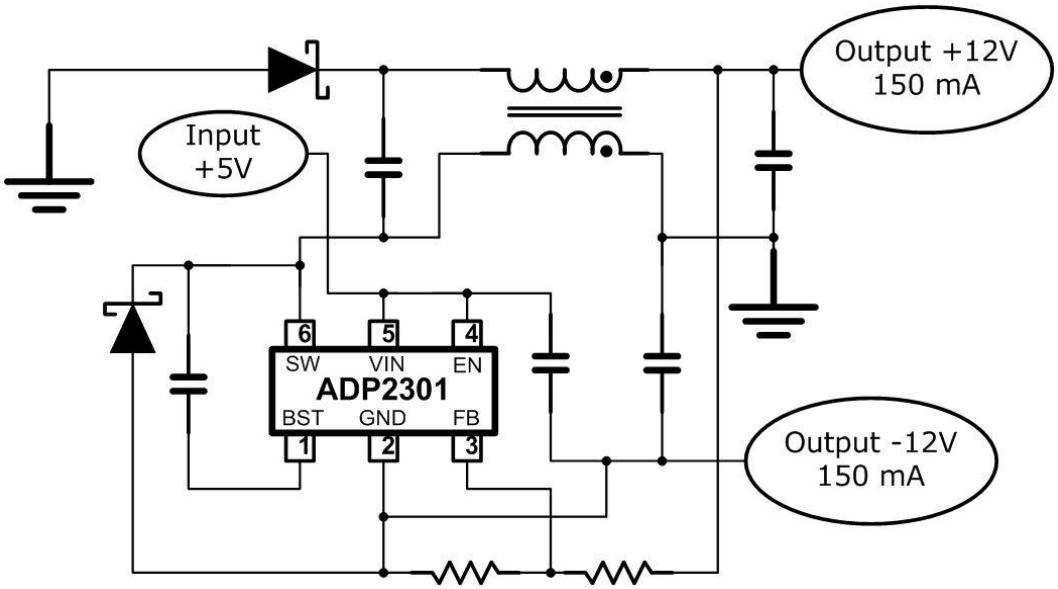

Fig. 24. An inverting buck-boost/Zeta converter based on the ADP2301. In this circuit, freedom from multiple-output instability is assured by feedback from the 24-V output differential.

I am not recommending a dual negative output configuration with the ADP2301 as I do below with the ADP2442. Because the ADP2301 has neither an accessible transconductance-type COMP pin nor forced-CCM capability, the dual-negative output topology will be more susceptible to multiple-output instability unless more complex feedback is used.

Fig. 25 shows a variation on the circuit in Fig. 21 (the two were tested on the same PCB design.) Instead of producing one negative and one positive output, we produce two negative outputs.

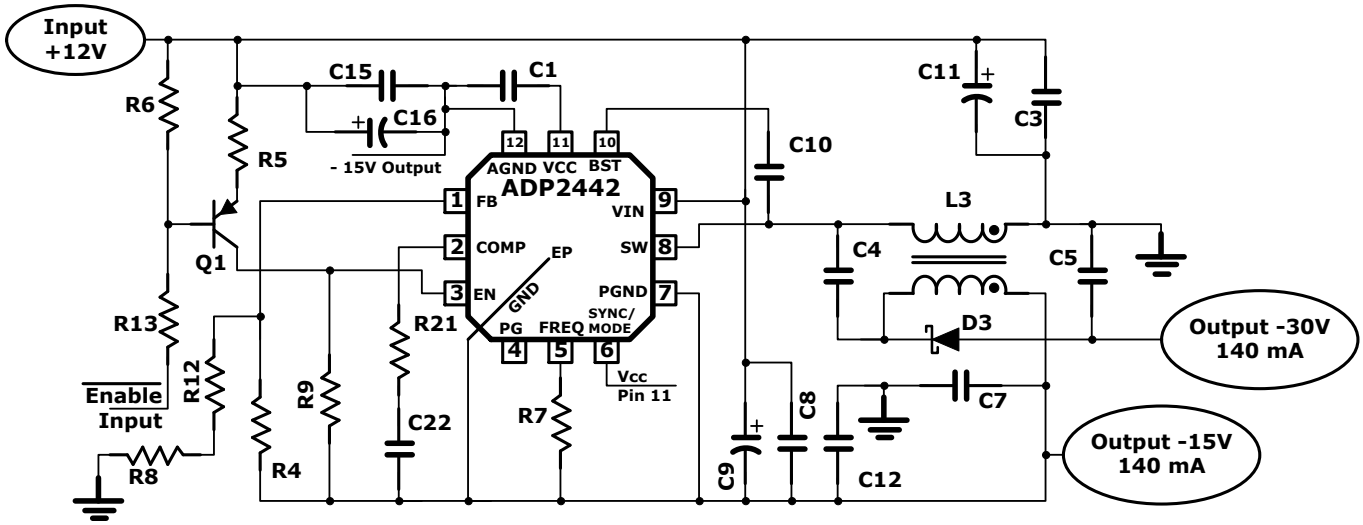

Fig. 25. Dual-negative output, inverting buck-boost using the ADP2442. Capacitor coupling (trick #3) between inductor windings helps this converter to produce dual outputs that track better than tapped inductors would. Forced-CCM operation (pins 6 and 11 tied together) allows this configuration to behave well without exhibiting dual-output instability. Do not couple the -30-V output into pin 2 COMP; this can cause improper operation.

Figs. 26 and 27 show the voltage regulation out of the dual-negative buck-boost. The -15-V regulation shown in Fig. 26 looks erratic, but in fact the output is tightly regulated within a < 0.1% window. I magnified the vertical scale so as to show what little variation there is.

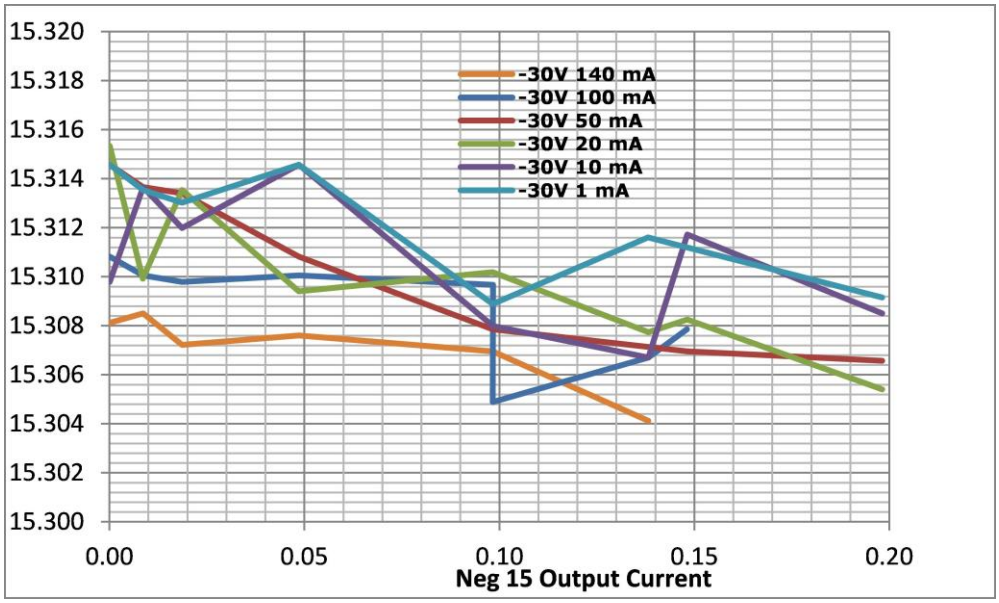

Fig. 26. The ADP2442 dual negative output, inverting buck boost measured -15-V Vout versus -15-V Iout, for different values of -30-V Iout.

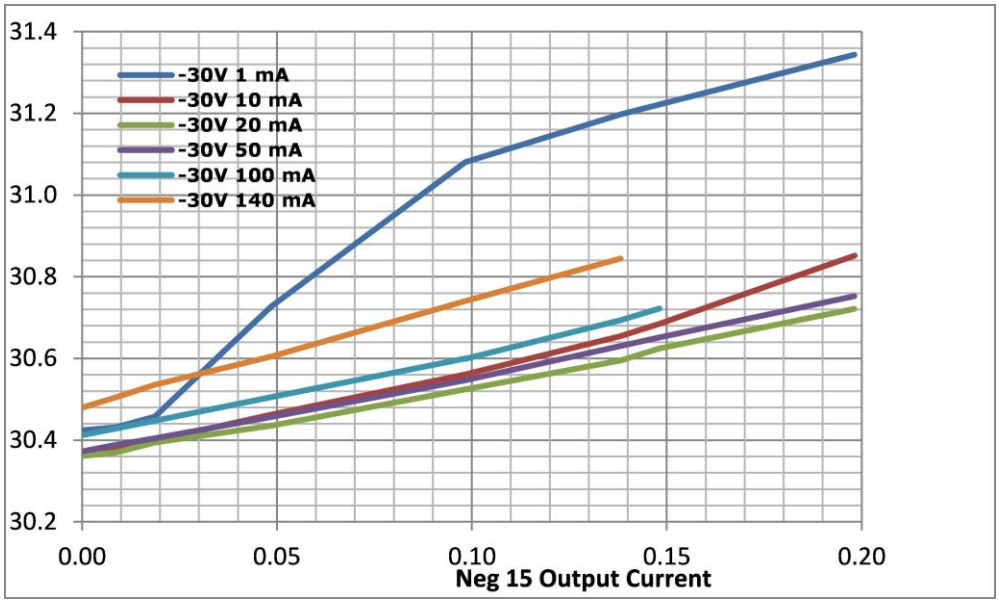

Fig. 27. The ADP2442 dual negative output, inverting buck boost measured -30 V Vout versus -15-V Iout, for different values of -30-V Iout.

There are several possible explanations for the weird curve shapes, but the -15-V output is directly and tightly regulated; dissecting imperfections in this nearly-perfect result is not the purpose of this article. Fig. 27 is really the more interesting of the two. The -30-V Iout magnitude climbs with increasing -15-V current in all the curves as expected. But as you move between the curves you are observing the effect on the -30-V Iout of varying load current from that output.

Increasing the load on the -30-V out actually increases the load on both outputs, due to the series dc connection. The increasing load on the -15-V out would tend to increase the voltage out of the -30-V out as the feedback loop compensates for increased I x R voltage drop in the inductor winding. However, increasing load on the -15-V out also increases the load and the voltage drop on the -30-V winding, which would tend to decrease the -30-V output voltage. We have opposing trends producing a non-obvious outcome. It turns out

that you get the minimum (magnitude) -30-V output voltage when you have a -30-V load current that is towards the light load end of the range.

Conclusion

This article has presented some useful tricks for improving the performance of several types of multiple-output voltage converters. It has also presented some likely unfamiliar or novel topologies that can take advantage of these tricks.

Although most of the designs produce two outputs, in fact all of the topologies shown can be extended to produce three or more outputs in cases where those are needed.

The author hopes that readers are intrigued by some of the ideas presented, so as to inspire creative new designs.

Appendix

This section provides bills of materials (BOMs) for the converter circuits presented in this article.

For all BOMs, resistors are 1% 0603 types except as noted.

Table 1. BOMS for isolated ac-input flyback converters.

Ref. Design	+5 V ±12 V	±12 V
	Fig. 1	Fig. 6
BR1	KBP208	KBP208
C2	Panasonic FR 150 µF 25V	Panasonic FR 150 µF 25V
C3	1 µF 16V 0805	1 µF 16 V 0805
C4	Pana FM 1200 16 V	DNP
C5	Pana FM 2200 6.3 V	Pana FM 1200 16 V
C6	100 nF 50 V X7R 0603	100 nF 50 V X7R 0603
C7	GRM31CR61A106KA01	C3216X5R1C475K
C8	100 nF 50 V X7R 0603	100 nF 50 V X7R 0603
C9	Pana FR 25 V	Pana FR 25 V
C11	Pana FM 680 16 V	DNP
C12	Pana FM 1200 6V3	Pana FM 680 16 V
C13	330 pF 100 V NP0 0603	DNP
C14	47 nF 1 kV 1210	47 nF 1 kV 1210 X7R
C15	470 pF 100 V NP0 0603	82 pF 100 V NP0 0603
C17	DNP	22 µF 25 V 1210 X5R
C19	C1608X7R1C105K TDK	C1608X7R1C105K TDK

C21	100 nF 50 V X7R 0603	100 nF 50 V X7R 0603
C23	1 nF 50 V NP0 0603	1 nF 50 V NP0 0603
C25	100 pF 50 V NP0 0603	100 pF 50 V NP0 0603
C27	Pana FM 680 16 V	Pana FM 680 16 V
C28	TDK C3216X5R1C475K	TDK C3216X5R1C475K
C29	82 pF 100 V NP0 0603	82 pF 100 V NP0 0603
C30	3.3 nF 50 V X7R 0603	3.3 nF 50 V X7R 0603
C33	Pana FM 2200 6V3	Pana FM 1200 16 V
C34	10 nF 50 V X7R 0603	10 nF 50 V X7R 0603
C35	DNP	100 nF 50 V X7R 0603
C80	C1608X7R1C105K	C1608X7R1C105K
C82	C3216X5R1C475K	DNP
C85	C1608X7R1C105K	C1608X7R1C105K
C87	Alum Elect 150 µF 400 V 105 deg snap-in	Alum Elect 150 µF 400 V 105 deg snap-in
C89	C1608X7R1C105K	C1608X7R1C105K
C93	100 nF 50 V X7R 0603	100 nF 50 V X7R 0603
C94	3.3 nF 50 V X7R 0603	22 nF 50 V X7R 0603
D1	MBRS360T3 ON Semi	DNP
D2	MBRS1100 ON Semi	SS2PH10 Vishay
D3	BAW56	BAW56
D6	PDS1040L Diodes Inc.	SS5P10 Vishay
D82	ES1J Fairchild	ES1J Fairchild
F1	2 A 250 Vac Time Delay	2A 250 Vac Time Delay
L5	ME3220 1 µH Coilcraft	500 nH; 4T AWG 20 on Micrometals T30-52
L6	ME3220 1 µH Coilcraft	DNP
Q3	MMBT3904	MMBT3904
Q82	SPD03N60C3 Infineon	SPD03N60C3 Infineon
R12	2.0 kΩ	2.0 kΩ
R13	12.7 kΩ	7.5 kΩ
R14	20 kΩ	20 kΩ

R15	DNP	27.4 kΩ
R16	100 Ω	100 Ω
R18	8.2 Ω 1206 5%	DNP
R19	16.9 Ω 1206	33 Ω 5% 1206
R20	8.2 Ω 1206	8.2 Ω 1206
R21	10 kΩ	10 kΩ
R25	1 kΩ	1 kΩ
R27	47.5 kΩ	DNP
R29	3.48 kΩ	3.48 kΩ
R30	10 kΩ	10 kΩ
R31	15 kΩ	15 kΩ
R32	33 Ω 5% 1206	33 Ω 5% 1206
R36	200 Ω	200 Ω
R37	20 kΩ	20 kΩ
R39	4.75E+03 Ω	4.75E+03 Ω
R65	8.2 Ω 1206	8.20 Ω 1206
R84	20 kΩ 500 mW. 2 x 20 kΩ 1206's in parallel, in series with two more. (4 total).	20 kΩ 500 mW. 2 x20 kΩ 1206's in parallel, in series with two more. (4 total).
R1A	0.68 Ω 1206	0.68 Ω 1206
R1B	DNP	DNP
R33	75 Ω 500 mW. 2 x 75 Ω 1206's in parallel, in series with two more. (4 total).	75 Ω 500 mW. 2 x 75 Ω 1206's in parallel, in series with two more. (4 total).
R5	132.6 kΩ 0.75 W (6 x 22.1 kΩ 1206 in series)	132.6K 0.75W (6 x 22.1 kΩ 1206 in series)
T1	Transformer wound on Ferroxcube PQ3230 3F3 46T Primary, 3T 5-V output, 4T +12-V output, 7T -12-V output, 7T Control	Transformer wound on Ferroxcube PQ3230 3F3 36T Primary, 5T 12-V output, 5T control
Th1	Inrush limiter 16 Ω 1.2 A	Inrush limiter 16 Ω 1.2 A
U1	UC3844A or UC3844B	UC3844A or UC3844B
U2	ADuM3190 Analog Devices	ADuM3190 Analog Devices

Table 2. BOM for ADP1614 SEPIC/Cuk pictured in Fig. 8.

Ref	Rating	Size/Type/PN	Manufacturer
C2	2.2 nF 25 V, 10%	0603, X7R	Generic
C3	1.0 µF 10 V, 20%	0603, X5R	Generic
C4	1.0 nF 25 V, 10%	0603, X7R or NP0	Generic
C5	10 µF 10 V, 10%	GRM31CR61A106K	Murata
C6	2.2 µF 25 V, 10%	GRM21BR61E225KA12L	Murata
C7	10 µF 16 V, 20%	C3216X5R1C106M	TDK
C8	10 µF 16 V, 20%	C3216X5R1C106M	TDK
C9	10 µF 16 V, 20%	C3216X5R1C106M	TDK
C10	68 µF 16 V	EEUFC1C680	Panasonic
C11	2.2 µF 25 V, 10%	GRM21BR61E225KA12L	Murata
C12	15 pF 10 V, 10%	0603, NP0	Generic
C13	10 µF 16 V, 20%	C3216X5R1C106M	TDK
C16	100 nF 10 V, 10%	0603, X7R	Generic
D1	Schottky 1 A 30 V	STPS1L30U	STMicro
D2	Schottky 1A 30V	STPS1L30U	STMicro
L1	Inductor Coupled 22 µH	LPD6235-223	Coilcraft
L2	Inductor Coupled 22 µH	LPD6235-223	Coilcraft
L3	Inductor 1 µH	ME3220-102	Coilcraft
R3	20 kΩ 5%	0603	Generic
R4	110 kΩ 1%	0603	Generic
R5	49.9 kΩ 1%	0603	Generic
R9	4.99 kΩ 1%	0603	Generic
R10	26.1 kΩ 1%	0603	Generic
U1	ADP1614ACPZ-1.3	Boost Regulator IC 1.3 MHz	Analog Devices

Table 3. BOMs for the two dual-output ADP2442 converters.

	±15-V out	-15-V and -30-V out
	Fig. 21	Fig. 25
C1	TDK C1608X5R1C105M	TDK C1608X5R1C105M
C3	TDK C2012X5R1C475M	TDK C2012X5R1C475M
C4	TDK C3216X7R1E105K	TDK C3216X7R1E105K
C5	DNP	Murata GRM32ER71H475KA88
C7	Murata GRM32DR61E106K	Murata GRM32DR61E106K
C8	TDK C3216X7R1H105K	TDK C3216X7R1H105K
C9	Suncon 35CE4R7GA	Suncon 35CE4R7GA
C10	100 nF 50 V X7R 0603	100 nF 50 V X7R 0603
C11	Suncon 16CE22KX	Suncon 16CE22KX
C12	TDK C3216X7R1E475M	TDK C3216X7R1E475M
C15	Murata GRM32ER71H475KA88	Murata GRM32ER71H475KA88
C16	DNP	DNP
C22	2.20E-09 F	2.20E-09 F
D3	Vishay SS1P4	Vishay SS1P4
L3	Coilcraft LPD6235-473	Coilcraft LPD6235-473
Q1	MMBT3906	MMBT3906
R4	3.01 kΩ	3.01 kΩ
R5	26.1 kΩ	26.1 kΩ
R6	10 kΩ	10 kΩ
R7	200 kΩ	200 kΩ
R8	47.5 kΩ	DNP
R9	4.99 kΩ	4.99 kΩ
R10	DNP	4.32 kΩ
R12	26.1 kΩ	DNP
R13	4.99 kΩ	4.99 kΩ
R21	20 kΩ	20 kΩ
R22	DNP	143 kΩ

U1	ADP2442ACPZ ADI	ADP2442ACPZ ADI

Acknowledgements

The author wishes to thanks Dr. Richard Redl for his valuable consultation on the content of this article. He also extends thanks to Analog Devices for its support of his efforts. Finally, Bob thanks his wife, Ding Zhang, for her patience and encouragement.

About The Author

Bob Zwicker received a BSEE in 1974 from North Carolina State University and began designing switching power supplies in 1980. He has one patented invention for a method of secondary-side control of synchronous rectifiers. Bob became an applications engineer in 2002 and began doing semiconductor power applications with Analog Devices in 2005. He lives and works out of his home in Olympia, Wash.

For further reading on buck-boost converter design, see the How2Power Design Guide, select the Advanced Search option, go to Search by Design Guide Category, and select "Buck-boost" in the Topology category.