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Streamlining Synchronous Buck-Boost Converter Design

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Conspicuous in various power converter specifications of late is a need to convert a wide-ranging input voltage to a regulated output voltage.[1] That task becomes more challenging, however, if the nonregulated input voltage is expected to vary continuously above, equal to, and below the regulated output voltage setpoint, calling for buck-boost conversion. Buck-boost conversion is essential across numerous applications including battery charging, solid-state lighting, industrial computing, and automotive.[2]

This article offers a brief review of many factors associated with four-switch buck-boost converter designs. It specifically addresses component selection and power loss calculations, and pulls from a quick-start calculator tool[3] to coordinate and accelerate converter design flow.

Synchronous Buck-Boost Converter Operation

As an efficient method to provide both stepup and stepdown conversion, a properly-designed buck-boost circuit is as indispensable as it is convenient. Let's review the four-switch (non-inverting) synchronous buck-boost topology shown in Fig. 1.

The main attraction of this buck-boost power stage is that buck, boost, and buck-boost conversion modes are engaged as needed to achieve high efficiency across broad ranges of input voltage and load current. It also provides a positive output voltage—in contrast to its cousin, the single-switch (inverting) buck-boost—as well as lower power loss and higher power density relative to SEPIC, flyback, and cascaded boost-buck topologies.

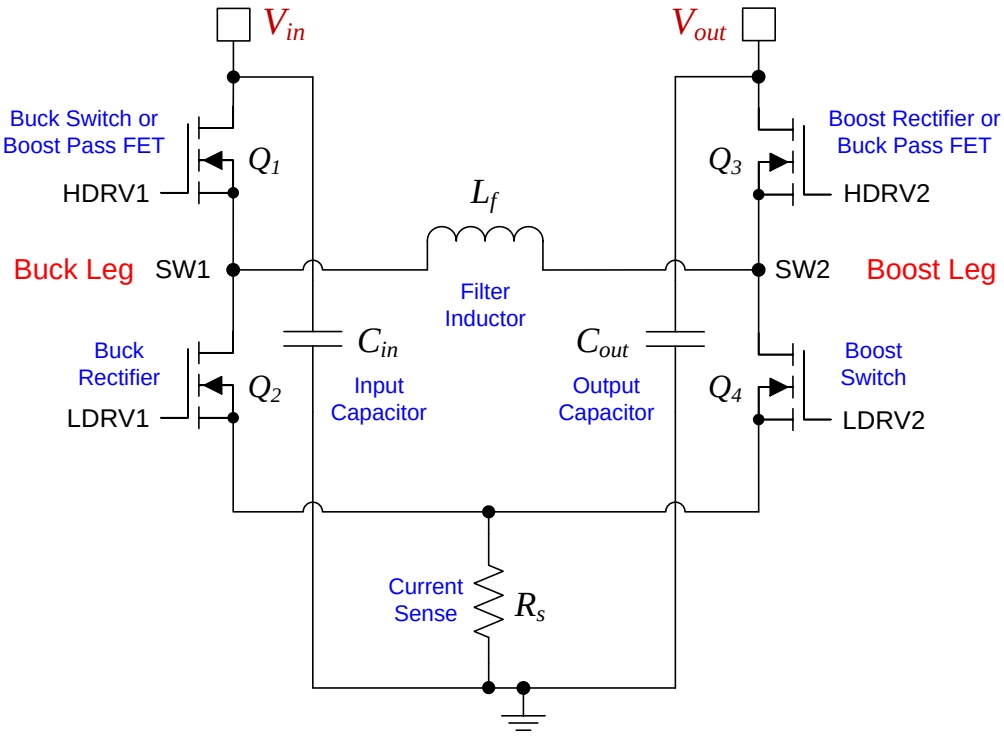

Fig. 1. Four-switch synchronous buck-boost converter power stage.

Four power MOSFETs are arranged in Fig. 1 as buck and boost legs in an H-bridge configuration, with switch nodes SW1 and SW2 connected by inductor L_F. Synchronous buck or boost operation occurs when the input voltage lies above or below the output voltage, respectively, and the high-side MOSFET of the opposite, non-switching leg conducts as a pass device. More important, when the input voltage approaches the output voltage the switching buck or boost leg reaches an anticipated duty cycle limit, triggering a transition to buck-boost operating mode. The mode of operation should change smoothly and autonomously without the need to change the control configuration. How this is accomplished, and what the interdependent relationship between power stage and control scheme may be, is quite important.

For example, one particular buck-boost controller, the LM5175[4], employs a unique scheme in buck-boost mode whereby both buck and boost legs switch at reduced frequency in quasi-interleaved manner, providing substantive advantages for efficiency and power loss. Peak current-mode boost and valley current-mode buck control techniques enable smooth mode transitions, requiring just one low-side configured shunt resistor for current sensing. A slope compensation implementation based on the difference of V_{IN} and V_{OUT} lends to deadbeat response and marks a good method to increase power supply rejection (PSR) and reject line transients.

Design Flow For Current-Mode Buck-Boost Converter

Illustrated in Fig. 2 is a complete schematic diagram of a four-switch synchronous buck-boost converter. The schematic includes components for power stage, gate-driver bootstrap, current-sense network, spread-spectrum frequency modulation (SSFM) for lower electromagnetic interference (EMI),[5] programmable undervoltage lockout (UVLO), output feedback, and loop compensation.

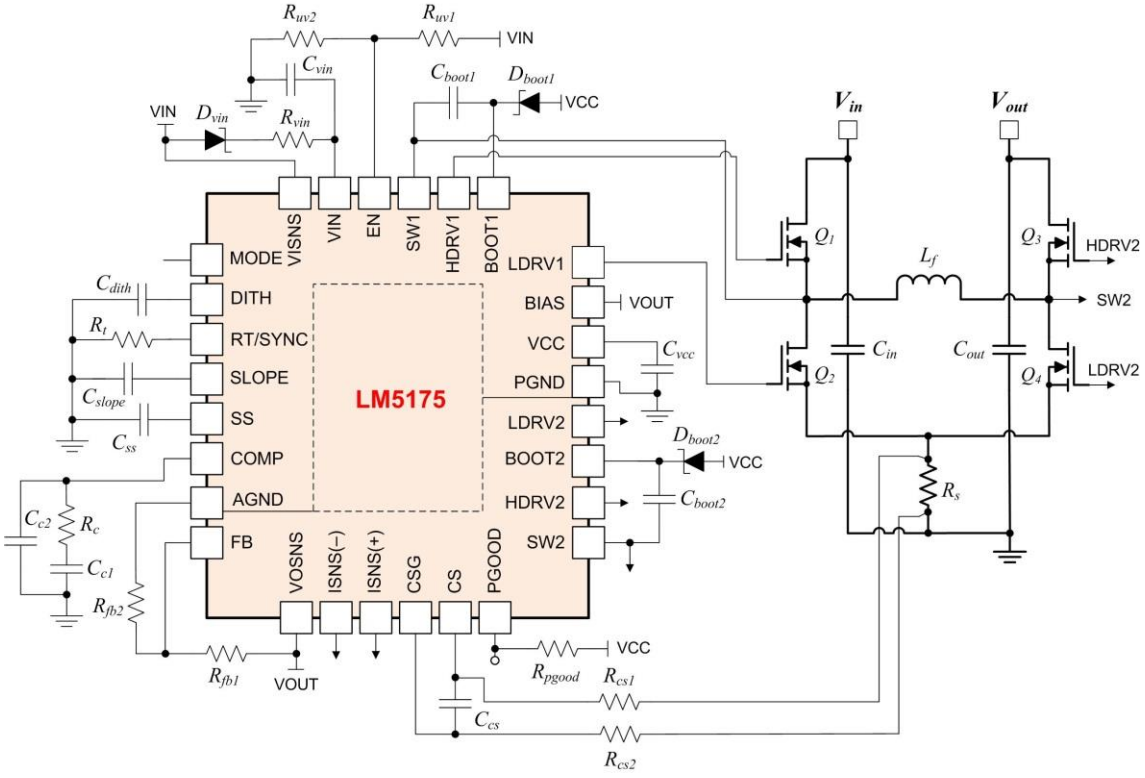

Fig. 2. Circuit schematic of four-switch buck-boost converter with current-mode controller.

A quick-start tool resource[3] provides a framework for analysis and design of the four-switch buck-boost converter. Progression is from converter specification to component selection to performance review (efficiency, component dissipations, and Bode plot), followed by design iteration if needed. Using the LM5175 synchronous buck-boost controller as a starting point, let's review the step-by-step design flow for a 400-kHz converter that delivers a 12-V output rated at 6 A from a 6-V to 42-V input source.

Step 1: Operating Specifications

The screen capture provided in Fig. 3 illustrates step 1 for entry of the user's specifications for input voltage range, output voltage, load current, and switching frequency.

Step 2: Filter Inductor

The inductance depends on the input voltage range and the target peak-to-peak inductor ripple current ratios. Equation 1 sets target ripple current ratios in deep boost and deep buck operating points at 30% and 80%, respectively.

$$L_f = \text{avg}\frac{\frac{V_{in(\min)}^{\ 2}}{V_{out}}\left(1-\frac{V_{in(\min)}}{V_{out}}\right)}{0.3I_{out}f_{sw}}, \frac{V_{out}\left(1-\frac{V_{out}}{V_{in(\max)}}\right)}{0.8I_{out}f_{sw}}. \quad (1)$$

There are three main parameters that attest to inductor performance—resistance (DCR), saturation current (I_{SAT}), and core losses. Inductors with powdered-iron core material have gained prominence at switching frequencies up to 400 kHz, becoming a more mainstream solution in many applications. A noteworthy and desirable feature is that inductance gradually falls off as current increases. Meanwhile, ferrite-cored inductors have comparatively lower core losses, though they come with the caveat to safeguard against a sharp drop in inductance at the onset of saturation.

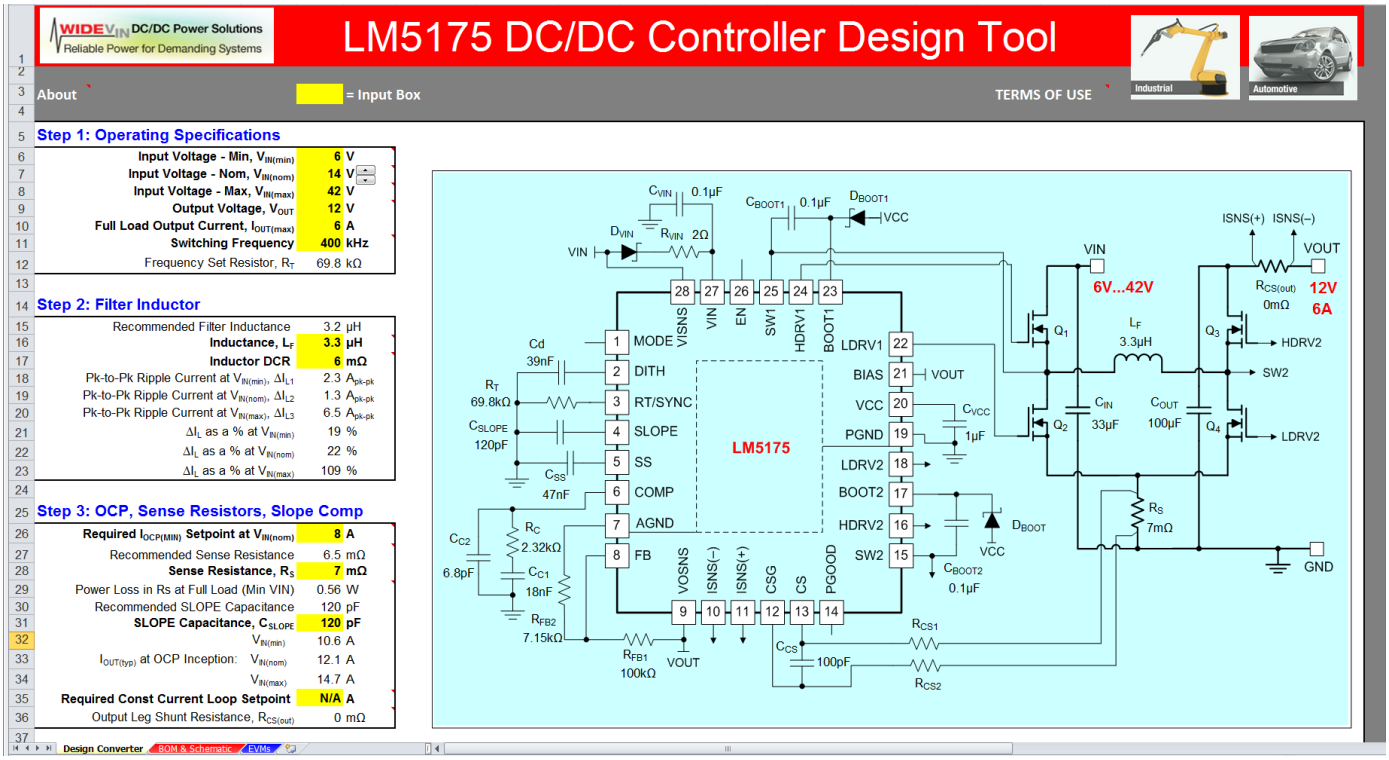

Fig. 3. Steps 1 through 3 refer to operating specifications, filter inductor, and current sense, respectively. The schematic is auto-populated based on entered and calculated component values.

Step 3: Shunt Resistance

The shunt resistance is set based on the relevant thresholds for current limit inception. For example, equation 2 pertains to the LM5175 and specifies an 80-mV valley threshold in buck and 160-mV peak threshold in boost. The shunt power dissipation peaks at lowest input voltage when boost duty cycle is at its maximum. A wide aspect ratio shunt resistor, 1225 footprint for instance, benefits PCB layout placement[5] adjacent to both low-side MOSFETs' source connections.

$$I_{\text{out}(OCP)} = \begin{cases} \left(\dfrac{160\text{mV}}{R_s} - \dfrac{\Delta i_L}{2}\right)\left(1 - D_{boost}\right), \text{boost} \\ \left(\dfrac{80\text{mV}}{R_s} - \dfrac{\Delta i_L}{2}\right)\left(1 - D_{boost}\right), \text{buck-boost} \\ \dfrac{80\text{mV}}{R_s} + \dfrac{\Delta i_L}{2}, \text{buck} \end{cases} \quad (2)$$

Next, slope compensation takes the sensed signal and adds a slope component equal to the inductor upslope in buck mode or inductor downslope in boost mode. Slope capacitance[4] calculates from equation 3 as

$$C_{slope} = \frac{g_{m(slope)} L_f}{R_s A_{CS}} . \quad (3)$$

Steps 4 And 5: Input And Output Filter Capacitors

Embedded in Fig. 4, steps 4 and 5 refer to input and output capacitances set by buck and boost operating modes, respectively. High-density designs increasingly avail of an aggregate of several X5R- or X7R-dielectric ceramic components, sometimes accompanied by a small-size electrolytic capacitor for bulk energy storage. Equation 4 sets baseline capacitance estimates using specifications for peak-to-peak ripple voltages, assuming no equivalent series resistance (ESR) ripple component.

$$C_{in} = \frac{I_{out} D_{buck} \left(1 - D_{buck}\right)}{f_{sw} V_{Cin(\text{pk-pk})}}$$
$$C_{out} = \frac{I_{out} D_{boost(\max)}}{f_{sw} V_{Cout(\text{pk-pk})}} \quad (4)$$

Then with capacitances chosen, the respective peak-to-peak ripple voltages are back-calculated, knowing the ESRs, as

$$V_{Cin(\text{pk-pk})} = I_{out}\left(ESR_{Cin} + \frac{D_{buck}\left(1 - D_{buck}\right)}{f_{sw} C_{in}}\right)$$
$$V_{Cout(\text{pk-pk})} = I_{out}\left(\frac{ESR_{Cout}}{1 - D_{boost(\max)}} + \frac{D_{boost(\max)}}{f_{sw} C_{out}}\right). \quad (5)$$

Input capacitor RMS current (and ripple voltage) is highest at 50% duty cycle in buck mode. On the other hand, the highest output capacitor RMS current occurs at maximum duty cycle in boost mode. Expressions for RMS currents are

$$I_{Cin(\mathrm{RMS})} = I_{out}\sqrt{D_{buck}\left(1-D_{buck}\right)} \le \frac{I_{out}}{2}$$

$$I_{Cout(\mathrm{RMS})} = I_{out}\sqrt{\frac{D_{boost}}{1-D_{boost}}} = I_{out}\sqrt{\frac{V_{out}}{V_{in(\min)}}-1}. \qquad (6)$$

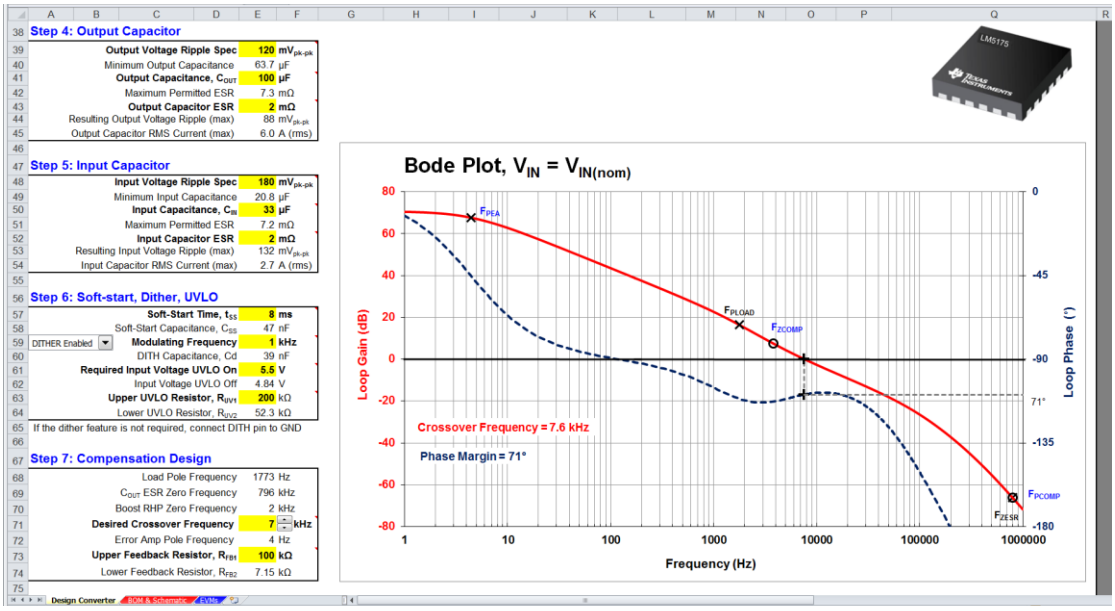

Fig. 4. Steps 4 through 7 refer to filter capacitor selection, compensator design, and Bode plot analysis.

Step 6: Soft-Start, Dither, UVLO

Based on a startup time specification, the required soft-start capacitance is

$$C_{ss} = \frac{I_{ss}T_{ss}}{V_{ref}}. \qquad (7)$$

The next option is to choose the dither capacitance to set the spread-spectrum modulating frequency[5] using equation 8, where G_d is a conductance coefficient related to the controller.

$$C_{dith} = \frac{G_d}{f_{mod}} \qquad (8)$$

Undervoltage lockout resistors set the rising and falling input-voltage thresholds for converter startup and shutdown, respectively. Choose the upper UVLO resistance to set the hysteresis. Then, if $V_{UV(ON)}$ is the UVLO comparator rising threshold, the corresponding lower UVLO resistance falls out as[4]

$$R_{uv2} = \frac{V_{uv(on)}}{I_{uv1} + \left(V_{in\_uv(on)} - V_{uv(on)}\right) / R_{uv1}} . \quad (9)$$

Step 7: Loop Compensation

The small-signal control loop performance is measured by two fundamental Bode plot metrics: crossover frequency and phase margin. The compensator zero frequency, determined by R_C and C_{C1}, provides phase boost prior to crossover. A pole established with C_{C2} located near the output capacitor ESR zero (or half switching frequency, whichever is lower) provides noise attenuation and minimizes output ripple propagation to the COMP node. The compensation components are chosen using

$$R_c = \frac{2\pi f_{cross} C_{out} A_{CS} R_s}{g_{mEA} A_{fb}}$$

$$C_{c1} = \frac{1}{\pi R_c f_{cross}} \quad . \quad (10)$$

$$C_{c2} = \frac{1}{2\pi R_c f_{zESR}}$$

To tweak for increased bandwidth, simply increase the compensation resistance R_C and adjust C_{C1} for phase margin as needed. The right half plane zero (RHPZ) is, of course, relevant in boost, and the constraint that crossover is below 50% of the RHPZ frequency for acceptable phase margin is described by

$$f_{cross} \le \frac{f_{RHPZ(\text{boost})}}{2} = \frac{R_{load}}{4\pi L_f} \left(\frac{V_{in(\min)}}{V_{out}} \right)^2 . \quad (11)$$

It is important to point out that the crossover frequency trends lower in boost mode owing to reduced current-mode modulator gain (proportional to $1–D_{BOOST}$). Indeed, a quick Bode plot review at minimum input voltage clears up whether the compensator zero is contributing sufficient phase near crossover.

Step 8: Efficiency Prediction

Step 8, shown in Fig. 5, provides plots of efficiency and component power dissipations versus line and load. Characterization of all four power MOSFETs centers around on-state resistance, gate charges, gate resistance, transconductance, gate-source threshold voltage, and body diode forward drop and reverse-recovery charge parameters. Sure, the inductor current runs higher in boost than in buck, but the boost-leg MOSFETs rated for V_{OUT} generally have lower $R_{DS(ON)}$ than the buck-leg devices rated for maximum V_{IN}.

Equations 12 and 13 calculate conduction, switching, and gate-drive losses in buck and boost modes, respectively. Corresponding expressions for buck-boost mode are weighted combinations of equations 12 and 13 according to the operating point within the buck-boost window and frequency divided by two.

$$P_{cond(buck)} = I_{out}^2 \left(D_{buck} R_{DS(on)Q1} + (1 - D_{buck}) R_{DS(on)Q2} + R_{DS(on)Q3} \right)$$
$$P_{sw(buck)} = V_{in} \left[I_{out} \left(t_{on\,Q1} + t_{off\,Q1} \right) + Q_{rr\,Q2} \right] f_{sw} \qquad (12)$$
$$P_{gate(buck)} = V_{CC} \left(Q_{g\,Q1} + Q_{g\,Q2} \right) f_{sw}$$

$$P_{cond(boost)} = I_{in}^2 \left(D_{boost} R_{DS(on)Q4} + (1 - D_{boost}) R_{DS(on)Q3} + R_{DS(on)Q1} \right)$$
$$P_{sw(boost)} = V_{out} \left[I_{in} \left(t_{on\,Q4} + t_{off\,Q4} \right) + Q_{rr\,Q3} \right] f_{sw} \qquad (13)$$
$$P_{gate(boost)} = V_{CC} \left(Q_{g\,Q3} + Q_{g\,Q4} \right) f_{sw}$$

As expected, inductor copper and core losses, switch deadtime conduction loss, shunt loss, and bias regulator loss also factor into efficiency calculations. Considering losses in totality, a four-switch buck-boost converter with 12-V regulated output quite readily achieves efficiencies in excess of 96% across broad ranges of output current and input voltage.

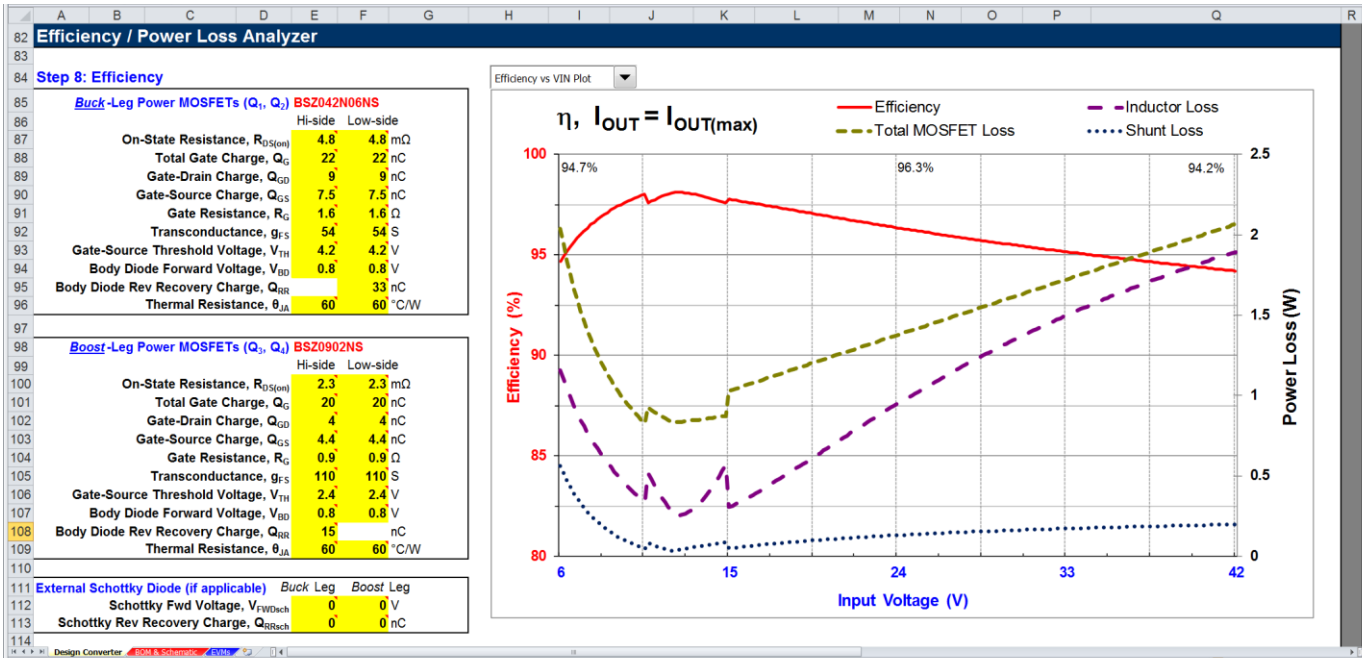

Fig. 5. Step 8 refers to MOSFET specification, efficiency plots, and power loss analysis.

Summary

Buck-boost converters for industrial and automotive applications have unique power solution requirements. Testament to its ease-of-use, high efficiency, compact size, and low overall bill-of-materials cost, a four-switch synchronous buck-boost converter offers a collective of advantages to meet the main required functions. Given the component interdependencies and tradeoffs involved, a quick-start calculator is certainly a convenient tool for expedited and streamlined converter design.

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About The Author

Timothy Hegarty is a systems engineer with the Texas Instruments Silicon Valley Analog group. He received his bachelor's and master's degrees in electrical engineering from University College Cork, Ireland. His area of interest is integrated PWM switching regulators and controllers for wide-input-voltage-range industrial and automotive applications. He is a member of the IEEE Power Electronics Society. You can reach Tim at ti_timhegarty@list.ti.com.

For further reading on buck-boost converter design, see the How2Power Design Guide, select the Advanced Search option, go to Search by Design Guide Category and select "Buck-Boost" in the Topology category.