ISSUE: April 2015

Don't Throw That Switch Yet! First Steps In A Large Inverter Design

by Paul Schimel, International Rectifier, El Segundo, Calif.

We've all been through it. Long design cycle, tons of work and late hours, deadlines pulled in, power levels pushed out, etc. Then comes the one moment that either makes it rewarding or just a heck of a mess—the moment you throw the big switch. With a couple hundred watt SMPS, the moment isn't that unnerving. At a couple kilowatts, it gets pretty tense, and at some point above that, shields are in place and personal protective equipment (PPE) is worn.

There can only be one question on your mind at this time: did I iron out all of the details? Whether you are a simulation fanatic that views hardware as a scary departure that gets in the way of the mathematics, a hardware die hard that lives to see the 5000-hp machine cog and test the welds on the motor mounts and reactionary torque arm—or anywhere in between—the devil is always in the details. The final thought has to be precisely that.

Most anyone designing a large inverter or motor drive will tell wonderful tales of plasma events, gnarly twisted bussbars and fuses of much greater I^2*t value than the bondwires of the devices. I have had some of my own experiences with such fireworks over the last couple of decades. But beyond the war stories there are a few good tips that I can share.

In our last segment, we discussed selecting the right IGBT module for the application.[1] This included understanding the machine and its operating conditions, the IGBT module construction and the various IGBT ratings. With that as the foundation, the next logical step is to begin the inverter design. This work will take a look at the first three topics along that path.

The first of these topics is the dc link, which requires that the capacitors, bussbars and interactions be carefully addressed. From this point the conduction and switching losses for the IGBT and FRED die are calculated with datasheet parametric values. Finally, this discussion segues into thermal design.

DC Bus Design And Capacitor Selection

The role of the dc bus is straightforward. It has to store enough energy to ride through mains voltage sags, safely accommodate swells, and source the currents required by the IGBT modules.

Safe current density for a system like this is usually between 300 and 1000 CM/A where CM/A stands for circular mils per ampere. In this "old school" vernacular, a wire of 10-mil diameter has a diameter of 0.010 in. and a cross section of 100 CM, depending on airflow availability. If the structure is in still air, a larger cross section is a better idea. Ultimately the temperature rise specification of the drive and/or the insulation system on the dc bus will govern how big a cross section is needed.

There are many innovative solutions that offer good flexibility and minimal stray inductance beyond a traditional "two-bar" approach. A lot of these technologies will laminate thinner positive and negative conductors between thin insulators to offer much lower inductance and higher distributed capacitance, effectively building a "dc transmission line."

The value of the capacitor bank is usually dominated by the voltage sag requirements and holdup time specifications. If the capacitor bank has to run the inverter at full load for perhaps one half of a mains cycle, this gives rise to capacitors of substantial value.

Consider perhaps a 340-V dc link with a minimum allowable voltage of 300 V. If the full load dc current from the bus is 1000 A, and the required holdover time is ½ cycle on a global inverter, then the capacitor has to be at least (1000 A)*(10 ms/(340 V – 300 V)) or 250,000 µF as per $I = C*dv/dt$.

But the process isn't that simple. The question of ripple current arises. The capacitor bank has to be able to handle the ripple currents that would both charge and discharge the capacitor. The frequencies of this

interaction are the rectified mains frequency (180 Hz in the U.S.), the output fundamental frequency and the switching frequency. This is a hefty superposition problem best approached with a well-thought-out, detailed simulation.

There isn't much room for stray inductance in the dc bus. From the viewpoint of the IGBT, if there is stray inductance in the dc bus, the energy stored in that stray inductance is then $LI^2/2$. If the inverter's currents are large—perhaps several hundred or thousands of amperes—the energy stored in a few nanohenries of stray inductance has significant impact on the IGBT and FRED. Excessive dc bus inductance can cause substantial, damaging overvoltage events on the turn-off edge of an IGBT waveform.

For this reason, most IGBT modules are set up with dc bus connection terminals close to each other. Close enough to accommodate a very low dissipation factor, low-ESR, low-ESL polypropylene bus capacitor bolted directly to the terminals. This puts the best possible source as near the module as possible. These capacitors can source tremendous currents with minimal loss. Once the capacitor values and loss budgets are understood, a call to the senior engineers at your capacitor vendor should have you on the right track to satisfy your holdover, ripple current and minimal ESR loss requirements.

Conduction And Switching Loss Calculations

The inverter design, like most any other power electronics design effort, has to stay within the maximum junction temperature specifications of the IGBT. The IGBT will have a maximum junction temperature specification in the datasheet, and most applications derate that even further based on the project specifications as well as house rules and procedures.

To stay within this temperature specification you have to know the maximum ambient or boundary temperature, the maximum junction temperature, the thermal impedances and the losses in the device. Loss calculations are difficult for three-phase inverters. Most are left to Mathcad routines or programs that capture each vector state and the switching losses between them as RMS quantities.

Any loss calculation should be correlated with real, measured case temperatures in situ.

The calculation below is based on Graovac and Purshel's work (see reference 2.) It is much simpler than the sophisticated simulation programs. The basis of the calculation is to use the RMS output current (I_{out}), the device voltage drops and resistances (V_{ce}, r_{ce}, V_f, and r_d), the modulation index (m), the displacement power factor (PF) and the switching frequency (f_{sw}) to deliver approximate conduction and switching losses. The following example uses the IRG5K400HF06BP dual IGBT module.

The junction resistances can be calculated by equations 1 and 2.

r_{ce} = the approximate slope of the I_c vs V_{ce} curve at max temp near the typical V_{ce} value. (1)

For the IRG5K400HF06BP,

$$r_{ce} = \frac{(2.8\,V\ - 1.15V)}{(800\,A - 0A)} = 2.1\ \mathrm{m\Omega} \quad .$$

r_d = the approximate slope of the I_F vs V_F curve at max temp near the typical V_F value. (2)

For the IRG5K400HF06BP,

$$r_d = \frac{(1.8\,V\ - 1.00V)}{(800\,A - 0A)} = 1.0\ \mathrm{m\Omega} \quad .$$

The conduction and switching losses can be calculated by

$$P_{condloss_{IGBT}} = (V_{ce} * I_{out}) * \left(\frac{1}{2*\pi} + \frac{m*PF}{8}\right) + \left(r_{ce} * {I_{out}}^2\right) * \left(\frac{1}{8} + \frac{m*PF}{3*\pi}\right) \quad (3)$$

$$P_{condloss_{FRED}} = (V_f * I_{out}) * \left(\frac{1}{2*\pi} + \frac{m*PF}{8}\right) + \left(r_d * {I_{out}}^2\right) * \left(\frac{1}{8} + \frac{m*PF}{3*\pi}\right) \quad (4)$$

$$P_{swloss_{IGBT}} = f_{sw} * (E_{on} + E_{off}) \quad (5)$$

$$P_{swloss_{FRED}} = f_{sw} * (E_{rr}) \quad . \quad (6)$$

For an initial starting point, the datasheet values for E_{on}, E_{off}, E_{rr} and V_{cesat} at maximum temperature must be used in the loss calculations. The phase current of course is based on the worst-case load. As the design solidifies, iterate this calculation with measured values in situ. Use the measured V_{cesat} and V_f values, as well as the E_{off} and E_{on} values determined by in-situ double pulse testing.

There has been a lot of work done on scaling E_{off} and E_{on} between the test currents used in the datasheet and the phase currents seen in situ. However, the best approach is to simply measure E_{off}, E_{on}, E_{rr}, V_{cesat} and V_f in situ rather than the scaling approach. The scaling factor varies with device technology and is often misleading. There's no uncertainty in using the actual measured numbers.

Thermal Design

Once the maximum conduction and switching losses are known, the thermal design is started. The thermal design has a very simple goal. That is, to achieve sufficient thermal transfer through the heatsink to keep the IGBT devices below the maximum allowed junction temperature. But therein lies the problem. In a finished module, we can't measure the junction temperature. We can measure the case temperature and possibly the value of a thermistor located near the dice.

The datasheet gives $R_{\Theta jc}$ for the individual IGBTs and FRED dice in the module. The maximum ambient temperature seen by the equipment and related heatsink is known by this point and the company's in-house design rules that give maximum junction temperature guidelines are in play.

The switching and conduction losses can be calculated. All that remains is the means to get the heat away from the module and the interface between the module and the heatsink.

This is best brought together with an example. Let's say we are using the IRG5K400HF06BP dual module in an inverter switching at 4 kHz, delivering 200 A rms per phase with a machine PF of 0.8 and a modulation index of 85%.

Step 1. We calculate the following losses per IGBT and FRED given the 4-kHz switching frequency and the worst-case load current of 250 A rms per phase.

Per equation 3: IGBT conduction loss = 104.4 W per switch.

Per equation 4: FRED conduction loss = 66.5 W per switch.

Per equation 5: IGBT switching loss = 92 W per switch.

Per equation 6: FRED switching loss = 5.2 W per switch.

Step 2. From the datasheet we have $R_{\Theta JC}$.

- $R_{\Theta JC\_IGBT}$ = 0.077°C/W
- $R_{\Theta JC\_FRED}$ = 0.348°C/W

Step 3. The thermal constraints for the project are:

- T_{jmax} = 150°C
- $T_{ambient\_max}$ = 50°C.

Step 4. If we apply $R_{\Theta JC}$, from the max allowed junction temp (assuming included margin), we get:

IGBT temperature rise (junction to case) = 196.4 W * 0.077°C/W = 15.1°C;

FRED temperature rise (junction to case) = 71.7 W * 0.348°C/W = 25.0°C.

Given the T_{jmax} design constraint, this means that the case temperature must be held at 125°C maximum. This is padded slightly to a 120°C maximum case temperature.

Step 5. There are two IGBTs and two FREDs in this module package, therefore there is 536.2 W of heat to be removed. From this value, and the max case and ambient temperatures we can specify the thermal resistance of the heatsink in the final two steps.

Step 6. Given the above values, $R_{\Theta CS}$ combined with $R_{\Theta SA}$ has to be:

$R_{\Theta CA}$ = (120°C case temp - 50°C max ambient)/536.2 W = 0.131°C/W.

Step 7. A good assumption for thermal transfer compound is that it will yield 0.05°C/W per square inch if properly applied and compressed to 0.001-in. final thickness. The 61-mm package subtends about 9 square inches of area at the baseplate. The thermal resistance of the compound should then be 0.0055°C/W. For this example, we will assume some manufacturing deviation and use 0.01°C/W.

Step 8. To account for the thermal resistance of the compound, the heatsink for this one module needs to have an $R_{\Theta SA}$ of 0.12°C/W. A good heatsink with proper airflow can accomplish this. Heatsink and coldplate vendors have this information on their various extrusions and cold plates varying over air or coolant flow rates (see the figure.)

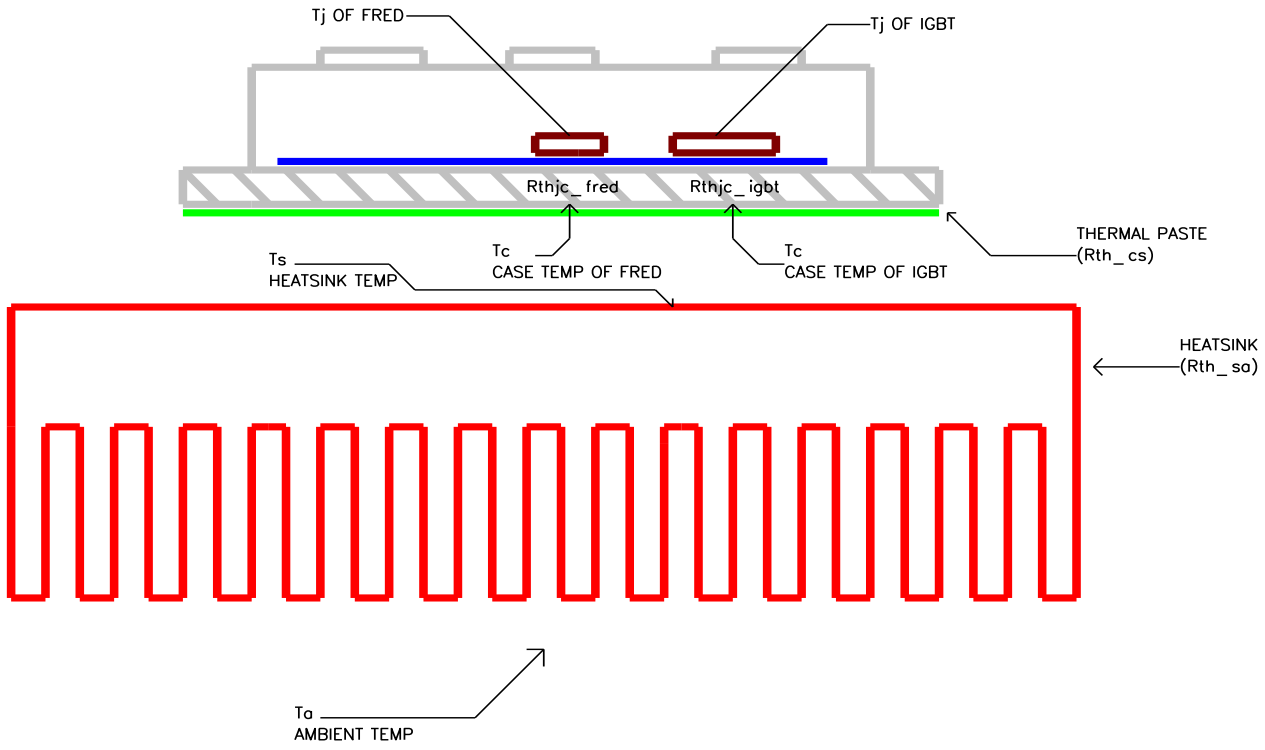

Figure. Thermal stackup. Note $R_{\Theta jc}$ is for individual die.

Conclusion

Thus far in the inverter design process, we have selected the module, designed the dc link and capacitors, calculated some preliminary switching losses and designed a first-pass heatsink. We aren't ready to throw the switch yet and turn the inverter on. There's still a good amount of work ahead. We will soon discuss a couple more design concepts like in-situ measurements, mechanical design, gate drive, snubber design and safety. Stay tuned for these topics and more in future articles.

References

1. "Mission IGBT: Understanding And Specifying IGBT Modules," by Paul Schimel, December 2014 issue of How2Power Today.

2. "IGBT Power Loss Calculation Using the Datasheet Parameters" by Dusan Graovac and Marco Purshel, January 2009, Infineon.com.

About The Author

Paul Schimel is a lifelong innovator with an untiring commitment to engineering excellence in both the practical and theoretical aspects of power electronics and related mixed signal, mixed mode and mixed domain design and control work. He is a licensed PE bringing two decades of formal experience to his customer base. His informal training started at age 6 when he began following in his dad's footsteps: the Western Electric Hawthorne Works legacy of design excellence. He is familiar with most DOD, MIL, UL, NFPA70, DOD and IEC standards and how they are tested and passed.

He attended the School of Electrical Engineering at the University of Illinois at Urbana Champaign, where he earned a BSEE degree while specializing in power electronics. After this, he spent eight years in successful design engineering roles in consumer equipment including power supply design for projection and direct view televisions and telecommunications equipment including ring generators, battery rectifiers/eliminators, dc-dc converters, and UPSs—both switch-mode and ferroresonant.

Schimel then moved on to applications engineering where he has spent the last 12 years on power management support and design work for Unitrode/TI, Fairchild, International Rectifier and International Rectifier HiRel / Infineon. He has assisted successful designs from milliwatts to megavolt-amps and from IC/Device design to prototype stages to finished end equipment. Applications ranging from industrial to automotive to full radiation hardened designs. He moonlights in broadcasting, antique test equipment restoration, metal working, woodworking, TIG welding, loudspeaker building, and amateur radio. He also holds a commercial radio telephone license, a refrigeration license, and PE license. Schimel holds several patents on magnetic structures for power electronics and novel circuitry. "When I find a design or problem to be impossible, I go see Paul, he figures it out" expounds one of his 20 year peers in the industry.

For further reading on IGBTs, see the How2Power Design Guide, select the Advanced Search option, go to Search by Design Guide Category and select "Power Transistors" in the Component category.