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Application-Specific FOM: Key To Choosing The Right MOSFET

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Size, efficiency and cost are the definitive characteristics of any power supply. In the computing segment, the efficiency requirements have been codified and are popularly known as 80 Plus standards. They encompass different levels of system efficiency from the simple 80 Plus up to Titanium 80 Plus, as shown in Table 1.

Table 1. 80 Plus efficiency and PFC certification standards.

	Efficiency											
	80 PLUS		80 PLUS BRONZE		80 PLUS SILVER		80 PLUS GOLD		80 PLUS PLATINUM		80 PLUS TITANIUM	
	V_{IN} = 115 V ac	V_{IN} = 230 V ac	V_{IN} = 115 V ac	V_{IN} = 230 V ac	V_{IN} = 115 V ac	V_{IN} = 230 V ac	V_{IN} = 115 V ac	V_{IN} = 230 V ac	V_{IN} = 115 V ac	V_{IN} = 230 V ac	V_{IN} = 115 V ac	V_{IN} = 230 V ac
10% load												90%
20% load	80%		82%	81%	85%	85%	87%	88%	90%	90%		94%
50% load	80%		85%	85%	88%	89%	90%	92%	92%	94%		96%
100% load	80%		82%	81%	85%	85%	87%	88%	89%	91%		91%
PFC	0.9 @100% load		0.9 @50% load		0.9 @50% load		0.9 @50% load		0.95 @50% load		0.95 @20% load	

Looking at the tight specifications for system efficiency, it is obvious that choosing the best components for the application will be a challenge even for experienced designers. Power semiconductors contribute the bulk of the losses and must be chosen carefully for the lowest loss for the given operating environment. The ultimate criterion is of course the actual performance of the system. But given the wide range of MOSFETs available today in different voltages and packages, it is not practical to experimentally evaluate all the devices in what would be considered a representative sample. Some designers simply choose the lowest R_{DSON} device from a given set, which invariably leads to a costly and suboptimal solution. Many others rely on the so-called figure of merit (FOM).

The traditional FOM has been the R_{DSON} x Q_G product, which promises a balance between conduction and switching losses.[Ref] Several variations have been proposed using other parameters like Q_{GD} or Q_{OSS} of the MOSFET instead of Q_G, or adding other terms to the equation.

Unfortunately, none of the conventional FOMs are designed to predict real-world performances that matter to designers. There are no terms to represent the operating conditions, such as switching frequency, gate drive, or even the output current or power. Further, total losses in any switching device are the sum of conduction and switching losses, each of which in turn is proportional to R_{DSON}, V_{FWD} of the diode, and switching charges such as Q_G, Q_{SW}, and Q_{OSS}.

However, the FOM definitions are always given in terms of products of these parameters. Simply put, almost all FOM definitions are rooted in device design but "blind" to the application. Instead of these generic formulas, the designers need to do a loss analysis at the system level and use it as the basis for device selection. The advantage is that both operating conditions as well as device parameters get to play a role in device selection.

Loss analysis for switching converters can be quite complicated, requiring a great deal of device parametric data, knowledge of circuit parameters, and complex mathematical equations. However, our purpose here is not to compute losses with high precision, but to do so in a manner that is accessible to most designers and which enables them to select the best device by comparing a small set of published device parameters. We illustrate the process for the common power factor correction (PFC) stage, mandatory for ac-dc converters where the input power level is 75 W or more. The principle of loss-derived FOM is of course applicable to any topology.

Loss Equations for A MOSFET in CCM Mode PFC

The standard implementation of active PFC is a boost converter following the input rectifier. Though newer topologies are gaining acceptance, the boost PFC is still the dominant solution and will be investigated further here. The basic boost PFC and its standard waveforms are shown in Fig. 1. Here we choose the continuous current mode (CCM) of operation. The analysis will cover power levels from 100 W, which is typical for ac-dc adaptors for notebook computers, up to 500 W, which is the typical rating for desktop silver box power supplies.

The losses for a power MOSFET in any application can be listed individually as:

- Conduction—from R_{DSON}
- Turn-on switching—V x I crossover
- Turn-off switching—V x I crossover
- Charging/discharging of output C_{OSS}
- Charging/discharging of input C_{ISS}
- Body diode—V_{FWD} and Q_{RR}.

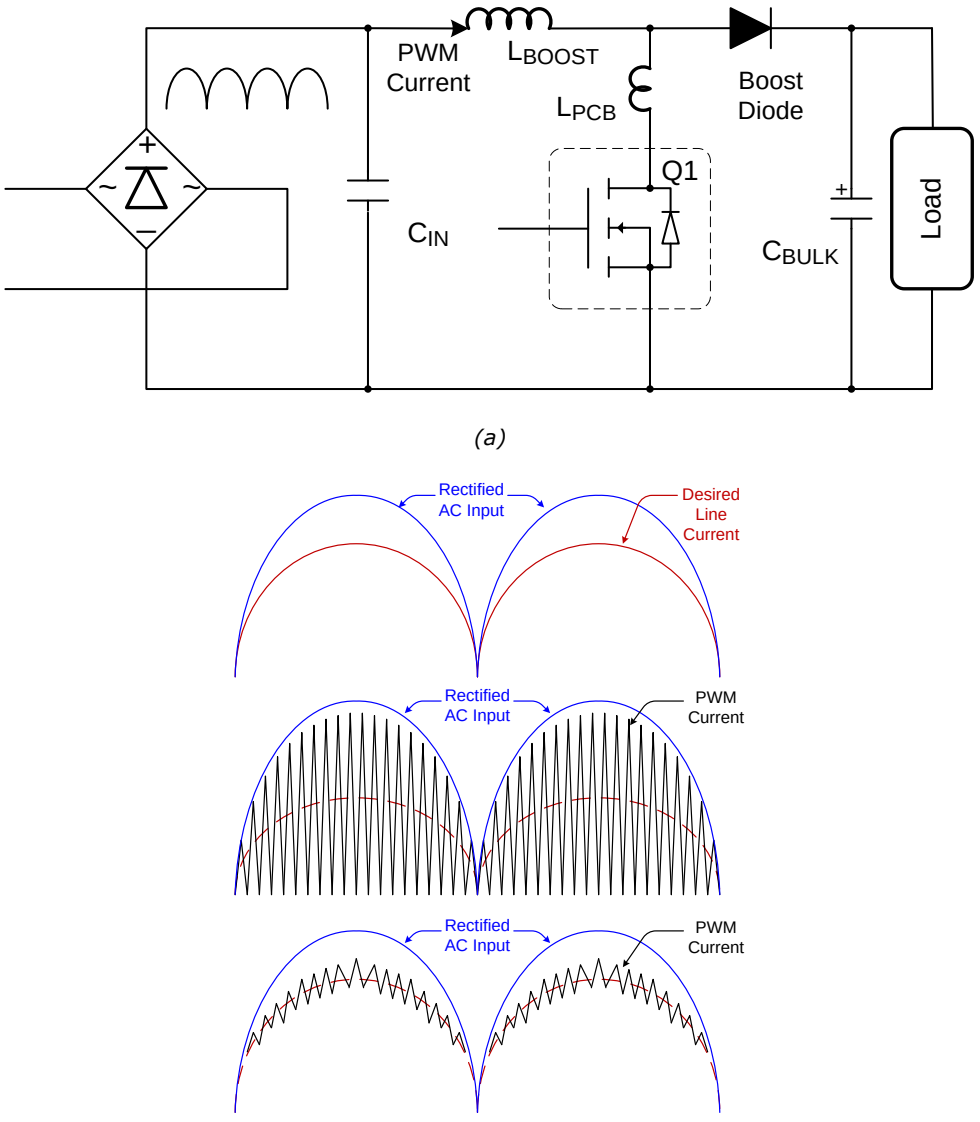

Fig. 1. Basic PFC boost circuit (a) and simplified PFC waveforms for critical and continuous modes (b).

Before calculating actual losses it is necessary to estimate the operating parameters of the application, such as peak and RMS currents, input and output voltages, etc. The conduction losses are dependent on the RMS value of the current that the MOSFET will see during one input ac cycle. Switching losses are determined by the average value of the inductor current I_{AC}.

I_{AC} is the simpler parameter, obtained by averaging the rectified line current in each ac cycle.

$$I_{AC} = \frac{2\sqrt{2}}{\pi} \times \frac{P_{IN}}{V_{IN}}$$

The RMS value of the MOSFET current is not so straightforward. It varies within each switching cycle and is best calculated numerically. Fig. 2 shows I_{AC} and I_{RMS} plotted as a function of V_{IN} for a 500-W PFC. At lower inputs the values are quite close. At 100-V ac we can write:

$$I_{RMS} = \frac{I_{AC}}{1.082} = \frac{1}{1.082} \times \frac{2\sqrt{2}}{\pi} \times \frac{P_{IN}}{V_{IN}} \cong \frac{1}{1.2} \times \frac{P_{IN}}{V_{IN}}$$

Knowing the RMS current, conduction losses can be calculated.

$$P_{COND} = {I_{RMS}}^2 \times R_{DSON} \times TCR = \left(\frac{P_{IN}}{1.2 \times V_{IN}}\right)^2 \times R_{DSON} \times TCR$$

TCR is the temperature coefficient of resistance for R_{DSON}. Typical values are 2.0 to 2.5 for 600 V and 650 V MOSFETs.

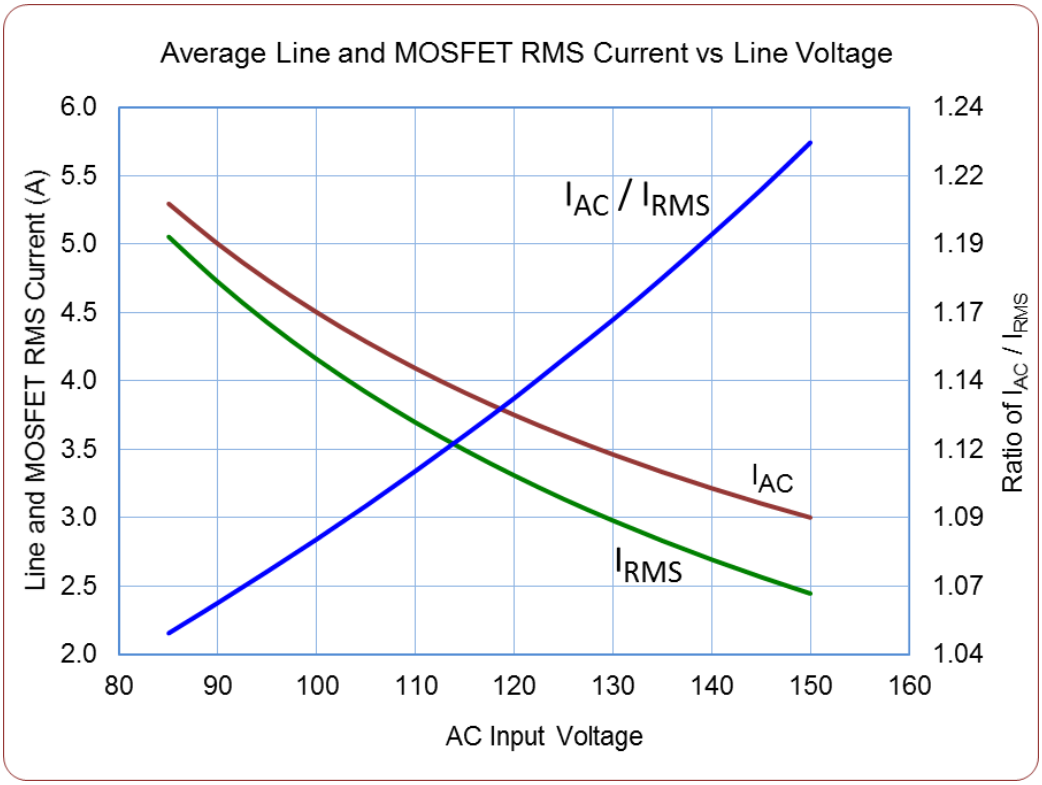

Fig. 2. I_{AC} and I_{RMS} for a 100-W PFC.

The standard gate-charge model for the turn-off sequence is shown in Fig. 3. When operating in CCM mode, the PFC MOSFET always turns on and off against the bulk voltage V_{DC}. Switching losses are a function of V_{DC}, I_{AC}, and switching times T_{SWON} and T_{SWOFF}. As explained in the reference, the projected rise time of the drain voltage, shown in blue, spans the entire Miller plateau represented by Q_{GD}. Q_{SW} is the effective switching charge, introduced as a combination of Q_{GS} and Q_{GD}. If the MOSFET were being driven with an effective constant current of I_{GON} and I_{GOFF},

$$T_{SWON} = \frac{Q_{SW}}{I_{GON}}$$

$$T_{SWOFF} = \frac{Q_{SW}}{I_{GOFF}}.$$

The total switching time T_{SW} can now be written in terms of an equivalent gate drive current I_{GEQ}:

$$T_{SW} = T_{SWON} + T_{SWOFF} = \frac{Q_{SW}}{I_{GEQ}}$$

where,

$$\frac{1}{I_{GEQ}} = \frac{1}{I_{GON}} + \frac{1}{I_{GOFF}}.$$

MOSFET datasheets typically offer Q_{GS} and Q_{GD} but not always Q_{SW}, the effective switching charge. For low voltage devices, Q_{SW} is usually approximated as:

$$Q_{SW(LV)} = \frac{Q_{GS}}{2} + Q_{GD}.$$

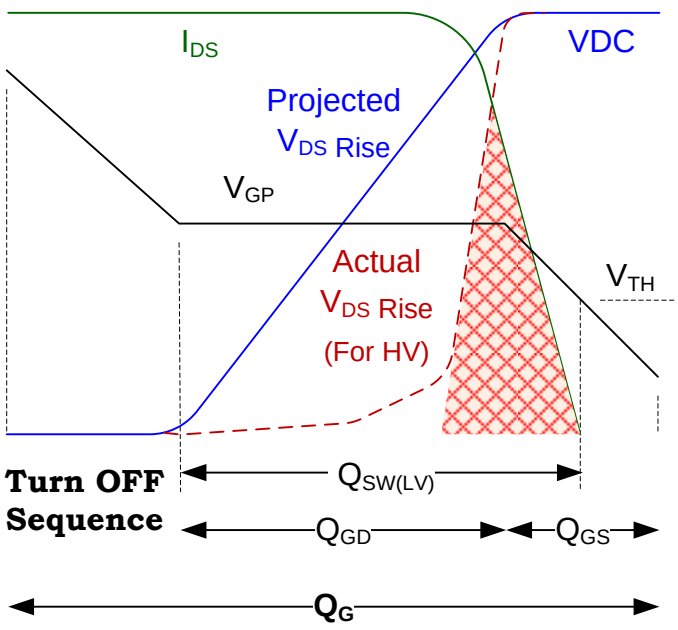

Fig. 3. Turn-off and Q_{SW} definition.

However, this approximation does not work for high-voltage MOSFETs, because of the wide variations in their capacitances. Typical capacitance variations for a high-voltage superjunction MOSFET are shown in Fig 4. Both C_{RSS} and C_{OSS} can vary by a factor of 100 within the first 100 V.

Returning to Fig. 3, while the projected rise for V_{DS} based on the conventional, low-voltage gate-charge model is shown in blue, the actual V_{DS} rise looks more like the dashed line in red. The corresponding switching loss, represented by the shaded area, is also much less than estimated by using the entire Miller plateau. To match the observed voltage rise and fall times, Q_{SW} may be written as:

$$Q_{SW} = 0.4 \times Q_{GS} + \frac{Q_{GD}}{4}$$

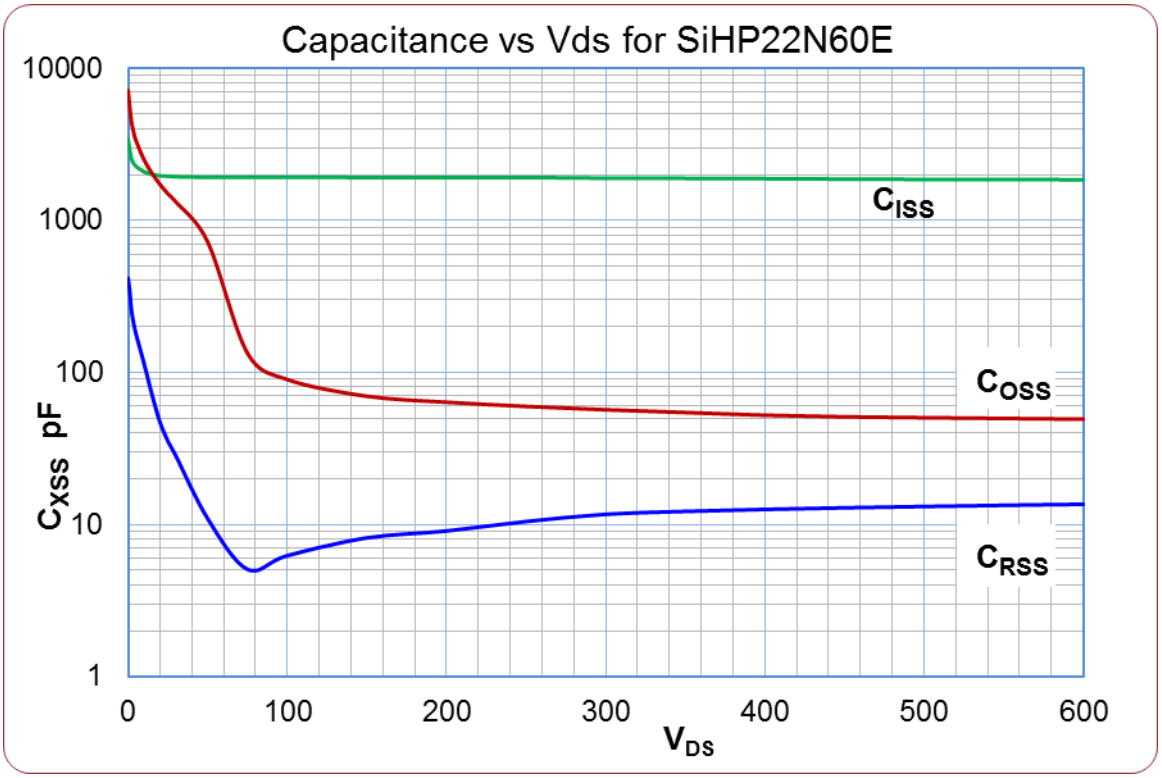

Fig. 4. Capacitance variation for superjunction MOSFETs.

This is an empirical relation derived to match observed switching times for high-voltage MOSFETs and works well enough for the current generation of superjunction devices. It may be pointed out that several authors have used Q_{GD} instead of Q_G in the conventional FOM to make it more meaningful. As seen here, neither number relates directly to T_{SW}, which is the real parameter relating to switching loss.

Having estimated the switching charge, the total switching losses are written as:

$$P_{SW} = \frac{1}{2} \times I_{AC} \times V_{DC} \times T_{SW} \times F_{SW} = \frac{\sqrt{2}}{\pi} \times \frac{P_{IN}}{V_{IN}} \times V_{DC} \times \frac{Q_{SW}}{I_{GEQ}} \times F_{SW}$$

In a hard-switched circuit like the CCM PFC, the MOSFET output capacitor is charged and discharged dissipatively during every cycle. As a result, the stored energy E_{oss} is lost twice in every switching period. The losses are given by:

$$P_{OSS} = 2 \times E_{OSS} \times F_{SW} \cong C_{OER} \times {V_{DC}}^2 \times F_{SW}$$

Again, because of the highly nonlinear characteristics, the energy stored in C_{oss} at high voltage needs a different calculation. The conventional capacitive energy formula of ½ CV^2 does not apply here. To calculate the stored energy, MOSFET manufacturers specify an additional parameter called C_{OER}. This is usually specified at 400 V or 480 V and is the equivalent constant capacitor that has the same stored energy as the MOSFET C_{oss} at those voltages. More recently, manufacturers have started including the complete E_{oss} curve in datasheets.

In PFC circuits, the body diode is not in the picture, so V_{FWD} and Q_{RR} and their associated losses can be ignored. Further, the typical switching frequency for PFC circuits in CCM mode is comparatively low at 65 kHz to 70 kHz. The low frequency, combined with low Q_G, implies that gate-drive losses do not contribute much and can be ignored as well. The total losses are now obtained by summing:

$$P_{TOT} = \left(\frac{P_{IN}}{1.2 \times V_{IN}}\right)^2 \times TCR \times R_{DSON} + \frac{\sqrt{2}}{\pi} \times \frac{P_{IN}}{V_{IN}} \times V_{DC} \times \frac{Q_{SW}}{I_{GEQ}} \times F_{SW} + C_{OER} \times {V_{DC}}^2 \times F_{SW}$$

The expression may appear rather complex and unusable, but a closer inspection reveals that most of the application-related values are already known by design. We substitute the following values commonly used in PFCs:

- V_{IN} = 100 V ac minimum
- V_{DC} = 400 V dc
- F_{SW} = 70 kHz
- TCR = 2 for 600 V MOSFETs.

The loss equation now simplifies to

$$P_{TOTAL} = 0.139 \times {P_{IN}}^2 \times R_{DSON} + 0.123 \times P_{IN} \times \frac{Q_{SW}}{I_{GEQ}} + 0.012 \times C_{OER}$$

where P_{IN} is in kilowatts (kW), R_{DSON} is in milliohms (mΩ), and Q_{SW} is in nanocoulombs (nC).

It is worth reiterating that the purpose of the equation is not to calculate losses with a high degree of precision, but to use it as a tool to compare different devices. For any given value of P_{IN} and equivalent gate current I_{GEQ}, one can look up the values for R_{DSON}, Q_{SW}, and C_{OER} from the MOSFET datasheets and compare losses. Using P_{TOTAL} as the loss-based FOM, the device choice is now based on the expected losses, derived for real-world operating conditions, instead of R_{DSON} x Q_G, which is at best an indirect pointer.

To illustrate this further, consider a reference device rated at 600 V with the following values:

- R_{DSON} = 100 mΩ

- Q_{sw} = 16 nC
- C_{OER} = 120 pF at 400 V.

Assuming the same R_{DSON} x Q_G product, and scaling all capacitances inversely with respect to R_{DSON}, we can generate a number of hypothetical devices with R_{DSON} varying from 50 mΩ to 500 mΩ. Using the loss equation for different values of P_{IN} yields the performance curves shown in Fig. 5. Looking at the loss curves, two conclusions may be drawn immediately.

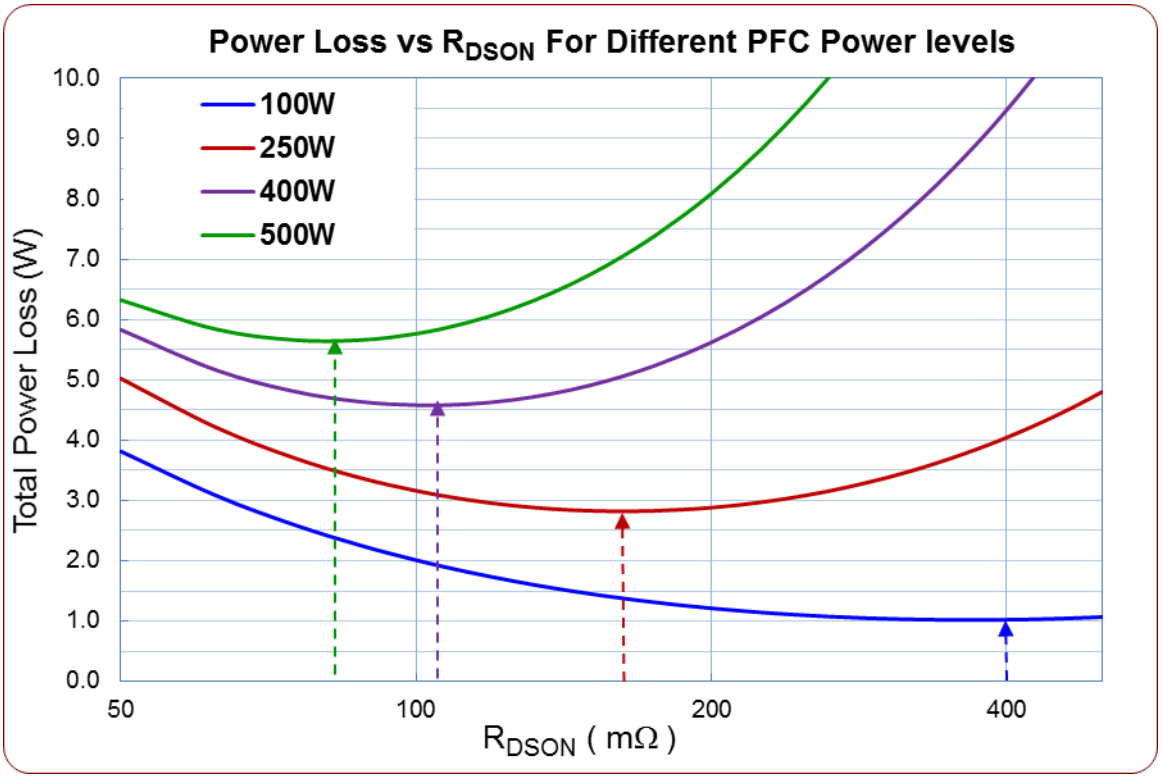

Fig. 5. Power loss as a function of R_{DSON}.

First, "lowest R_{DSON}" does not offer the lowest-loss solution under any operating condition. At any given power there exists an optimum value of R_{DSON} at which system efficiency is maximized. Moving away from the optimum to lower R_{DSON} not only adds to the cost but also increases overall losses.

For example, a 400-mΩ MOSFET can have the same performance as a 70-mΩ device at 250-W output, though neither is the right choice for that power level. The optimum value is in the range of 160 mΩ to 170 mΩ.

Second, R_{DSON} x Q_G itself is a poor guide to performance. All of the devices compared in the graph have the same exact R_{DSON} x Q_G product but can offer different performances depending on the operating conditions.

Conclusion

The inadequacies of the conventional R_{DSON} x Q_G product as a guide for MOSFET selection have been demonstrated. A better method using loss analysis of the system is proposed as an application-specific FOM. It involves estimating application losses as the weighted sum of various device parameters. The weight assigned to each parameter is based on operating conditions such as switching frequency, gate drive, and output power.

The relevance of the proposed FOM is illustrated in the practical PFC circuits for computing power supplies in the 100-W to 500-W power range. Even with a number of simplifying assumptions, a first-order, loss-based FOM is a superior tool to select the optimum device for the lowest-loss design.

Reference

Jess Brown, "Power MOSFET basics: Understanding MOSFET characteristics associated with the Figure of Merit." Vishay Siliconix Application Note AN-605, 2003, http://www.vishay.com/mosfets.

About The Authors

Sanjay Havanur is currently the senior manager for system applications at Vishay Siliconix. Previously, he served as the principal applications engineer at Alpha & Omega Semiconductor. Since receiving his Master's Degree in Power Electronics and Drives at the Indian Institute of Technology, Mumbai in 1983, Havanur has gained extensive experience in the field of power electronics, having worked in design and applications in both India and the U.S.

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For further reading on MOSFET characteristics and operation, see the How2Power Design Guide, select the Advanced Search option, go to Search by Design Guide Category and select "Power Transistors" in the Component category.