In-depth Report Documents Embedded Substrate Technologies Available For Development of Higher-Density Power Sources

At the Applied Power Electronics Conference last month in Charlotte, N.C., the Power Sources Manufacturers Association's (PSMA) Packaging Committee published a report titled "Current Developments in 3D Packaging With Focus on Embedded Substrate Technologies." A follow-up to the report on 3D packaging in power, which the PSMA published at last year's APEC, this new report is considered the first comprehensive study on using embedded substrate technology for building power sources.

This report contains extensive research and numerous product illustrations geared to an audience of technology executives and design engineers. Its purpose is to offer an in-depth industry perspective on how currently available materials and processes can be best used for the creation of advanced high-efficiency, high-power-density power products.

Co-chairs of the PSMA Packaging Committee, Ernie Parker of Crane Aerospace & Electronics and Brian Narveson of Narveson Consulting, describe the report as "the first comprehensive document to discuss the challenges companies will face to implement embedded substrate 3D power packaging to create the significantly higher power densities driven by the "More than Moore" digital power demands."

The PSMA created the 3D packaging report to address the pressing demands in the power industry to accelerate the development of higher-density power sources. The PSMA notes two key drivers for 3D packaging with embedded substrate technology. One driver is the trend toward higher power loads, while the other is the performance limiting effects of conventional power packaging.

In terms of the loads, the challenge arose from digital semiconductor packaging technology hitting a "cost barrier" brought about when advanced deep-submicron semiconductor technology could no longer reduce cost with the addition of more functions to the semiconductor die. This barrier was circumvented through the development of wafer thinning that enabled through-silicon-via (TSV) technology and the eventual introduction of 2.5D and 3D integration, which facilitated heterogeneous ("More than Moore") integration.

This integration allowed the power requirements of the digital load to increase two to five times, within the same footprint, in a single generation. Now the power industry is tasked with finding ways news ways to package power sources that will meet this demand, but without increasing footprint.

In parallel, power semiconductor technology is facing a "construction barrier" that prevents the realization of the significant benefits new technology can offer in terms of increased power efficiency and higher power density. These new technologies, including gallium-nitride (GaN), silicon-carbide (SiC), and gallium-arsenic (GaAs) power semiconductor devices, all require operation in a package that is free of bond wires and that minimizes parasitic interconnect elements. Both of these challenges can be addressed with power packaging utilizing embedded substrate technologies and are addressed in the report.

The PSMA's 340-page report, prepared under contract by LTEC Corporation with work subcontracted to Anagenesis and Fraunhofer-Institute, is based on the Packaging Committee's extensive research of over 750 articles and papers, analysis of 450 presentations/papers, and by conducting 30 industry expert interviews. Information was also derived from attendance at 10 industry conferences, workshops and seminars. The report contains 172 links and 394 citations.

The report provides detailed analysis of substrates (organic and inorganic), components (actives and passives), thermal management, high temperature die, packaging technologies, interposers, as well as additive manufacturing and laser fabrication. Each passive component (resistors, capacitors, inductors) has an entire chapter detailing which suppliers are currently shipping products usable in power sources.

Every chapter covers manufacturing issues and includes references to contract manufacturing companies already producing power products utilizing embedded substrate technology. Embedded substrate packaging leverages the large investment made by the digital industry in advanced packaging technologies and is being used to resolve the power source construction challenge. As the report demonstrates, 3D power packaging using embedded substrate technology is a disruptive technology, in that it enables large increases in power density and efficiency. Examples of embedded substrate technology are shown in Figs. 1 - 3.

The PSMA report on 3D packaging will be provided free of charge to PSMA members. Others interested in the report may order a copy from PSMA for $2,990.

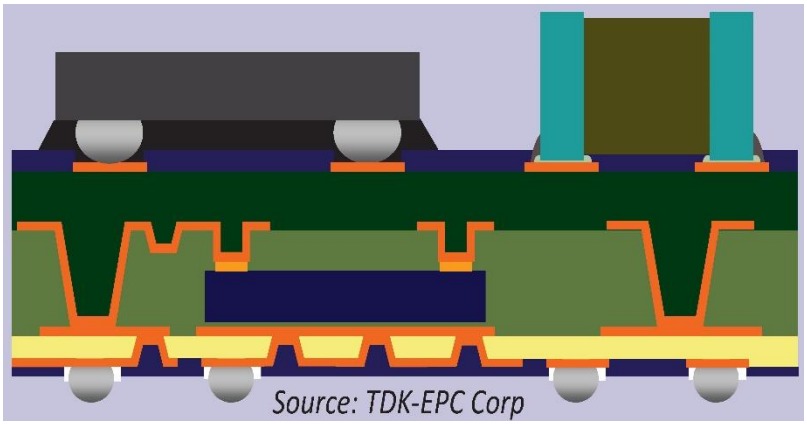

Fig. 1. The PSMA defines a 3D Embedded Power Module as a "system that uses a combination of at least one controller/driver IC, at least one active component in the power train, and associated interconnect means, embedded in a single package." Another key term, "component embedding," is defined as "the inclusion of at least one active or passive electrical component within the top and bottom conductive layers of a substrate."

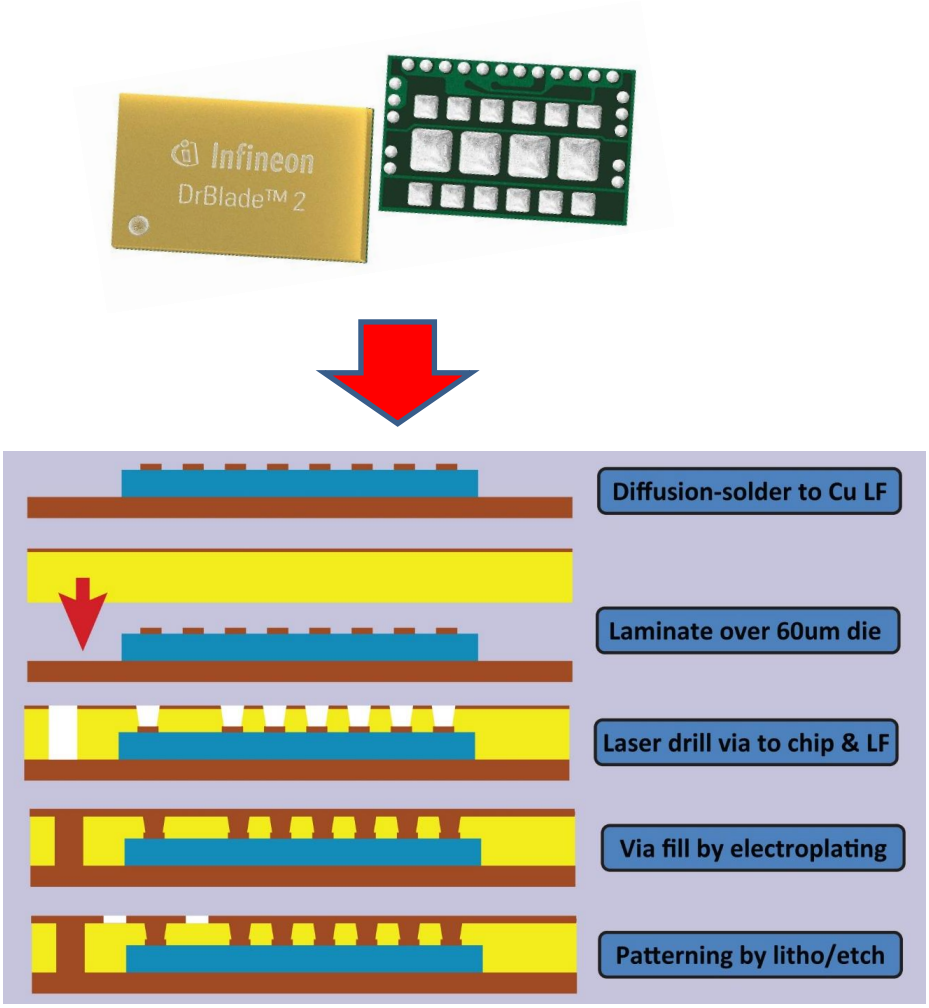

Fig. 2. Infineon's DrBlade 2 power stage combines three chips in a single 6.6-mm x 4.5-mm package—a high-side/low-side halfbridge configuration with a driver IC optimized to achieve peak efficiency values greater than 95%. The completed device and the package fabrication process are shown here.

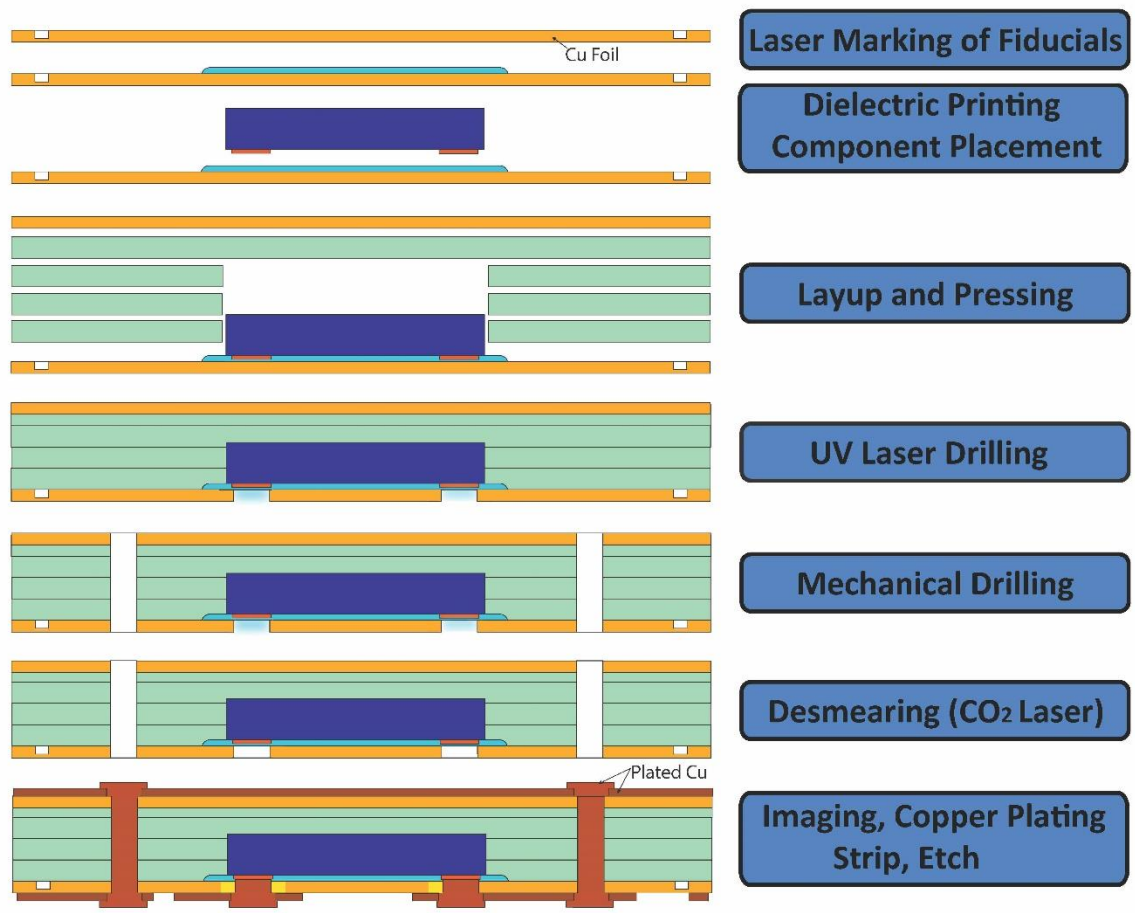

Fig. 3. The AT&S embedded component packaging process flow. According to Yole Développement, AT&S is the largest producer of embedded substrates for the power industry. Their technology easily adapts to embedding higher-power semiconductors and passives, yet is a cost-effective process utilizing conventional PCB manufacturing techniques.