ISSUE: July 2015

Advantages Of GaN FETs Versus "Best Of Breed" Silicon MOSFETs

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It's just good engineering to scrutinize the hype that follows the introduction of any new technology. GaN power FETs are an excellent example where the caveats are less exposed than their benefits. When should we abandon the established recent generation of silicon MOSFETs with proven reliability, high performance, and low cost for the claims made about GaN devices?

In this article, I examine some of the claims made about GaN power transistors from my perspective as a power system designer and development consultant for a large semiconductor corporation. Since many engineers (myself included) have been skeptical about the claims and comments made about GaN, in order to address these concerns, I have framed this discussion as a dialogue with an alter ego.

From The Obvious To The Subtle

GaN is great!

Alter ego: "Really? So prove it! And don't give me that marketing mumbo jumbo and colorized graphs without any real measurements and just vague references to efficiency."

The past decade has introduced many improvements in power switching technologies.

"No kidding, Einstein!"

The recent generation silicon MOSFETs have far fewer losses in application due to lower capacitance values, lower $R_{DS(ON)}$, and other properties that have reduced delays and improved thermal paths and lead inductances. All of this permits faster switching while creating lower losses.

"Yadda, yadda…ok, get to the point and do your spiel."

The availability of gallium nitride on silicon substrates reveals a potential competitor to all-silicon MOSFETs due to their higher electron mobility while constraining their cost. These HEMT, or high electron mobility transistors, are better switches that fit on a much smaller die.

"What? You couldn't find any cheap sapphire or diamonds?"

Some readily available GaN devices at or under 200 V perform in "enhancement mode" such that they are normally off. Many devices over 200 V are in "depletion mode" similar to a JFET and are normally on.

Many companies create a cascode circuit of two devices in series (Fig. 1) such that the high-voltage d-mode GaN device (let's assume a typical 600-V V_{DS} is required) is atop a low voltage e-mode silicon MOSFET, permitting the switching control by simple drive of the bottom MOSFET.

"Hmm, so if I want a high-voltage GaN part to replace a typical MOSFET, I'm really looking at two transistors in series. That doesn't seem better!"

Fortunately, until a true high-voltage GaN e-mode part is practical, low-voltage silicon MOSFETs (i.e. 30-V V_{DS}) are readily available with very low $R_{DS(ON)}$ values and very low drive charge requirements. Selection of the low-voltage MOSFET parameters may easily be an order of magnitude lower than the GaN device used, therefore, having little detriment on performance in general.

"What do you mean by 'in general'? Sounds like there's a catch!"

Construction of a cascode pair (see Fig. 1 again) must be done carefully such that when it is considered that (Q2) the bottom e-mode MOSFET's output capacitance, or C_{OSS}, will affect a delay at turn-off.

The moment the bottom MOSFET is off, the voltage on the GaN source (Q1) must rise with the MOSFET's output capacitance until the GaN can be off.

Assuming the gate of the GaN part is at 0 V, the source may need to rise above 10 V to 20 V or more for the current to completely stop.

This is not a problem for turn-on, in general.

"In general, again?"

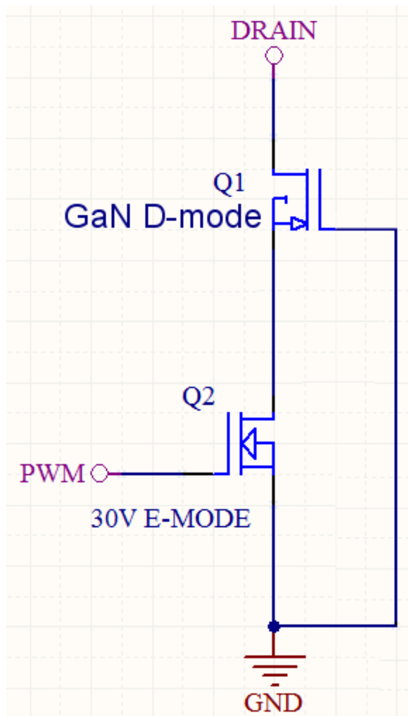

Fig. 1 For GaN devices above 200 V, most manufacturers offer a cascode pair that combines a low-voltage, enhancement-mode silicon MOSFET with a depletion-mode GaN transistor.

A GaN power FET is a fast switching device such that upon applying proper gate-to-source voltage, the turn-on delay is very short and fixed (3 to 5 ns, device dependent) over temperature and V_{DS} operating points. Current rise is then instantaneous as there is little or no "plateau" in the gate voltage.

Some of the devices I've tested have shown 400 V switching with voltage fall times (T_{vf}) within 6 ns.

"Woo hoo! 67 kV per microsecond!"

The GaN device has a very large transconductance and very little plateau due to a very small C_{RSS}, and unlike many silicon MOSFETs, adding gate resistance does not help shape the rate of switching to minimize EMI concerns. Some applications may require snubbers to control noise and ringing due to such fast transitions.

"Uh oh, I may need to shield this sucker!"

In the turn-off transition, the high-voltage GaN device has nearly a consistent delay, regardless of operating points of voltage or current. Voltage rise under 3 ns in a 400-V circuit has been observed as well as current fall times under 10 ns. In consideration of a complete application and current applied to circuits, any stray inductance in connections now has the potential to create severe spikes, noise, ringing, and device destruction.

"So, sometimes better is not better?"

Device performance shown below was made from a mature high-voltage power GaN device operated singly (without a cascode construction) and compared with the best of Infineon's CoolMOS devices that had similar $R_{DS(ON)}$ and V_{DS} parameters. The GaN device is proprietary and differences in performance from different manufacturers are possible.

Rather than citing figures of merit (FOMs) common in marketing, these simulations look at how these parts perform as operating points are swept. How do they compare as we change voltage, current and switching frequency?

"Good question!"

Beforehand, we must put parameters into perspective. Fig. 2 shows the parameters of interest when switching.

"I've seen this old stuff before. Do I really have to crank these numbers to see a difference between the parts?"

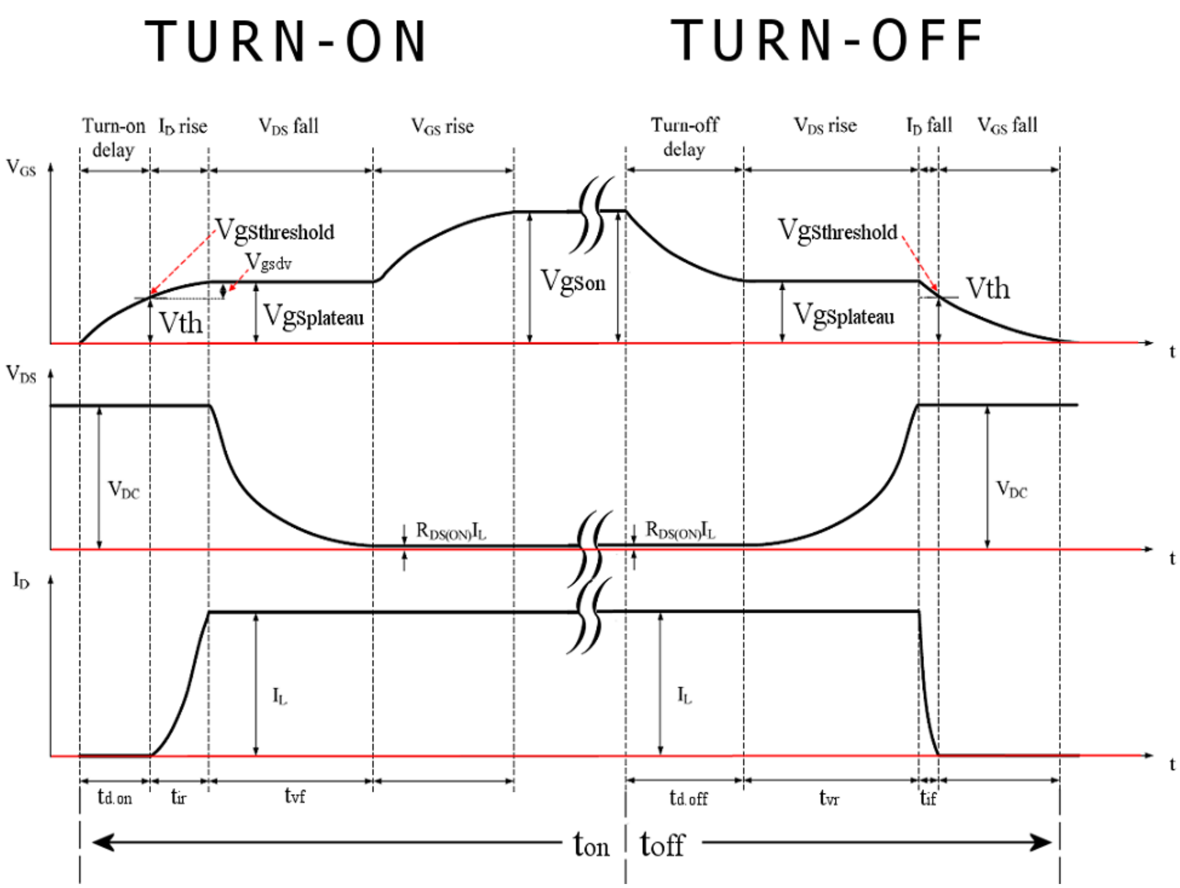

Fig. 2. Measurements of switching characteristics for a high-voltage GaN power switch.

An example of deriving parameters from calculations:

$g_{fs} = di_{ds}/dv_{gs}$

$V_{gsplat'} = V_{gdrv} - V_{gsplat}$

$V_{gx} = V_{gdrv} - V_{th}$

$V_{sat} = R_{ds}' \times I_{sw}$

$t_{d.on} = R_{ghi}(C_{iss'})\ln(1/(1-(V_{th}/ V_{gdrv}))$

$t_{ir} = R_{ghi}(C_{iss'})\ln(g_{fs}V_{gx}/(g_{fs}V_{gx}-I_{ds}))$

$t_{vf} = (V_{ds} - V_{sat})(R_{ghi})C_{gd}/(V_{gplat'})$

$P_{swon} = F_{sw}(I_oV_{ds}/2)(T_{pwr.on})$

$T_{pwr.on} = (t_{vf} + t_{ir})$

$t_{d.off} = R_{glo}(C_{iss})\ln(V_{gdrv}/V_{gsplat})$

$t_{vr} = kV_{ds}C_{rss}(R_{glo})/(V_{gsplat'})$

$t_{if} = C_{iss}(R_{glo})\ln(V_{gp}/V_{th})$

$P_{swof} = F_{sw}(I_oV_{ds}/2)(T_{pwr.off})$

$T_{pwr.off} = (t_{vr} + t_{if})$

"I'm cross-eyed now. Please don't bore me with formulas. I want data and graphs!"

Evaluating Real Devices

This example applies parameters that were specified by manufacturers and measured for verification; a result was found that compared three different parts in an application operating at 500 kHz while switching 400 V and 10 A with a 50% duty cycle (Table 1.) At first glance, it is apparent that the GaN part has a considerable efficiency advantage.

Table 1. Comparison of a depletion-mode GaN power device with best-in-class silicon superjunction MOSFETs from Infineon (proprietary data protected.)

	GAN	50R190	50R280	
Vgatedrv+	[illegible]	10.0	10.0	V
Vgatedrv-	[illegible]	0.0	0.0	V
Vgatedrv	[illegible]	10.0	10.0	V
Igatemax+	[illegible]	7.1	7.1	A
Igatemax-	[illegible]	9.7	9.7	A
Rgdrv+	[illegible]	2300	2300.0	mΩ
Rgdrv-	[illegible]	1900	1900.0	mΩ
Rg ext	[illegible]	500	500.0	mΩ
Rg int	[illegible]	3000.0	3000.0	mΩ
Rghi	[illegible]	5800.0	5800.0	mΩ
Rglo	[illegible]	5400.0	5400.0	mΩ
Vth actual	[illegible]	3	3	V
Vgsplat act	[illegible]	5.3	5.3	V
Vgsplat	[illegible]	5.3	5.3	V
Vgsplat'	[illegible]	4.7	4.7	V
Vgx	[illegible]	7.0	7.0	
Vth	[illegible]	3.0	3.0	
gfs	[illegible]	8.0	8.0	S

	GAN	50R190	50R280	
Coss	[illegible]	68.0	49.0	pF
Ciss	[illegible]	1137.0	773.0	pF
Crss (Cgd)	[illegible]	12.0	10.0	pF
Coss'@Vp	[illegible]	**10.5**	**7.6**	pF
Ciss'@Vp	[illegible]	**365.0**	**248.1**	pF
Crss'@Vp	[illegible]	**0.3**	**0.25**	pF
Qg	[illegible]	47	32.6	nC
Qgd	[illegible]	24.5	17.1	nC
td.on	[illegible]	0.755	0.513	nS
tir	[illegible]	0.843	0.573	nS
tvf	[illegible]	0.147	0.123	nS
Tpwr.on	[illegible]	0.991	0.696	nS
td.off	[illegible]	3.898	2.650	nS
tvr	[illegible]	0.138	0.115	nS
tif	[illegible]	3.494	2.376	nS
Tpwr.off	[illegible]	3.632	2.490	nS

	GAN	50R190	50R280	
Rds'@Fsw	[illegible]	**190**	**280**	mΩ
Rds@25C	[illegible]	160	250	mΩ
Rds@100C	[illegible]	300	450	mΩ
Tempco	[illegible]	2.5%	2.4%	
Tempco	[illegible]	187%	267%	
Vsat	[illegible]	1.900	2.800	V
$P_{RDS\ ON}$	[illegible]	**13435**	**19799**	**mW**
Pswon	[illegible]	1981	1392	mW
Pswof	[illegible]	7264	4981	mW
Pcoss	[illegible]	420	303	mW
Ploss AC	[illegible]	**9665**	**6675**	mW
Pd total	[illegible]	**23100**	**26474**	**mW**
ΘJA	[illegible]	3.0	3.0	°C/W
$T_{JUNCTION}$	[illegible]	**94.3**	**104.4**	°C
P_{QGATE}	[illegible]	470	326	mW
P_{TOTAL}	**14984**	**23570**	**26800**	**mW**

The example shown compares a very recent "best of breed" series of Infineon CoolMOS devices with a depletion-mode GaN part that has similar $R_{DS(ON)}$ and a higher voltage rating.

Note, that in this calculation, the two MOSFET parts show similar total losses (within 13%), but differ such that the device with lower $R_{DS(ON)}$ has obvious lower dc loss, yet higher ac loss which can blur a decision on which to use in an application.

"Yeah, but my application is different!"

To better realize how the parts compare requires sweeping all operating conditions.

In the following figures, an application for a 400-V dc boost circuit is simulated using a 50% fixed duty cycle while the load current and frequency of switching is varied.

Fig. 3 depicts anticipated power loss for each of the three devices selected with separate graphs for the ac portion of losses and the total power losses.

For exaggeration, Fig. 4 depicts very high switching frequencies used (for freaks only.)

Note that the ac losses between the three devices maintain a given ratio and all scale with switching frequency in the same manner. These ac losses include all dynamic issues and exclude the device loss associated with a static loss derived from $R_{DS(ON)}$ and the current (i.e. I^2R.)

Considerations for a condition called "dynamic $R_{DS(ON)}$" related to GaN devices is applied.The GaN device used has an $R_{DS(ON)}$ that varies above and below the two MOSFETs $R_{DS(ON)}$ values.

This condition occurs under various operating voltages, frequency, and duty cycles, where the apparent switch resistance can vary nearly 50%. Typically, the $R_{DS(ON)}$ increases with V_{DS} and frequency.

Frequency of switching and duty cycle both relate to time and we must assume that within the GaN structure and interface with the silicon substrate there are areas of charge that affect the device performance.

"Yep, I'll be looking for that white paper. Let's see the data!"

It is important to note in all cases that the GaN device does not prove the best efficiency choice at low current levels. Also, the "cheaper" MOSFET, with about 50% higher $R_{DS(ON)}$, will show lower total losses when compared at higher frequencies with the MOSFET with lower $R_{DS(ON)}$ due to its lower capacitance.

The example at 200 kHz shows that under 3.5 A of switching current, the total loss between the MOSFET devices is very similar. Therefore, in low-current applications, the decision to choose the cheaper part is easy.

An overall conclusion can be made that the GaN part is superior with regards to efficiency, but what is less obvious is that GaN devices can also operate at much higher temperatures than silicon MOSFETs.

The MOSFETs selected here are rated for operation up to a 150°C junction temperature while the GaN devices may perform beyond 200°C despite the commercial ratings specified.

"Doesn't the solder on the pc board melt off around that temperature? And don't pc boards start to delaminate around 150°C? So, maybe that's not a selling point."

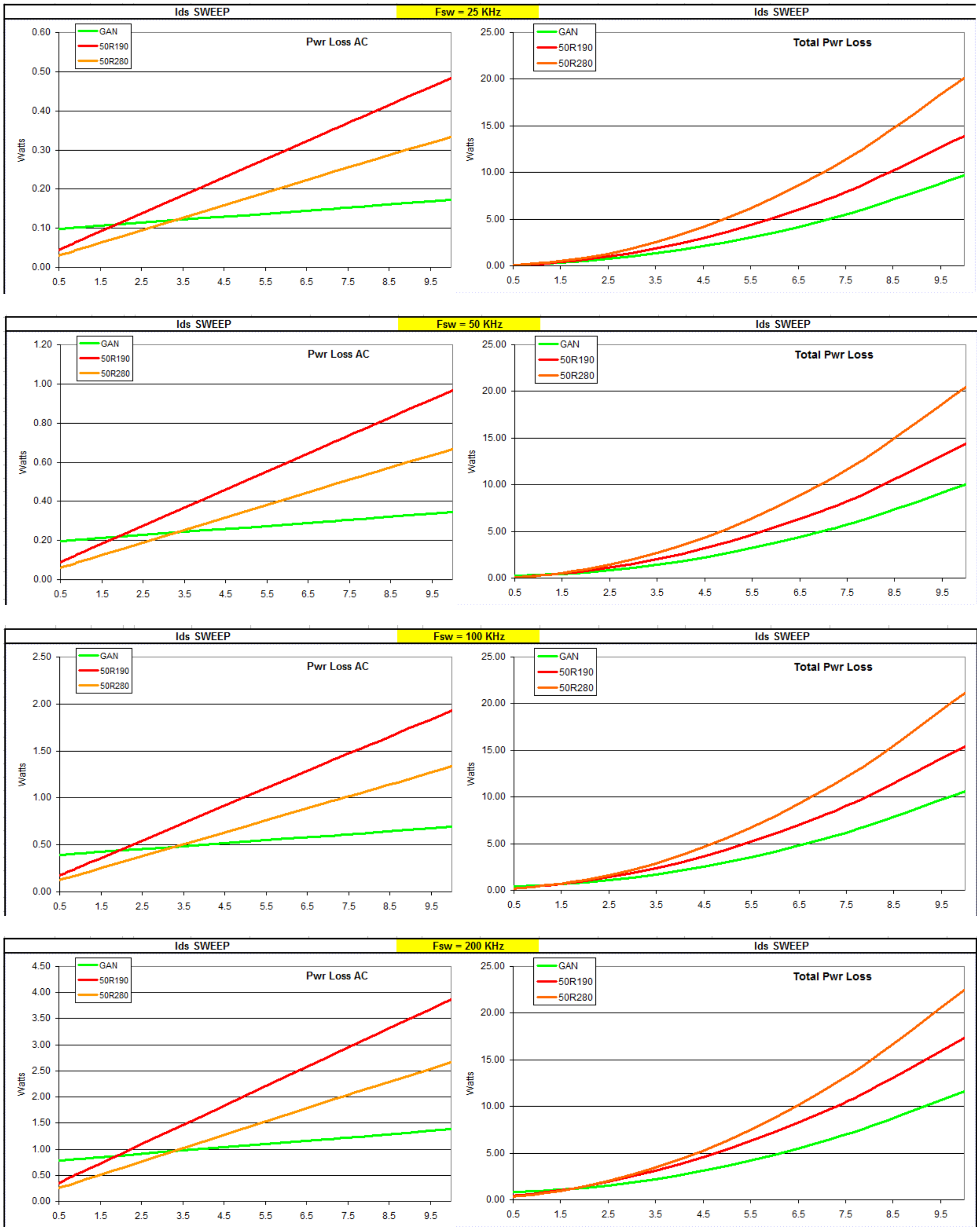

Fig. 3. Simulation of power losses for the GaN device and silicon MOSFETs (the ones described above in the table) in a 400-V dc boost converter. Losses are simulated here for relatively normal switching frequencies ranging from 25 kHz to 200 kHz.

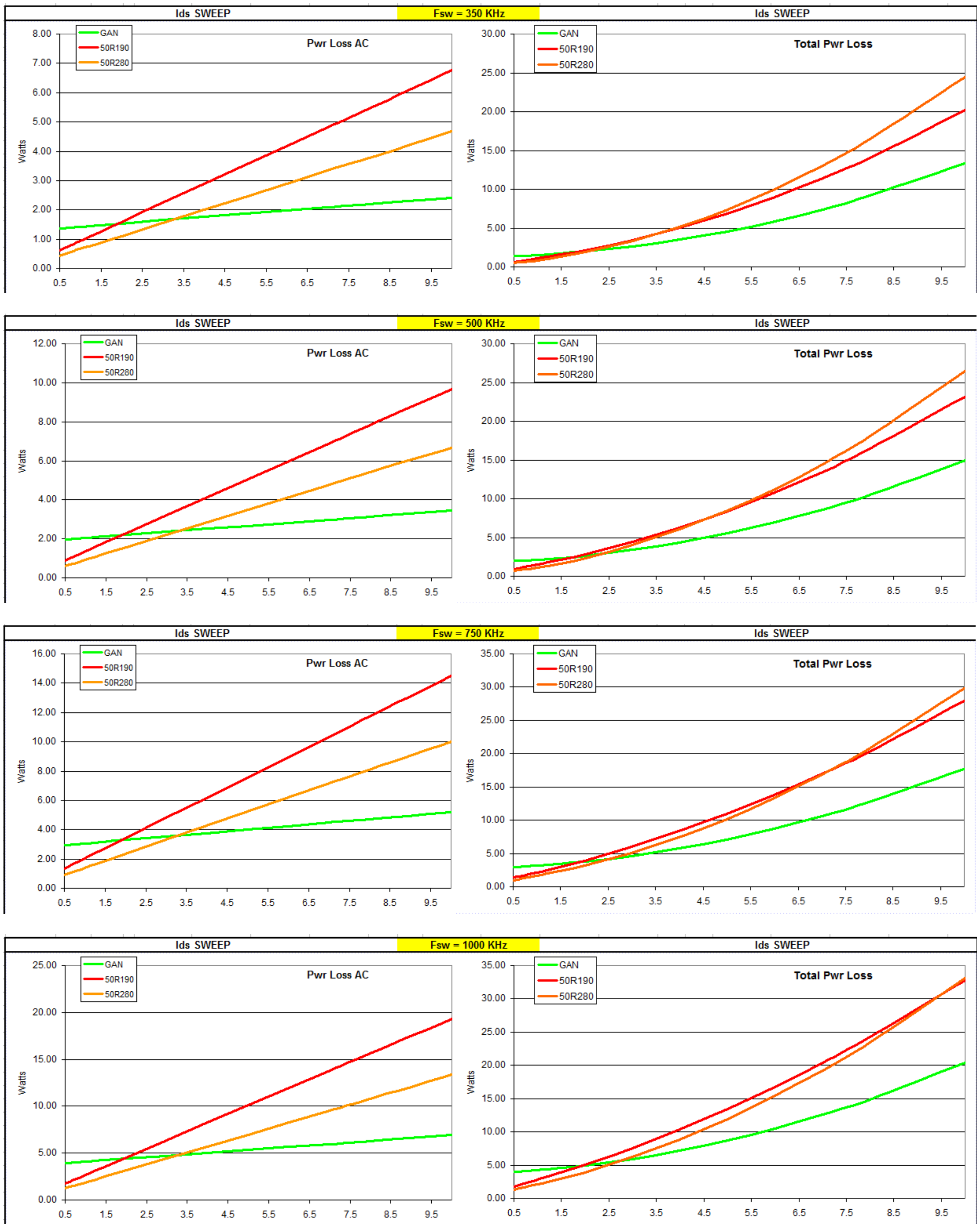

Fig. 4. Simulation of power losses for the same GaN device and silicon MOSFETs in a 400-V dc boost converter at higher switching frequencies of 350 kHz to 1 MHz.

Physical Proof Testing

The simulations shown have been verified by actual experimentation using the devices in a common PFC-type 400-V dc boost application supplying loads up to 1 kW and measuring efficiency across various levels of constant-current loading and sweeping the switching frequencies from 100 kHz to 1 MHz.

Thermal management in very lossy conditions was difficult and the MOSFET devices did not survive more than a few seconds while operating above 750 kHz due to thermal runaway.

The GaN device survived switching at up to 1.3 MHz. The testing was concluded once the FLIR camera measured the device body at 185°C.

"Wow, hot stuff!"

A conclusion observed from actual application is that due to high gain and fast switching, the drive path of gate to source should be separate from the switched current path of drain to source. Ultimately, the best part will be a four-terminal device.

The final word (at least for this article) is that engineers are always limited by the available materials for their designs. It will be an easy choice to use GaN devices once they are easily driven and their costs approach conventional MOSFETs. Super fast, efficient, and rugged—if applied appropriately—GaN is really great!

About The Author

CEO and owner of Avatar Engineering Corporation, Anthony Esposito, has over 35 years of experience in power conversion and precision instrumentation for all markets—consumer, industrial, telecommunications, automotive, green-power, medical, military, and space. Present activities include new semiconductor research, high-efficiency converters for military and medical applications, and miniature high-voltage transformers for next-generation Taser weapons.

Prior work includes medical MRI gradient amplifier and systems design, telco cell site power systems design, as well environmental controls design for NASA's original Enterprise Shuttle. The New Product Development (NPD) software, "EQuote" (short for Engineering Quote) has been used extensively by the SBA and Harvard Business.

Esposito resides in Arizona, is degreed in electrical engineering, business, and computer science, has numerous patents in power controls and communications, and often mentors young engineers on the joys of analog and magnetic component design, and entrepreneurship.

For further reading on designing power converters using GaN power devices, view the How2Power Design Guide's search results for SiC and GaN by clicking here. And for more technical information relating to GaN, see How2Power.com's section on Silicon Carbide and Gallium Nitride Power Technology.