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Novel GIT Structure Solves Current Collapse In GaN Power HEMTs

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The advantage of GaN power devices in terms of performance is no longer hype but a reality that has empowered many power supply designers to build new applications that are more efficient, compact and able to operate in harsher environmental conditions. With a projected market size of U.S. $600 million in 2020 and a CAGR of 80% to 2020[1], many new players have entered the field and are introducing new devices at an exceptional rate.

Naturally, the question arises of whether the devices are reliable enough with sufficient understanding of their failure modes. Panasonic has devoted much time to qualifying its X-GaN[2] devices, especially under actual-use conditions. One particular failure that is unique to GaN devices is the current collapse phenomenon. It causes an increase in dynamic $R_{DS(ON)}$ that can lead to catastrophic failure of GaN devices and the systems in which these devices are implemented.

So far, Panasonic is the only GaN device vendor that has openly declared the complete elimination of current collapse. The company has also understood that the standard qualifying methodologies i.e. JEDEC and AEC are insufficient in terms of testing for current collapse. Therefore, for the first time ever, this article will describe a novel hybrid-drain gate injection transistor structure and a dynamic testing procedure developed to ensure that Panasonic X-GaN is highly reliable.

Root Cause Of Current Collapse

The phenomenon of dynamic $R_{DS(ON)}$ increase—the so-called current collapse, which is depicted in Fig. 1—is caused by trapped electrons between the gate and drain in a GaN FET. The electrons can be trapped when high-drain-bias is applied as shown in Fig. 2, and may not dissipate instantaneously when the device is turned on. The trapped electrons repel carriers in the channel layer, and the dynamic $R_{DS(ON)}$ increases because the number of carriers in the channel layer is reduced. It is evident that the increase in the dynamic $R_{DS(ON)}$ depends on the applied drain voltage and also the length of time the GaN FET is subjected to this voltage.

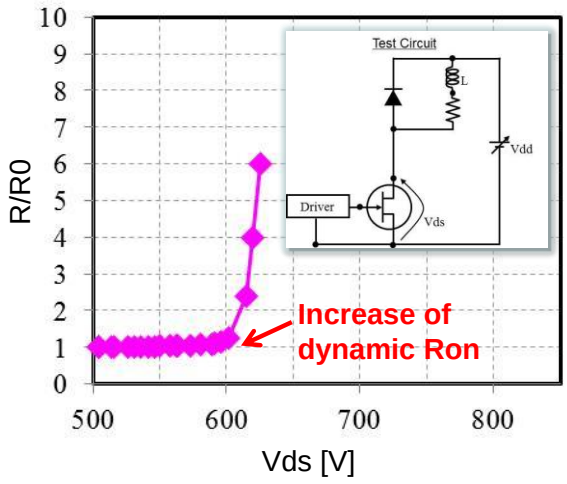


Fig. 1. Values of dynamic $R_{DS(ON)}$ normalized to the dc values (R/R0) in a conventional GaN FET.

Using Hole Injection To Eliminate Current Collapse

Fig. 2 shows Panasonic's unique approach to solving current collapse. Our approach is to introduce holes into the GaN device that release the trapped electrons instantaneously.

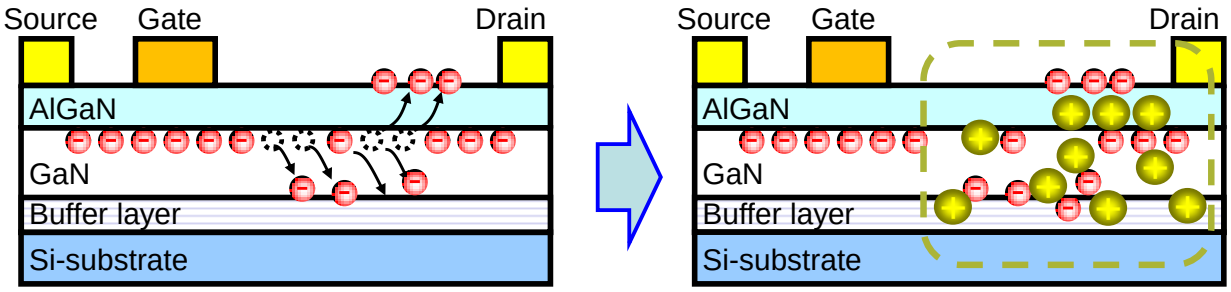


Fig. 2. Electrons trapped between the gate and drain in a GaN FET (shown on the left) are the cause of current collapse. Panasonic's unique approach to solving current collapse involves the introduction of holes in an added p-GaN region near the drain (shown on the right.)

In order to introduce holes into the device, an additional p-GaN region is incorporated near the drain. Fig. 3 illustrates schematic cross sections of a conventional gate injection transistor (GIT) and a new Hybrid-Drain-embedded GIT (HD-GIT). Normally-off operation with a p-type gate has been demonstrated in the conventional GIT and this work has been published.[3]

In the new GIT structure (shown on the right in Fig. 3) the additional p-GaN region is introduced near the drain and is electrically connected to the drain. The theory behind the addition of the p-type region is that holes injected in this region will effectively release the trapped electrons during the device's switching operation. The HD-GIT also employs a recessed gate to thicken the AlGaN layer to avoid carrier-depletion under the p-type region. The HD-GIT is confirmed to have dc characteristics that are identical to the conventional GIT.[4]

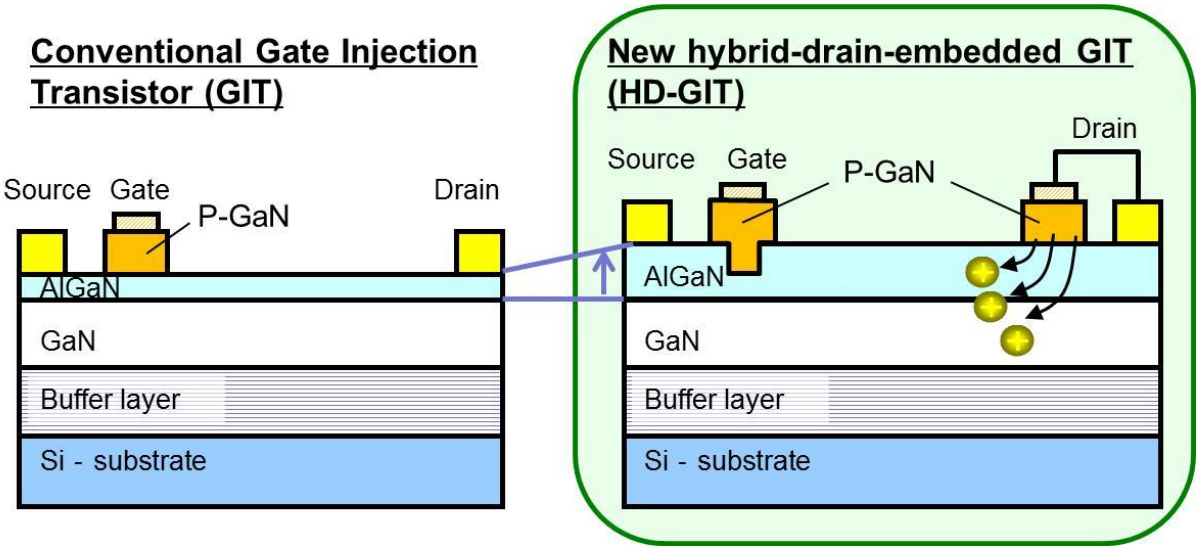


Fig. 3. Schematic cross sections of a conventional gate injection transistor (GIT) and a new Hybrid-Drain-embedded GIT (HD-GIT).

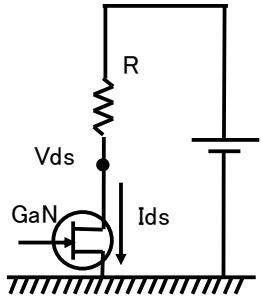
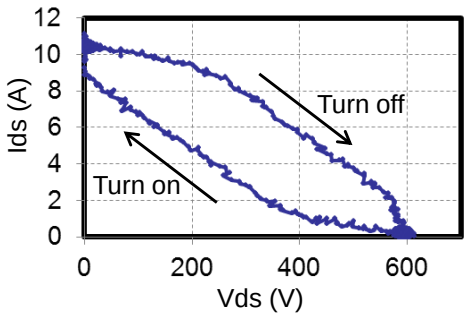
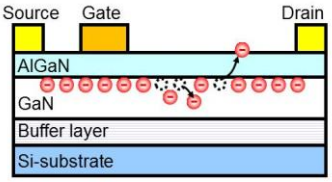
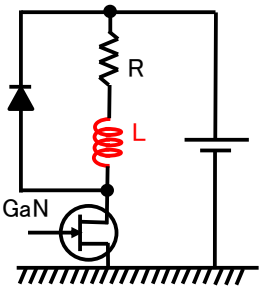
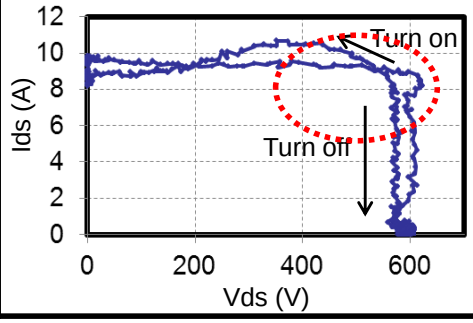
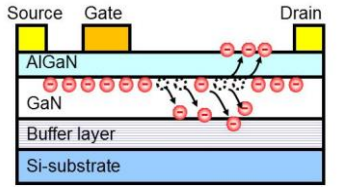
Inductive Hard Switching Testing

Before presenting the dynamic $R_{DS(ON)}$ characteristics of the HD-GIT, we'll discuss the dynamic testing procedure that is employed to ensure that the X-GaN devices are highly reliable.

The most severe switching test should be chosen for evaluating dynamic $R_{DS(ON)}$. Usually, two methods can be used to measure dynamic on-resistance—one is resistive-switching and the other is inductive hard switching.

The circuits and V-I locus for these methods are summarized in Table 1. As shown in the V-I locus, the inductive hard switching is more severe than the resistive switching, because the device is simultaneously subjected to both high currents and high voltage in a way that generates more trapped electrons. Therefore, the inductive hard switching method should be used to measure dynamic $R_{DS(ON)}$, which is relevant to achieving stable operation of the transistor in practical switching systems.

Table 1. Comparing resistive switching versus inductive switching as a means of evaluating dynamic $R_{DS(ON)}$.

	Circuit	Ids vs Vds (Locus)	Trapped charges in GaN-FET
Resistive switching			
Inductive switching			 More trapped electrons could be induced.

Dynamic Characteristics Of HD-GIT During Inductive Hard Switching

Fig. 4 shows both a test-circuit diagram and evaluation results for dynamic $R_{DS(ON)}$. Multi-pulse and inductive load tests are employed. Values of dynamic $R_{DS(ON)}$, R, normalized to the dc values, and R0, are plotted as a function of the drain voltages at the right.

As shown in the graph, the HD-GIT is free from current collapse even at 850 V while the sharp increase of the R/R0 is observed at 620 V for the conventional GIT and maybe even lower voltage for other competing GaN devices. Dynamic $R_{DS(ON)}$ is measured at 4.5 µs after switching from the off state to the on state. Note that the slight increase of R/R0 in the HD-GIT is due to the increase in the junction temperature during the measurement.

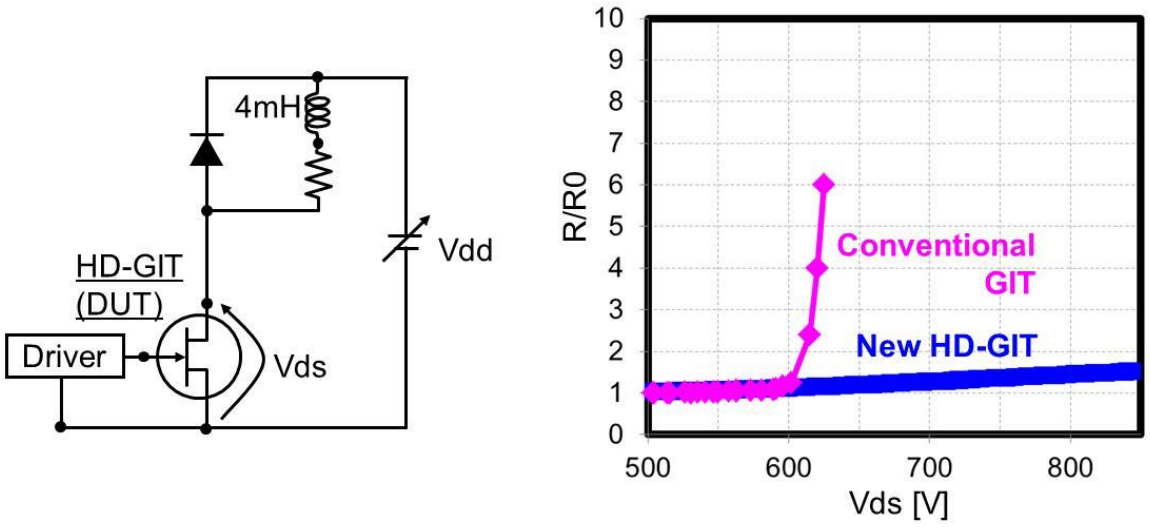


Fig. 4. The test circuit for inductive-load switching (shown on left) was used to measure the dynamic on-resistance of a conventional GIT and the new HD-GIT. The experimental results are shown in the graph on the right. Values of dynamic R_{ON} are normalized to the dc values (R/R0).

We evaluated the switching safe operating area (SOA) for one pulse of the GITs with an R_{ON} of 76 mΩ, also using the inductive hard switching method. Single-pulse SOA test results for both the conventional GIT and the new HD-GIT are shown in Fig. 5. As these measurements illustrate, the HD-GIT has a very large SOA, encompassing 800 V and 50 A, whereas the conventional GIT fails even at 800 V and 5 A. In both cases, the 50-A limit is determined by the drain current saturation of the GITs.

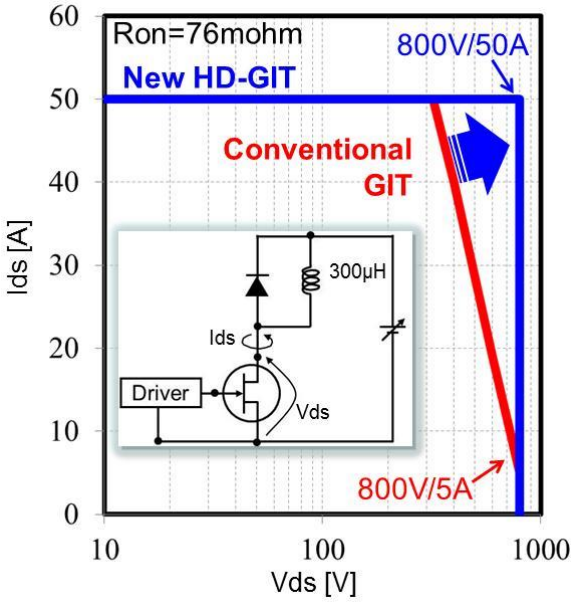


Fig. 5. The new HD-GIT has a greater switching safe operating (SOA) for a single pulse than a comparably rated conventional GIT.

Although there may be questions about the possible side effects of injecting holes such as turn-off delay, this apprehension is not valid at all. In fact, the HD-GIT has demonstrated the fastest switching characteristic the market has ever seen by achieving a dv/dt of 200 V/ns. We believe that the holes injected from the p-GaN region at the drain dissipate instantaneously with the recombination of trapped electrons without introducing any side effects.

Although other viable solutions have been demonstrated such as improvement of the surface properties and reduction of the electric field by field plate, the complete elimination of current collapse for normally-off or GaN power transistor cascodes with operating voltage at 600 V and above has never been published by any competing GaN vendors.

For power supply applications like power factor correction (PFC), the device should operate without the possibility of current collapse up to at least 400 V or higher. Otherwise, if designers use GaN devices that suffer from the dynamic $R_{DS(ON)}$ issue, they run the risk that the device will overheat in the application and be catastrophically destroyed. In other words, the unreliability of GaN power devices that are subject to current collapse outweighs their intrinsic benefits such as high-frequency switching and high junction-temperature capability.

With the HD-GIT structure employed in all Panasonic X-GaN devices, these results have ensured that the presented HD-GIT devices are robust and can maintain excellent performance even during hard-switching applications, where both high bias and high current are simultaneously applied. As mentioned earlier, the HD-GIT has also passed the standard qualifying methodologies i.e. JEDEC,[4] indicating that these devices are very promising for practical switching power supply applications and offer the customer a very safe and failure-free device for their disruptive applications.

References

1. "How Power Electronics will reshape to meet 21st century challenges?" by P. Gueguen, Plenary Sessions, ISPSD'15, HK (2015).

2. "Panasonic to Launch Industry's Smallest Enhancement-Mode 600V GaN Power Transistors Package" Panasonic press release about X-GaN, May 18, 2015.

3. "Gate Injection Transistor (GIT)—A Normally-Off AlGaN/GaN Power Transistor Using Conductivity Modulation," by Y. Uemoto, M. Hikita, H. Ueno, H. Matsuo, H. Ishida, M. Yanagihara, T. Ueda, T. Tanaka, and D. Ueda, IEEE Trans. Electron Device, vol.54, no.12, 3393 (2007).

4. "Current-collapse-free Operations up to 850 V by GaN-GIT utilizing Hole Injection from Drain," by S. Kaneko, M. Kuroda, M. Yanagihara, A. Ikoshi, H. Okita, T. Morita, K. Tanaka, M. Hikita, Y. Uemoto, S. Takahashi and T. Ueda, Proceedings of ISPSD'15, 41(2015).

5. Panasonic's GaN power devices, http://www.semicon.panasonic.co.jp/en/products/powerics/ganpower/.

About The Authors

Howard Sin is principal engineer at Panasonic Semiconductor Solutions (PSCS), where he has worked since 2004 and is currently a principal engineer leading the WBG devices business development, technical marketing and application support in the U.S.A. In addition, Sin has over nine years of experience in SMPS technology designing ultra-low standby power supply solutions. He holds a master of science degree in Power Engineering from the Nanyang Technological University, Singapore.

Saichiro Kaneko is chief engineer at Panasonic Semiconductor Solutions. Since 2011, he has been leading GaN power device design and reliability. Recently, Kaneko's presentation on current-collapse won the Best Paper Award at ISPSD 2015. From 1996 to 2011, he worked on the research and development of silicon lateral IGBTs and SiC wide-bandgap semiconductors. Kaneko graduated from Yokohama National University in 1996.

For further reading on GaN power devices, see How2Power.com's section on Silicon Carbide and Gallium Nitride Power Technology.