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Modeling The Effects of Leakage Inductance On Flyback Converters (Part 1): Converter Switching

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The frequency response of a flyback converter operating under voltage mode (VM) control and driven in continuous conduction mode (CCM) is that of a second-order system. If the vast majority of analyses predict a transfer function whose quality factor is solely affected by the various losses (ohmic paths, magnetic losses, recovery time-related losses and so on), very few tackle the damping effect brought by the leakage inductance.

However, transient simulations predict the damping of output oscillations as the leakage inductance increases. Because formulas available in the literature do not reflect this effect, a new flyback converter model is necessary and will be described in this article. Part 1 of this series begins by explaining the leakage inductance-induced damping effect on flyback waveforms and then deriving a new dc transfer function that accounts for this effect. Finally in this part, the leakage inductance effects will be observed in measurements taken on a prototype circuit.

The Flyback Converter In CCM

A perfect CCM flyback converter transmits power in two operating cycles: 1) the on-time t_{on} during which the primary-side power switch *SW* closes and energy builds up in the transformer primary inductance L_p and 2) the off-time t_{off} when the switch opens and energy is transferred to the secondary side via diode *D*. However, when scrutinizing the waveforms in a prototype, one can distinguished more states than the basic explanation describes.

Fig. 1 shows a typical converter featuring a transformer affected by a leakage inductance l_{leak}. When the power switch closes, the input voltage is applied across the transformer primary inductance L_p, neglecting the switch ohmic losses. Looking closer at the schematic in Fig. 1a, this is not exactly V_{in} that is applied across L_p since a divider made up of L_p and l_{leak} is at play here. The voltage across L_p during that moment is thus

$$V_{L_p}\Big|_{t_{on}} = V_{in}\frac{L_p}{L_p + l_{leak}} \quad . \qquad (1)$$

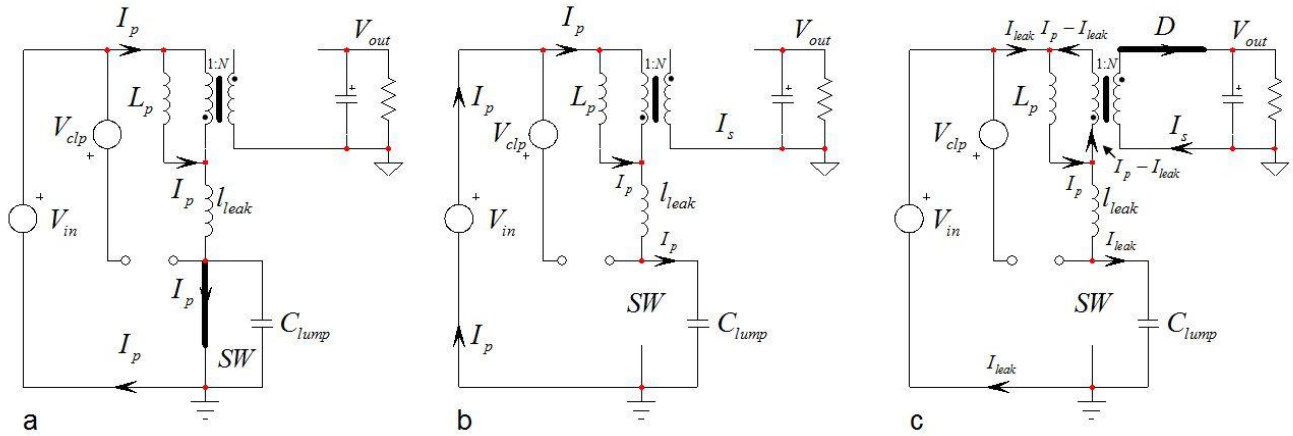

Fig. 1. The operating states of a flyback converter show energy storage in the primary side followed by energy circulation in the secondary side when the power switch opens.

During t_{on} and considering the coupling dots, the secondary-side diode is blocked. As both L_p and l_{leak} appear in series, the current $i_p(t)$ circulating in these elements increases with a slope equal to

$$S_{on} = \frac{V_{in}}{L_p + l_{leak}} . \quad (2)$$

When the controller instructs the switch to open, we jump to diagram (b). At this moment, the inductive current finds a path in the capacitance lumped at the drain node. This parasitic term represents the MOSFET's own non-linear capacitances as seen from its drain terminal, C_{rss} and C_{oss}, plus the various capacitances brought by the clamp diode, the transformer inter-windings capacitances and the output diode capacitance reflected to the primary. All these elements are lumped into a ground-referenced capacitor designated as C_{lump}. As current flows in C_{lump}, the drain-source voltage quickly increases. The slope is not constant given the MOSFET's non-linear capacitance. We can however say that the approximate slope of this voltage is given by

$$S_{drain} \approx \frac{I_{peak}}{C_{lump}} \quad (3)$$

in which I_{peak} is the current value when the switch opens. The drain voltage increases until the voltage across L_p reverses. At this moment, Fig. 1c, the secondary diode becomes biased but no current circulates in the secondary yet. As both L_p and l_{leak} are energized, l_{leak} forces a current into the lumped capacitance which continues its charge. Because of the series connection, the current in L_p and l_{leak} are equal and the net current flowing in the secondary diode is 0 A. The drain voltage at which *D* begins its conduction is equal to

$$V_{DS} \approx V_{in} + \frac{V_{out} + V_f}{N} . \quad (4)$$

The output voltage now flies back across L_p—hence the term *flyback* converter—and forces a downslope equal to

$$S_{off} = -\frac{V_{out} + V_f}{NL_p} . \quad (5)$$

The drain node continues its growth until it reaches the input voltage plus the clamp level V_{clp}. At this moment, the clamp diode conducts as shown in Fig. 2a. As the drain node voltage becomes stuck at $V_{in} + V_{clp}$, the leakage current no longer flows in C_{lump} but exclusively in V_{clp}. The charge of the lumped capacitor has absorbed energy from the leakage and primary inductances and the current now circulating in V_{clp} is slightly less than the original peak primary current.

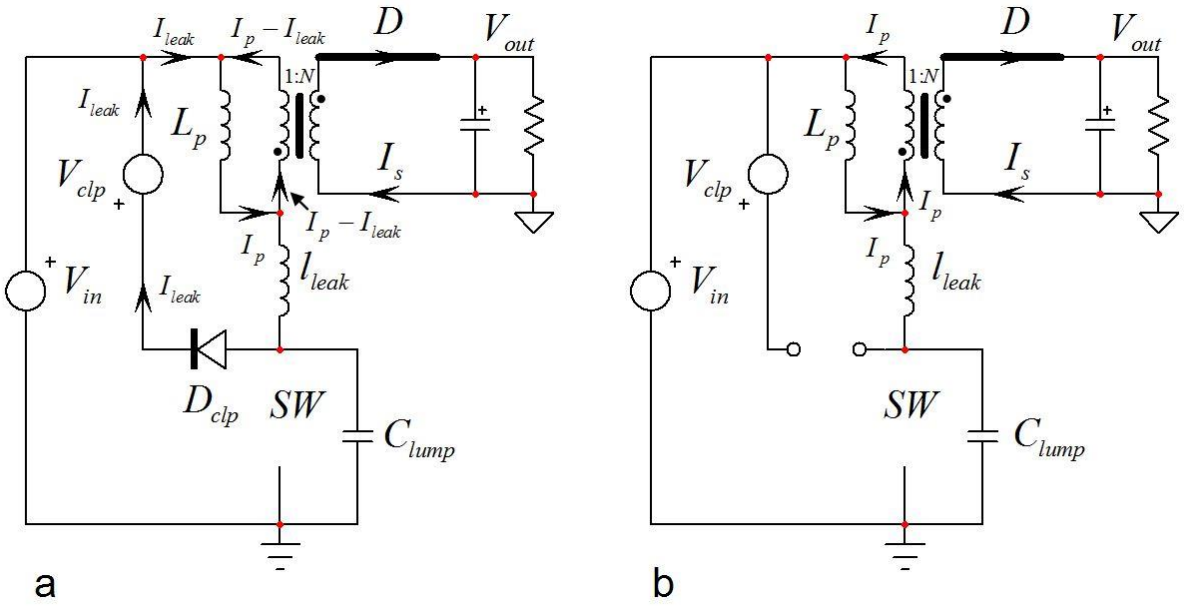

Fig. 2. The clamp diode conducts when the lumped capacitor is charged to V_{in} + V_{clp}.

When the switch opens with a peak current I_{p1}, the total energy stored in the circuit is equal to

$$W_{tot1} = \frac{1}{2}\left(L_p + l_{leak}\right) {I_{p_1}}^2 \ . \qquad (6)$$

The energy stored in the lumped capacitance when the clamp diode begins conduction equals

$$W_{C_{lump}} = \frac{1}{2} C_{lump} \left(V_{in} + V_{clp}\right)^2 . \qquad (7)$$

At this moment, the energy stored in the circuit now involves the lumped capacitance:

$$W_{tot2} = \frac{1}{2}\left(L_p + l_{leak}\right) {I_{p_2}}^2 + \frac{1}{2} C_{lump} \left(V_{in} + V_{clp}\right)^2 \qquad (8)$$

in which I_{p2} is the circulating current after charging the lumped capacitance. The quantity of energy described by equation 6 does not change except that part of it has been transferred to C_{lump}. Therefore,

$$W_{tot1} = W_{tot2} . \qquad (9)$$

Rearranging

$$\frac{1}{2}\left(L_p + l_{leak}\right) {I_{p_1}}^2 = \frac{1}{2}\left(L_p + l_{leak}\right) {I_{p_2}}^2 + \frac{1}{2} C_{lump} \left(V_{in} + V_{clp}\right)^2 . \qquad (10)$$

Solving for I_{p2} in this expression leads to

$$I_{p2} = \sqrt{I_{p1}{}^2 - \frac{C_{lump}}{l_{leak} + L_p}\left(V_{in} + V_{clp}\right)^2}\ . \qquad (11)$$

Assuming the following values

$$l_{leak} = 12\ \mu\text{H}\ \ L_p = 600\ \mu\text{H}\ \ I_p = 1\ \text{A}\ C_{lump} = 150\ \text{pF}$$
$$V_{out} = 19\ \text{V}\ \ V_f = 1\ \text{V}\ \ N = 0.25\ \ V_{in} = 330\ \text{V}\ \ V_{clp} = 110\ \text{V}$$

then equation 11 returns a current of approximately 976 mA or a reduction of 2.4% compared to the original 1-A peak current at the switch opening. Please note that C_{lump} is a highly nonlinear term, especially at low voltages when the switch opens. While equation 11 is an approximate theoretical formula, bench experiments confirm the lower current circulating in the clamping network when diode D_{clp} starts conducting.

Increasing the capacitance on the drain with an additional 100-pF capacitor (1 kV for offline applications) will reduce that current further. This extra capacitor helps the *RCD* clamp temperature and benefits the turn-off losses by snubbing the drain voltage. EMI will also be improved by reducing the dV/dt on that node. However, adding that capacitor can potentially increase the high-line turn-on losses if the operating frequency is high. So, a tradeoff must be found here.

At this point, the leakage inductance voltage is fixed (neglecting ripple): the lower terminal is stuck at V_{in} + V_{clp} (neglecting the clamp diode drop) while its upper terminal is equal to

$$V_{in} + \frac{V_{out} + V_f}{N}\ .$$

The voltage applied across the leakage inductance is thus

$$V_{clp} - \left(V_{out} + V_f\right)\Big/ N\ .$$

The reset time of the leakage inductance begins here. The current defined in equation 11 drops with a slope equal to

$$S_{off,l_{leak}} = -\frac{V_{clp} - \dfrac{V_{out} + V_f}{N}}{l_{leak}}\ . \qquad (12)$$

As the leakage inductance resets, current in the secondary-side diode $i_d(t)$ builds up at a slope defined by equation 12 but positive this time and scaled by the turns ratio. When the leakage inductance is fully depleted, the current in the output diode is at its peak (Fig. 2b). The secondary current now goes down at a slope defined by equation 5. This downslope lasts until the switch is turned on again. This is the off-time denoted as t_{off}.

However, the current in the output diode cannot instantaneously return to zero. And the reason is the time needed to energize the leakage inductance: its current must jump to that of the primary inductance still coupled to the secondary. This is the time during which the switch current grows from zero to the valley current I_v. When $I_{SW} = I_v$, all the primary current now flows in the power switch and the secondary-side diode is blocked. Two important comments can be inferred from this information.

First, the secondary-side diode keeps conducting for a time t_1 when the switch turns on. It is the time for the leakage current to grow from zero to the valley current I_v. As the output diode still conducts during this short

period of time, L_p keeps demagnetizing: the leakage inductance extends the secondary-diode conduction time by d_1T_{SW}. Despite the switch closure, the slope change in the primary inductance does not occur before the current in the leakage inductance reaches the valley current and diverts the entire flow to ground: the duty ratio D is reduced by d_1.

Secondly, when the switch SW opens, the secondary-diode net current in the secondary is zero as all the primary current is diverted to charging C_{lump}. As the leakage inductance resets, the secondary current builds up and reaches its peak when reset is complete: the leakage inductance delays the occurrence of the secondary current by the time t_2 and affects its peak value. The energy stored in the leakage inductance plus the extra energy stolen from the primary inductance are dissipated in the clamping network.

A close-up of this process appears in Fig. 3. As you can see, the delaying action of the leakage inductance is clear and prevents the secondary current from immediately reaching its peak. Furthermore, this peak current is not I_{peak}/N but as shown in the reference is equal to

$$I_{d,peak} = \frac{I_{peak}}{N}\left(1-\frac{l_{leak}}{L_p}\frac{1}{\frac{NV_{clp}}{V_{out}+V_f}-1}\right). \qquad (13)$$

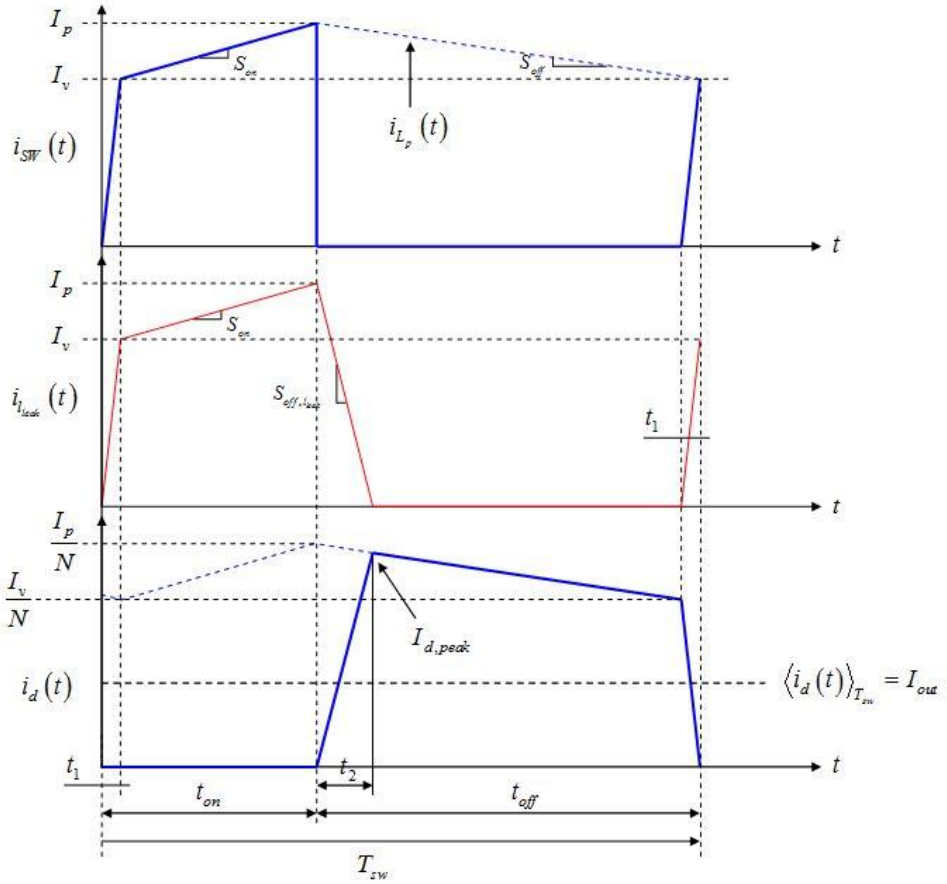

Fig. 3. The secondary-side current, i_d, peaks when the leakage inductance is depleted.

Updating The DC Transfer Function

Now that we have a better understanding of what is going on during the transitions, let's compute the small time periods we have referred to as t_1 and t_2. The first term, t_1, is the time needed to energize the leakage inductance from zero to the valley current I_v. When SW closes, the voltage applied across the leakage inductance is the reflected output voltage (diode *D* still conducts) in series with the input voltage V_{in}. Neglecting the secondary-side diode forward drop V_f, the time t_1 is thus defined as:

$$t_1 = \frac{I_v l_{leak}}{V_{in} + \frac{V_{out}}{N}} . \quad (14)$$

If we normalize it to the switching period, we obtain a duty ratio d_1 equal to

$$d_1 = \frac{I_v l_{leak}}{\left(V_{in} + \frac{V_{out}}{N}\right) T_{sw}} . \quad (15)$$

The leakage inductance reset time t_2 is determined in a similar manner. The voltage applied across the leakage term when the switch opens (neglecting the lumped capacitor charging time) is the clamping level V_{clp} minus the reflected voltage since *D* began conducting. We thus have

$$t_2 = \frac{I_p l_{leak}}{V_{clp} - \frac{V_{out}}{N}} . \quad (16)$$

Once normalized to the switching period, we obtain a duty ratio d_2 equal to

$$d_2 = \frac{I_p l_{leak}}{\left(V_{clp} - \frac{V_{out}}{N}\right) T_{sw}} . \quad (17)$$

To determine the output voltage of a converter, a good tool is the inductor volt-second balance law, which states that the average voltage across an inductor *L* at steady-state is zero:

$$\left\langle v_L(t) \right\rangle_{T_{sw}} = 0 . \quad (18)$$

The voltage across the primary inductance follows the graph shown in Fig. 4. To satisfy equation 18, we can write the following equation

$$\left\langle v_{L_p}(t) \right\rangle_{T_{sw}} = V_{in} \frac{L_p}{L_p + l_{leak}} (D - d_1) - \frac{V_{out}}{N} (1 - D + d_1) = 0 . \quad (19)$$

Solving for V_{out} in the above expression and rearranging leads to

$$\frac{V_{out}}{V_{in}} = \frac{(D-d_1)L_pN}{(1-D+d_1)(L_p+l_{leak})} = \frac{D-d_1}{1-D+d_1}N\frac{L_p}{L_p+l_{leak}} \quad (20)$$

which simplifies to

$$\frac{V_{out}}{V_{in}} = \frac{ND}{1-D} \quad (21)$$

when the leakage inductance is zero.

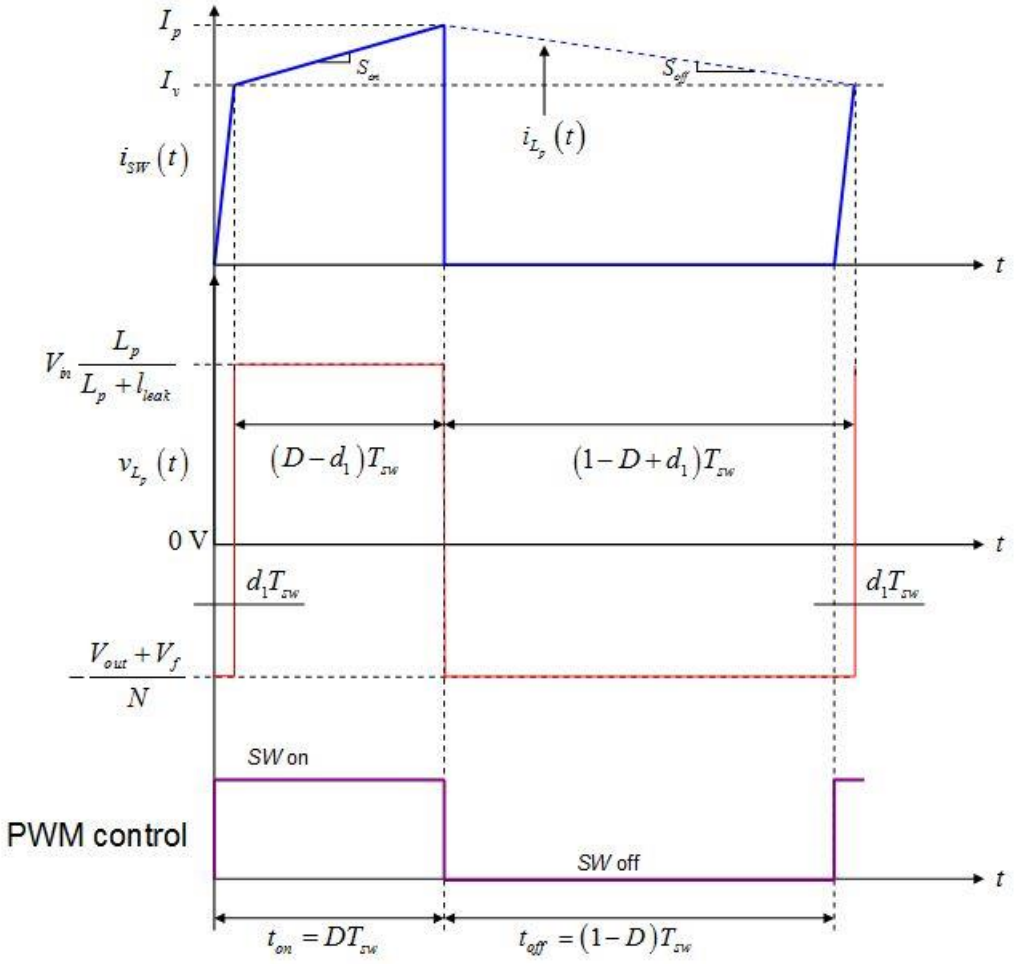

Fig. 4. The average voltage across the primary inductance is 0 V at steady state.

What is interesting to observe is the fact that the effective on-time—the time during which the primary inductance slope is positive—is actually DT_{sw} reduced by d_1T_{SW}. This effective duty ratio further shrinks as the leakage inductance increases. The voltage applied across the primary inductance is also not V_{in} but less as expressed by equation 1.

A Simple Cycle-By-Cycle Model

To test our calculations and waveforms, we have captured a simple flyback converter operating at a 40% duty ratio and delivering slightly more than 60 W. A SPICE model of this circuit appears in Fig. 5 with the simulation results for this circuit shown in Fig. 6. The leakage inductance has been set to 50 µH, illustrating a badly-coupled transformer if you consider a 600-µH primary inductance (8.3%).

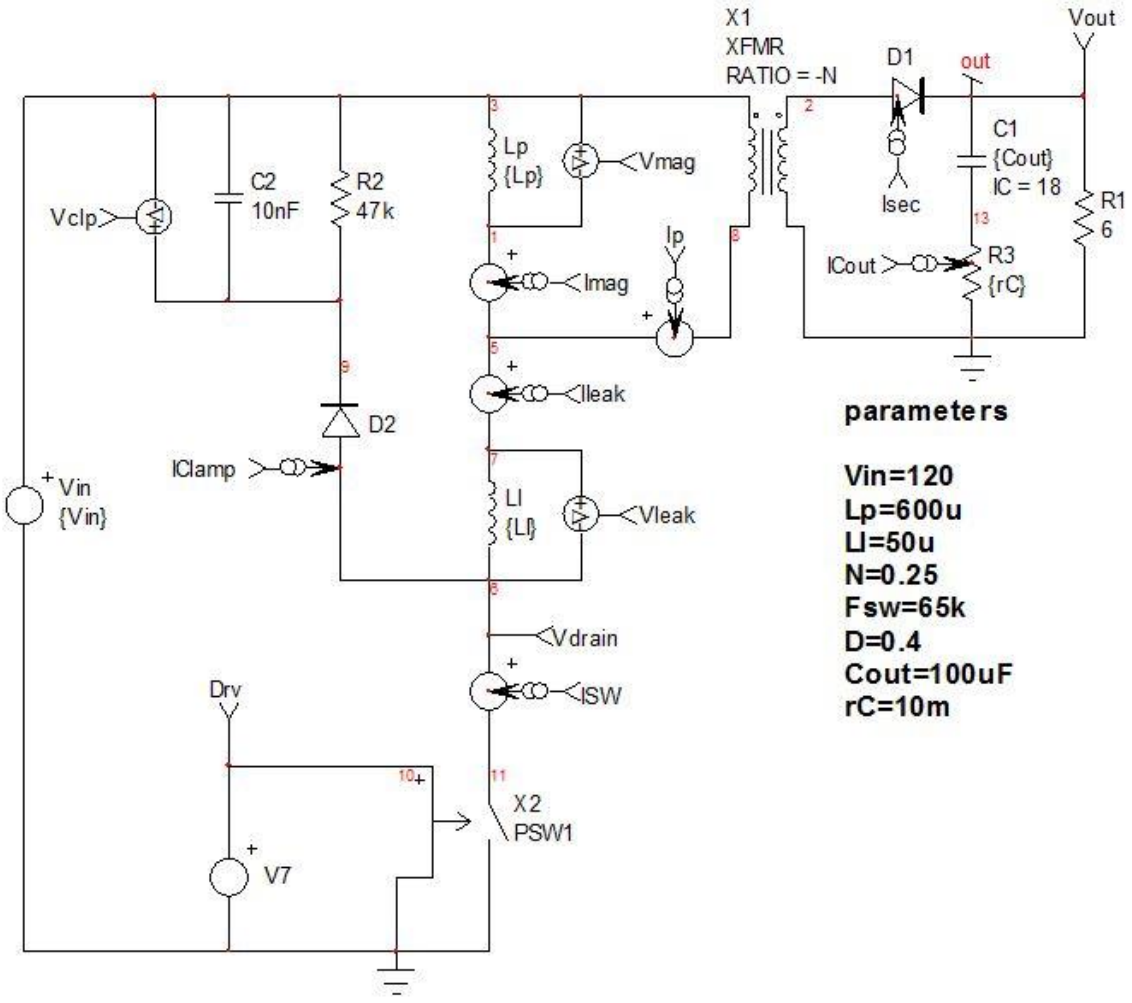

Fig. 5. This simple model helps simulate a flyback converter and reveals its basic waveforms.

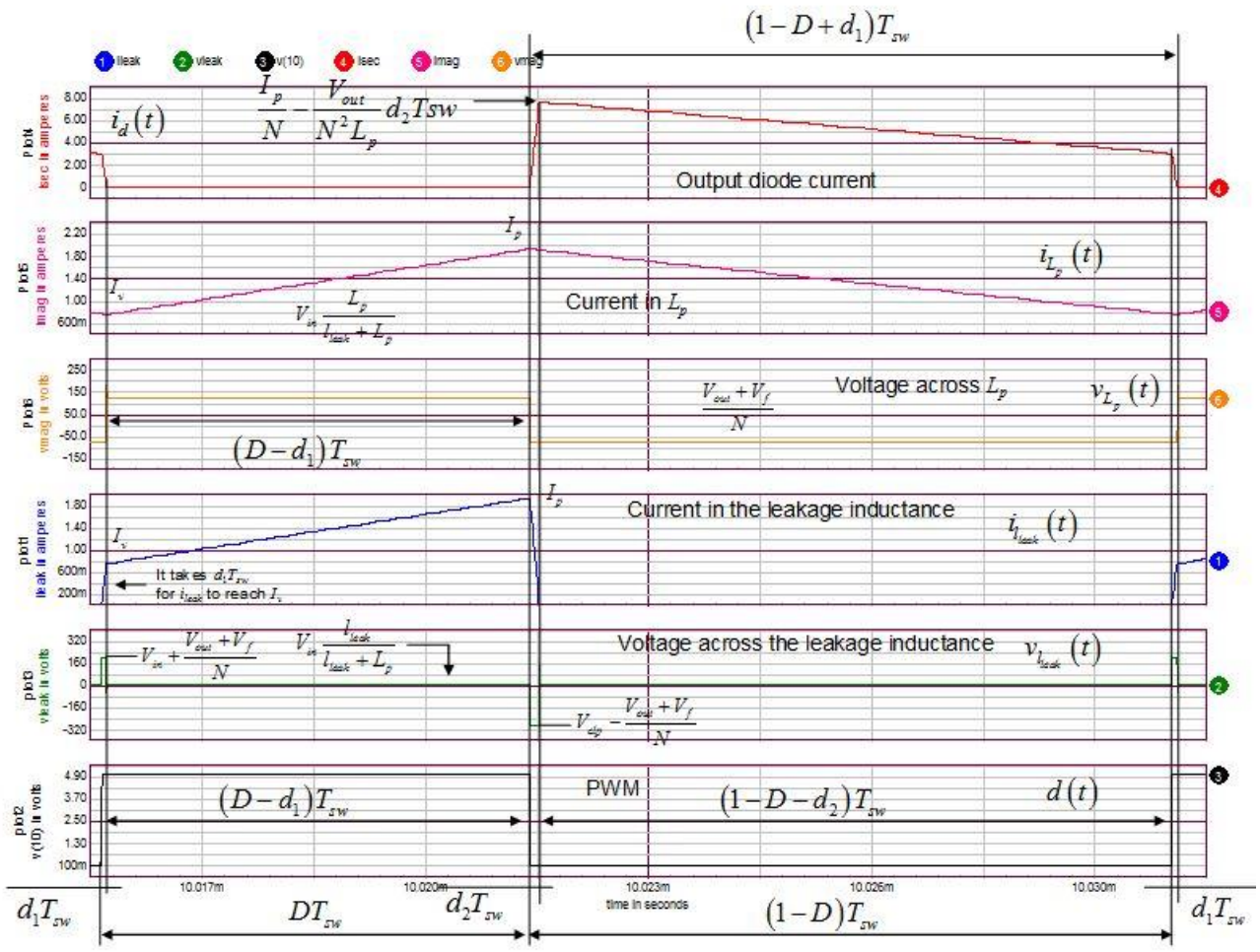

Fig. 6. These waveforms show all the events we have described in the previous discussion.

From the Fig. 6 simulation, we can extract the following operating points in which V_{clp} is the voltage across C_2:

$$I_p = 1.77 \text{ A}$$
$$I_v = 672 \text{ mA}$$
$$V_{clp} = 528 \text{ V}$$

The leakage inductance magnetizing time as described by equation 14 is measured at 176 ns (from the waveforms in Fig. 6). With a 65-kHz switching frequency, the d_1 duty ratio is thus

$$d_1 = 176n \times 65k = 1.14\% . \quad (22)$$

Theoretically, with a transformer turns ratio N of 0.25, the output voltage of this flyback converter is equal to 20 V as defined by equation 21. If we apply equation 20 instead, the output voltage should actually be equal to

$$V_{out} = \frac{0.4 - 0.0114}{1 - 0.4 + 0.0114} \times 0.25 \times 120 \times \frac{600u}{600u + 50u} \approx 17.6 \text{ V} \quad . \tag{23}$$

The simulated output voltage appears in Fig. 7 and confirms this value. Please note that the diode we used in simulation has a forward drop equal to 0 V. You obtain this result by setting the diffusion parameter *N* to 10 m in the diode model.

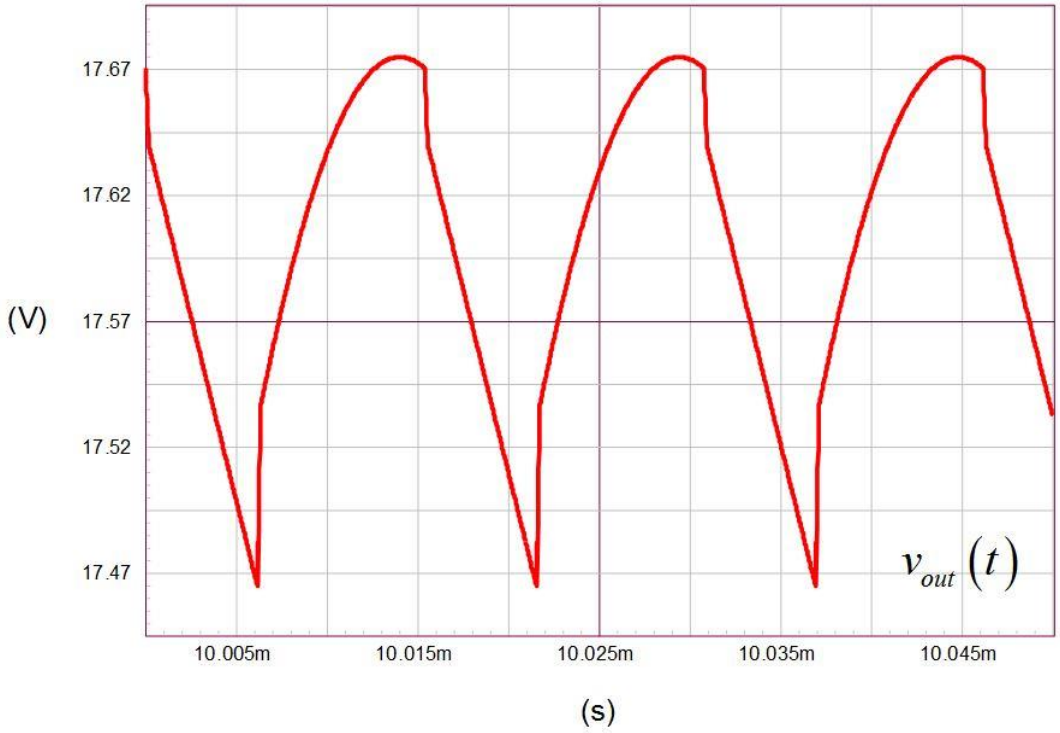

Fig. 7. Simulated output voltage for the flyback circuit in Fig 5.

The output current can also be precisely calculated knowing the leakage inductance reset time. Simulations give a valley current of 672 mA while the peak is 1.77 A. Applying equation 16 and considering a 528-V clamp voltage (the voltage across C_2 in Fig. 5), the leakage inductance reset time is equal to

$$t_2 = \frac{1.77 \times 50u}{528 - \frac{17.57}{0.25}} = 193 \text{ ns} \tag{24}$$

and corresponds to a duty ratio of

$$d_2 = 193n \times 65k = 1.26\% \, . \tag{25}$$

We can also estimate the secondary peak current when the leakage inductance is reset, 193 ns after the switch has turned off. Applying equation 13, we find

$$I_{d,peak} = \frac{1.77}{0.25}\left(1 - \frac{50u}{600u}\frac{1}{\frac{0.25\times 528}{17.57} - 1}\right) \approx 7\ \text{A}\ . \qquad (26)$$

From the Fig. 3 bottom waveform, we can now determine the average current circulating in the diode and in the load by calculating the various areas under the $i_d(t)$ curve:

$$\left\langle i_d(t)\right\rangle_{T_{sw}} = \frac{1}{2} I_{d,peak} d_2 + \frac{I_{d,peak} + \frac{I_v}{N}}{2}(1 - D - d_2) + \frac{1}{2}\frac{I_v}{N} d_1\ . \qquad (27)$$

Applying numerical values, we have

$$\left\langle i_d(t)\right\rangle_{T_{sw}} = 0.5\times 7\times 0.0126 + \frac{7 + \frac{0.672}{0.25}}{2}(1 - 0.4 - 0.0126) + 0.5\times\frac{0.672}{0.25}\times 0.0114 = 2.9\ \text{A}\ . \qquad (28)$$

This is the value given by the waveform viewer as shown in Fig. 8.

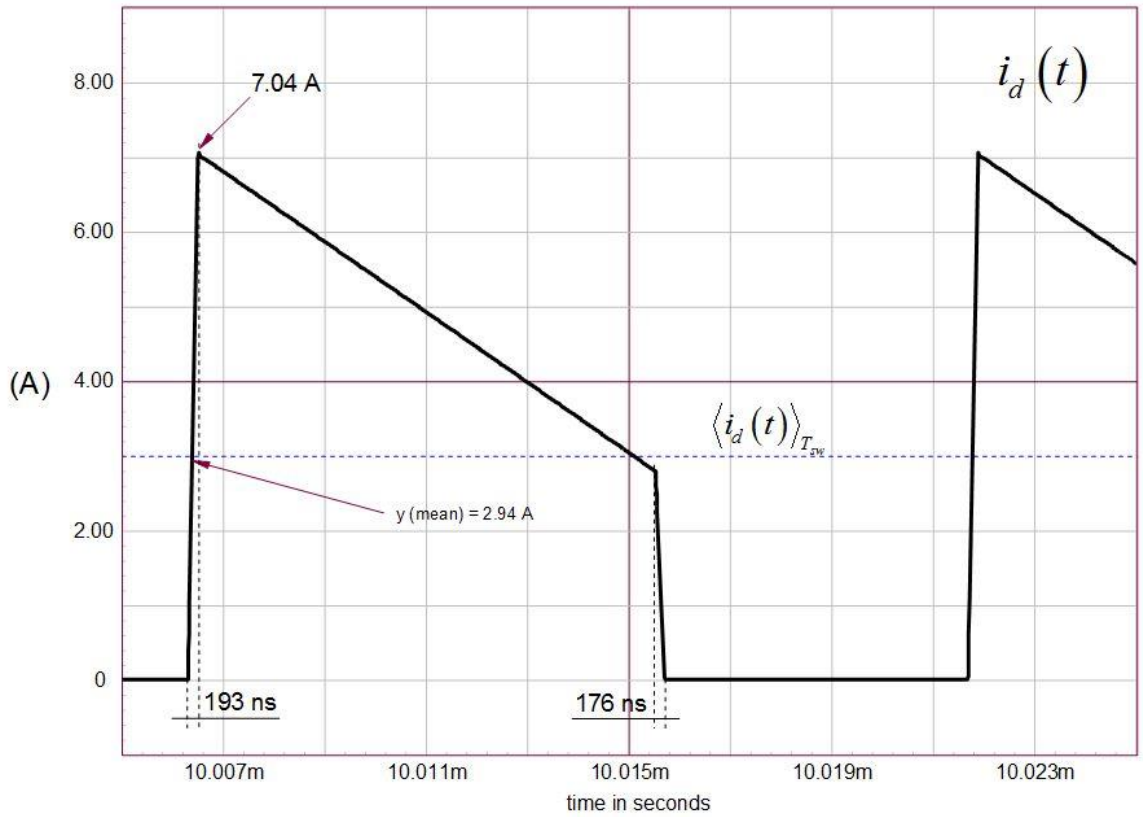

Fig. 8. The simulated secondary-side average current depends on the peak value but also on the various small duty ratios d_1 and d_2.

Hardware Verification

To confirm our analysis, we have built a simple fixed-duty ratio flyback converter whose leakage inductance has been artificially grown to 2.5% of the primary inductance by adding an external inductor. Fig. 9 shows the voltage on the MOSFET drain and the current in the secondary-side diode. As expected, the current does not instantaneously increase in the secondary when the switch opens. This is the delay brought by the leakage inductance demagnetization time.

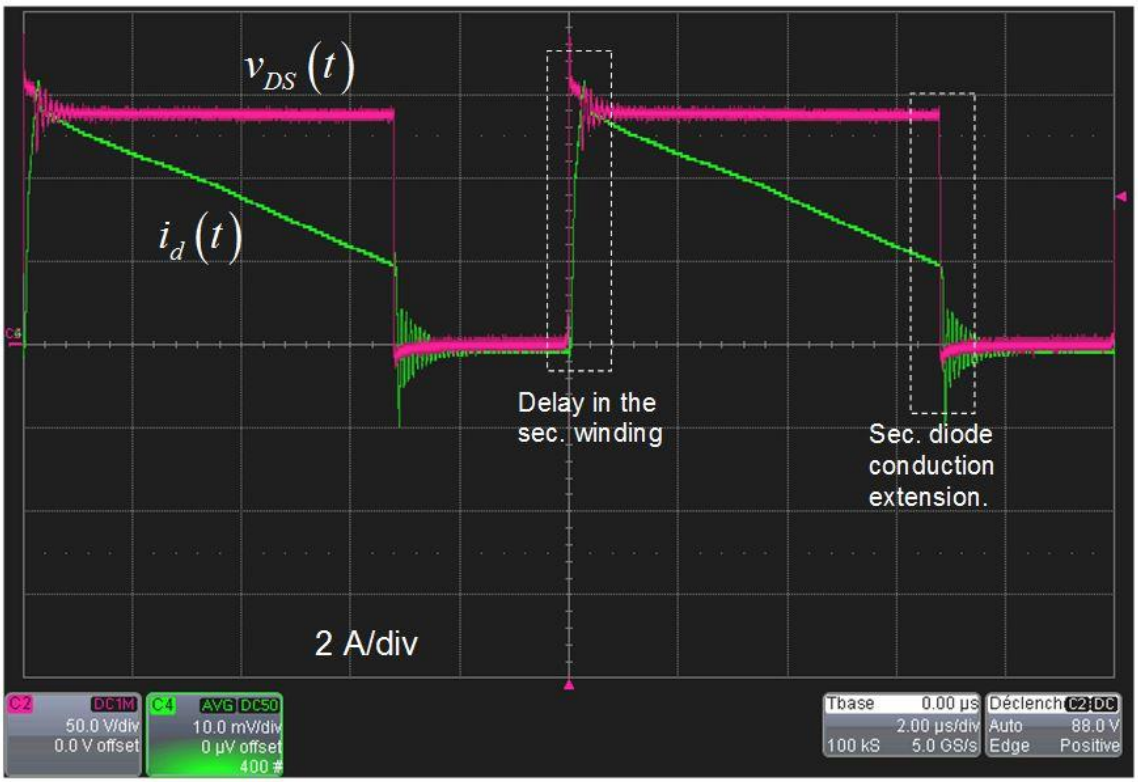

Fig. 9. Waveforms obtained from the flyback converter prototype show the delay in the secondary side but also the small extension in the conduction time of the secondary diode. This extension in conduction time is easier to observe in the Fig. 10 close-up.

On the right side of the oscilloscope image, you see that the diode waveform is slightly behind the drain voltage going down sharply. This is the leakage inductance magnetization time from 0 to the valley current. The close-up of Fig. 10 confirms a 62-ns conduction time.

The MOSFET turn-on event is well synchronized with the falling of $v_{DS}(t)$, but the magnetization cycle for L_p truly begins 62 ns later. During these 62 ns, L_p keeps demagnetizing despite the fact that the MOSFET has been turned on. This phenomenon is quite short here and can obviously be neglected. However, you can clearly observe the delay, which will get significantly longer with an active-clamp architecture.

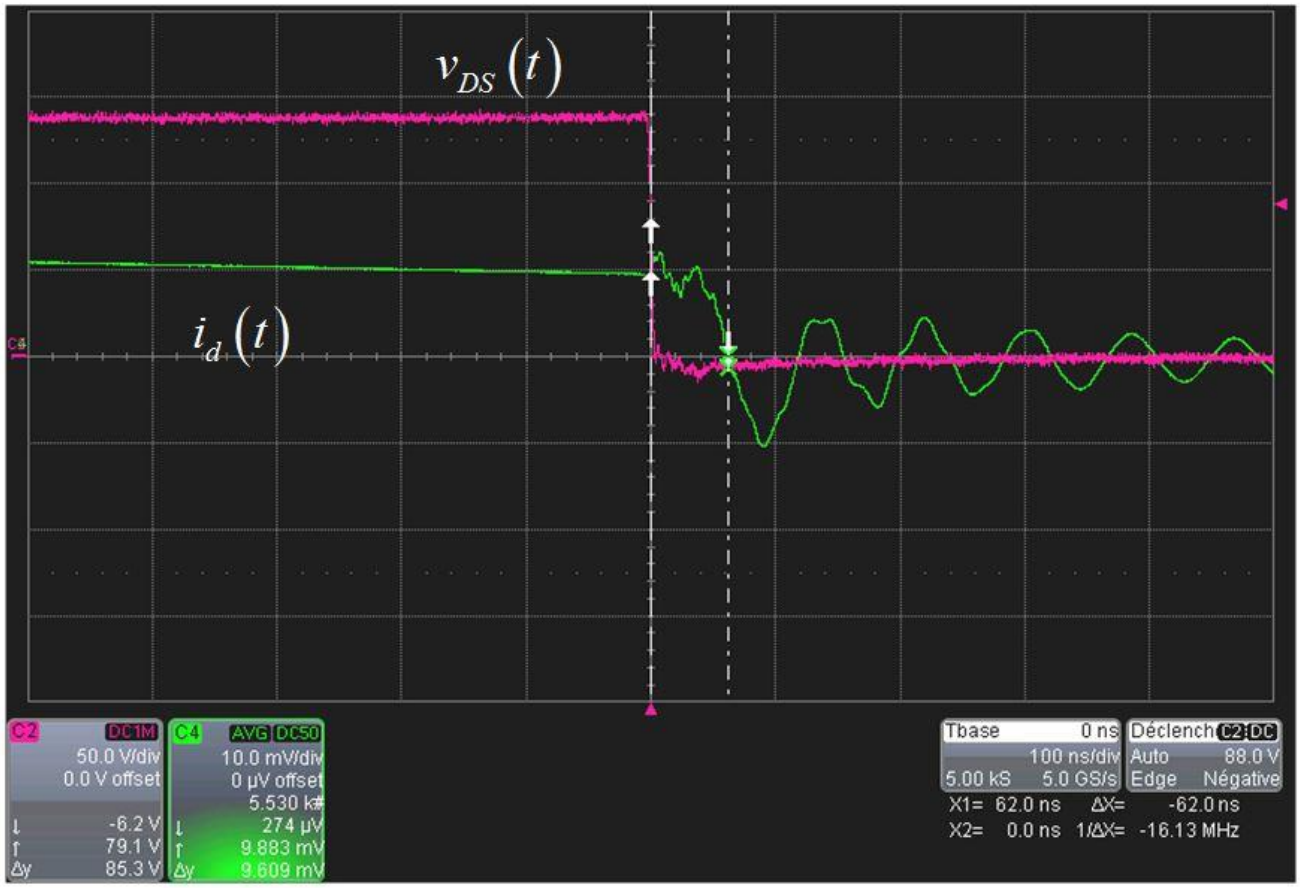

Fig. 10. A close-up of the falling edge shows an extended duration of 62 ns for the secondary-side diode.

In Fig. 11, you can clearly see the delay in the secondary-side current but you can also evaluate the leakage inductance reset time. It is the time during which the drain voltage plateaus after the switch opening event. This event lasts 217 ns in this example. The overshoot can be quite significant and depends on the clamp diode forward transit time. It must be accounted for when assessing the worst-case margin you have on the MOSFET BV_{DSS}.

When the *RCD* diode blocks, a high-frequency ringing involving the leakage inductance and C_{lump} occurs. It is sometimes necessary to damp these oscillations as they can severely radiate and affect the EMI signature. Make sure the loop involving the *RCD* clamp is extremely short and kept close to the transformer. A series resistance with the diode of a few tens of ohms helps to damp these oscillations.

In the Fig. 11 oscilloscope shot, the delay lasts a short period of time as the leakage inductance is quickly reset. In an active-clamp converter, however, a resonance involving l_{leak} and C_{clamp} occurs at turn-off, naturally expanding the reset along the off-time. This resonance induces a smooth discontinuous waveform in the secondary despite a CCM operation.

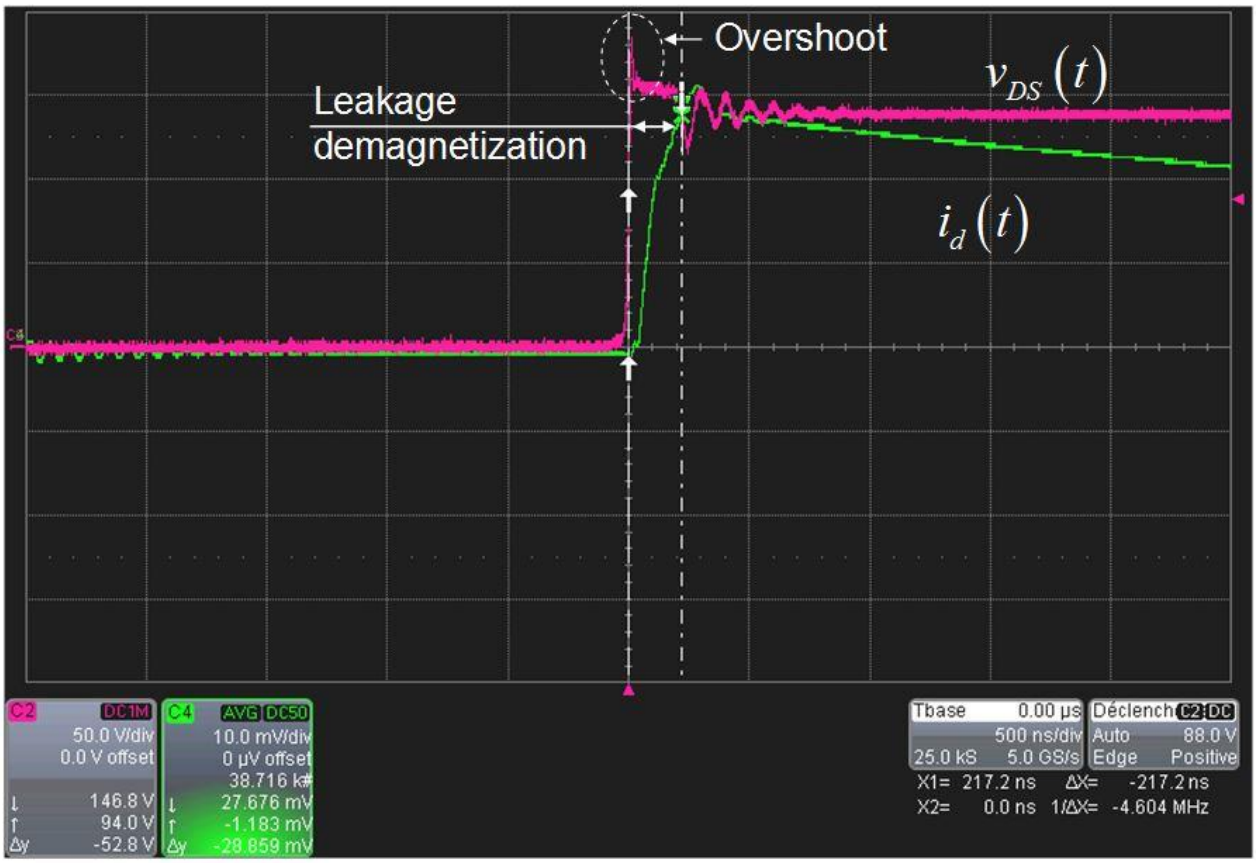

Fig. 11. Observing the drain voltage reveals interesting information, in particular the leakage inductance reset time.

Conclusion

This first part shows how flyback converter waveforms are affected by the leakage inductance. The effective duty ratio is reduced by the time needed to energize the leakage inductance while the demagnetization time of the primary inductance is extended by the same amount. The dc transfer function is affected and a new expression has been derived. These events are small in a flyback converter and can be difficult to visualize with a well-coupled transformer. However, in an active-clamp converter, they can be of significant duration. Our next part will focus on the small-signal effects brought by the leakage inductance.

Reference

"Switch Mode Power Supplies: SPICE Simulations and Practical Designs", second edition by Christophe Basso, McGraw-Hill 2014, ISBN 978-0071823463.

About The Author

Christophe Basso is a technical fellow at ON Semiconductor in Toulouse, France. He has originated numerous integrated circuits among which the NCP120X series has set new standards for low standby power converters. SPICE simulation is also one of his favorite subjects and he has authored two books on the subject. Christophe's latest work is "Designing Control Loops for Linear and Switching Power Supplies: A Tutorial Guide."

Christophe received a BSEE-equivalent from the Montpellier University, France and an MSEE from the Institut National Polytechnique de Toulouse, France. He holds 18 patents on power conversion and often publishes papers in conferences and trade magazines.

For further reading on leakage inductance, see the How2Power Design Guide and enter "leakage inductance" in the keyword search. And for more on magnetics design in general, see the Design Guide, locate the "Design Area" category, and click on the "Magnetics" link.