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Misconceptions About GaN Create Barriers To Better Power Performance

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You've heard about GaN transistors' superior performance, and you are excited. The samples finally arrive, and you put them onto your board. You turn on the power, you bring up the load, and you see… no better performance than before. Worse, you have switching problems that didn't previously exist. These transistors are no good. What a sham. What is all the buzz about? Is it possible you are missing something?

For more than two decades, silicon power MOSFETs have dominated as the switch in switching power supplies. In these applications, high speed and reduced power loss versus frequency could not be achieved as well using the previous technology, bipolar transistors. Over time, power MOSFETs have improved, creeping closer to the performance of an ideal switch.

Yet, non-ideal characteristics unique to these transistors must still be comprehended if the end application is to fully benefit from their advantages. As the switching speed of power MOSFETs has increased with advances in silicon technology, circuit designers have been forced to make more conscious decisions about component placement and printed circuit board layout to improve efficiency while managing parasitic elements to keep noise and interference under control.

GaN transistors represent the next step in the progression toward an ideal switch, and in several respects offer a leap in performance rather than just another small step. Traditional challenges to component placement and control of parasitic elements follow the same principles as before but are now even more pronounced. The baseline requirements for board layout have therefore shifted, requiring tighter drive and power loop designs than were necessary with slower power MOSFETs.

In this respect, customers who attempt to place a GaN power transistor into an existing circuit designed for silicon power MOSFETs are often disappointed that they run into problems or at the very least, do not see the improvement in performance they expected. To obtain the full benefit from the implementation of a GaN transistor, it is necessary to design the system around it, rather than treating the system switch as an afterthought. This activity builds on the assumption that the designer has selected a circuit topology and a control methodology that will utilize the advantages of the GaN transistor.

Some of the key differences between GaN power transistors and silicon power MOSFETs are shown in the table. As the table illustrates, the GaN device has much lower gate charge, and radically lower reverse-recovery charge. In addition to these things, the output capacitance characteristic is flatter versus drain-source voltage and results in superior output capacitance charge compared with the silicon device. These differences lead to different behavior in the GaN device. Lower gate charge means the same driver IC can be used with lower drive loss. But, does this really offer a significant benefit?

Table. Comparing a first-generation GaN device with a recent-generation silicon MOSFET.

600-V Transistor	On-resistance (mΩ)	Gate charge, Q_G (nC)	Output Capacitance, C_O (nF)	Output charge, Q_{OSS} (nC)	Reverse recovery charge, Q_{RR} (nC)
Gen 1 GaN cascade	180	18	116	47	38
State-of-the-art silicon MOSFET	195	23	321	131	5800

Rather than placing the transistor into an existing situation, the best approach is to look at the system benefits GaN can enable. With lower drive loss, the switching frequency can be increased without adding to the drive portion of power dissipation, per the following equation:

$$P_{DRIVE} = Q_G * V_{GS} * f_{SW}$$

where Q_G = gate charge, V_{GS} = applied gate-source voltage, and f_{SW} = switching frequency.

Increasing the switching frequency allows use of smaller magnetic components in the circuit. Depending on circuit type and system requirements, it might also mean an opportunity for reduced bulk capacitor size. These changes lead to a saving of space that enables higher power density.

Other aspects must be considered to ensure an improvement in power density is viable. During each switching cycle, energy is stored on the output capacitance of the transistor, which must be removed for the device to operate with low resistance when switched on. If the switching circuit is operated in a way that will recycle this energy, there is no penalty with increased switching frequency. Otherwise, it is important to comprehend the switching loss at the output of the transistor, which will also be proportional to frequency.

With reduced system size, heat conduction paths must be checked to ensure proper handling of remaining power dissipation so that component and system temperature requirements are not violated over operating conditions. With the same power dissipation and higher power density, system thermal resistance must be the same to keep component operating temperatures similar to the less dense case. To have the same system thermal resistance in a smaller volume may require a different design or more thermally conductive materials.

Another misconception about GaN transistors is one that carried over from power MOSFETs. When power MOSFETs first arrived on the market, they had very limited energy capability when an overvoltage event forced full system current through the device in the off-state. It took many years to engineer improvements to the device allowing it to survive overvoltage events. Yet, but before this happened designers continued to use power MOSFETs due to other system performance advantages.

A similar situation exists with today's first-generation GaN power transistors. They should not be relied on to shunt a high energy excursion from the system. In fact, even with silicon power MOSFETs, the perception is that the avalanche energy on the datasheet indicates sufficient protection for a device in the customer's application. This has given customers a false sense of security. In reality, the rated avalanche energy most often does not reflect the device capability in the customer's usage conditions.

Similarly, with GaN transistors, care must be taken to limit exposure to line surges and other events that can flood the system with extra energy and cause high-voltage excursions. However, in this respect, today's GaN transistors have an advantage over silicon MOSFETs. The actual breakdown voltage is well above the rated steady-state voltage, meaning that transient voltages can go much higher before the device is destroyed. Careful design would not only include transient surge suppressors in the system, but also a consideration of the energy required to raise the drain-source voltage of the GaN transistor, taking into account the system capacitance to ground.

One of the main advantages of GaN transistors is their switching speed. However, without considering system aspects to take advantage of this performance, the benefits of GaN may not be realized. With the fast edge rates enabled by GaN transistors, system designers can significantly increase switching frequencies. While parasitic inductances have always had an impact on switching circuits, they become much more critical as edge rates and switching frequency rise.

Faster edge rates contain more high-frequency harmonic content, increasing risk of propagation as either conducted or radiated electromagnetic interference (EMI). Filters for conducted EMI must be properly tuned for the combination of power transistor and surrounding circuit, rather than relying on an existing design in the false belief that it is adequate. To mitigate radiated EMI, switching nodes must be kept as short and wide as possible.

While parasitic inductances in packaging of fast switching transistors have been documented to have a significant effect on power conversion efficiency, PCB layout is just as critical. Total inductances within power and drive loops must be minimized to have the best control of device switching performance. Examples of these inductances are shown in the figure.

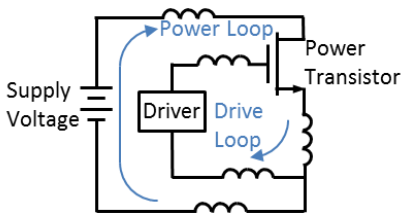

Figure. Parasitic inductances in power and drive current loops for a power transistor.

With minimized parasitic inductances enabling faster switching frequencies, other components can be reviewed for modification. At higher switching frequency, it is generally possible to reduce the size of magnetic cores in transformers or inductors, helping to increase system power density. If the same materials and method of manufacture can be used as with the larger versions, magnetic components will cost less.

Capacitance requirements in the system may also be reduced if system requirements can still be met, but this is far from a foregone conclusion. For instance, there may be a hold-up time requirement, which in turn requires a minimum capacitance.

Reducing parasitic inductances to their minimums and designing around them allows shorter and more controlled switching events. This allows the full benefit of fast switching GaN transistors to be seen in end application efficiency.

GaN power transistors bring the promise of allowing customers to push their designs beyond the limits of silicon. The system switch is no longer the limiting factor in power conversion, and other circuit considerations must be made to enable more-efficient, compact designs. It is important to consider circuit layout and component selection to push system performance beyond the state of the art. After all, GaN is not a drop-in replacement for silicon. It is a new paradigm.

Reference

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For further technical news and design information relating to GaN power devices, see How2Power.com's section on Silicon Carbide and Gallium Nitride Power Technology.