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This Misconception About Power Integrity Can Cost You Big

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Many power supply engineers mistakenly believe that power integrity (PI) is mainly a system-level issue and not a concern for the power supply design. But the reality is very different. If you're developing power solutions while working under this misconception, the problems can be both hard to find and intractable to fix. When power integrity problems occur, they can cost your company big bucks and significant schedule delays.

Ignoring PI issues when developing voltage regulators or when designing them into systems can lead to malfunctioning designs, time consuming design iterations and board spins to fix problems, stoppages in production, use of "band-aids" that add extra components to solve PI problems, and other undesirable and costly scenarios. If you're on the chip development side of the fence, PI issues discovered too late could lead to scrapping of wafers and the need to create new wafer masks, which become very costly.

These problems can be avoided if designers of voltage regulators, designers of the power distribution networks (PDNs) that carry the power and designers of the circuits that use the power take time to consider the impact that these power generating circuits will have on PI in the intended applications.

Now if you're a designer of board-level power converters, either at a power IC company or a power module manufacturer, you might be wondering, "How can I account for all the different application scenarios that my products might see?" The truth is you can't. But recognize that, just like in larger systems, the impedances must be defined on both sides of the interface.

An Analogy

The misconception that PI doesn't concern designers of board-level power solutions is analogous to believing that high speed and microwave engineers don't need to worry about impedance matching as that's a system-level issue. In the case of RF, most circuits maintain a 50 Ω impedance. The source is 50 Ω, the load is 50 Ω and the interconnecting printed circuit boards and cables are 50 Ω. The impedance matching is well understood and designers of each circuit stage plan for this in their design.

The PCB designer also assures that the traces maintain the 50 Ω impedance necessary to match the source and load circuits. The same is true of high-speed differential transceivers, though the impedance levels tend to be higher, often 100 Ω. While power systems are not nearly so well defined, the same considerations are warranted.

What Is PI?

Power integrity (PI) is the assurance that *appropriate* power is delivered to the circuits within the system. Appropriate is dependent on what is being powered. For example, low-noise microwave amplifiers (LNAs), low-jitter clocks and analog sensors can be sensitive to microvolts of power supply ripple and noise. These requirements for PI are quite different from those of high-speed transceivers and FPGAs, which must maintain certain operating voltage levels over wide bandwidths, despite very large operating current transients.

Therefore, good PI is the assurance that these various power quality requirements are met at each circuit throughout the system. It's easy to see then why it might be incorrectly perceived as a system-level issue. But the fact remains it is not a system-level issue. The power supply plays a very large role in PI, in conjunction with the PDN and load. Overcoming an unsuitable power supply design may be expensive at best and insurmountable at worst.

What Is The PDN

The power system is comprised of power converters, printed circuit board planes and decoupling capacitors. Collectively, these represent the power distribution (or delivery) network (PDN) as seen in Fig. 1. These individual elements interact with each other and achieving sufficient PI requires them to be properly balanced. In Fig. 1, the power converter is a VRM, but it could be any switching or linear regulator.

Fig. 1. The power distribution network (PDN) is comprised of the VRM, planes and decoupling capacitors.

The characteristics of the power converter have a significant impact on PI and, counterintuitively, a power converter that is "too good" regulation-wise can destroy the PDN balance, resulting in significantly degraded PI. This is because the output impedance of a regulator whose regulation is too good (i.e. too low), may be incompatible with the rest of the PDN path and load impedance. The performance can be unfixable without a circuit change and subsequent board spin.

The Power Converter's Contribution To PI

For an example of a power converter that's too good, we turn to the Picotest VRTS3 test and measurement training board. The section of the board shown in Fig. 2 includes a linear regulator with a selection of output capacitors (U301 and C301-C304), a printed circuit board trace and a 10 nF local decoupling capacitor, C402. The resulting power is applied to a 125 MHz clock (OSC401).

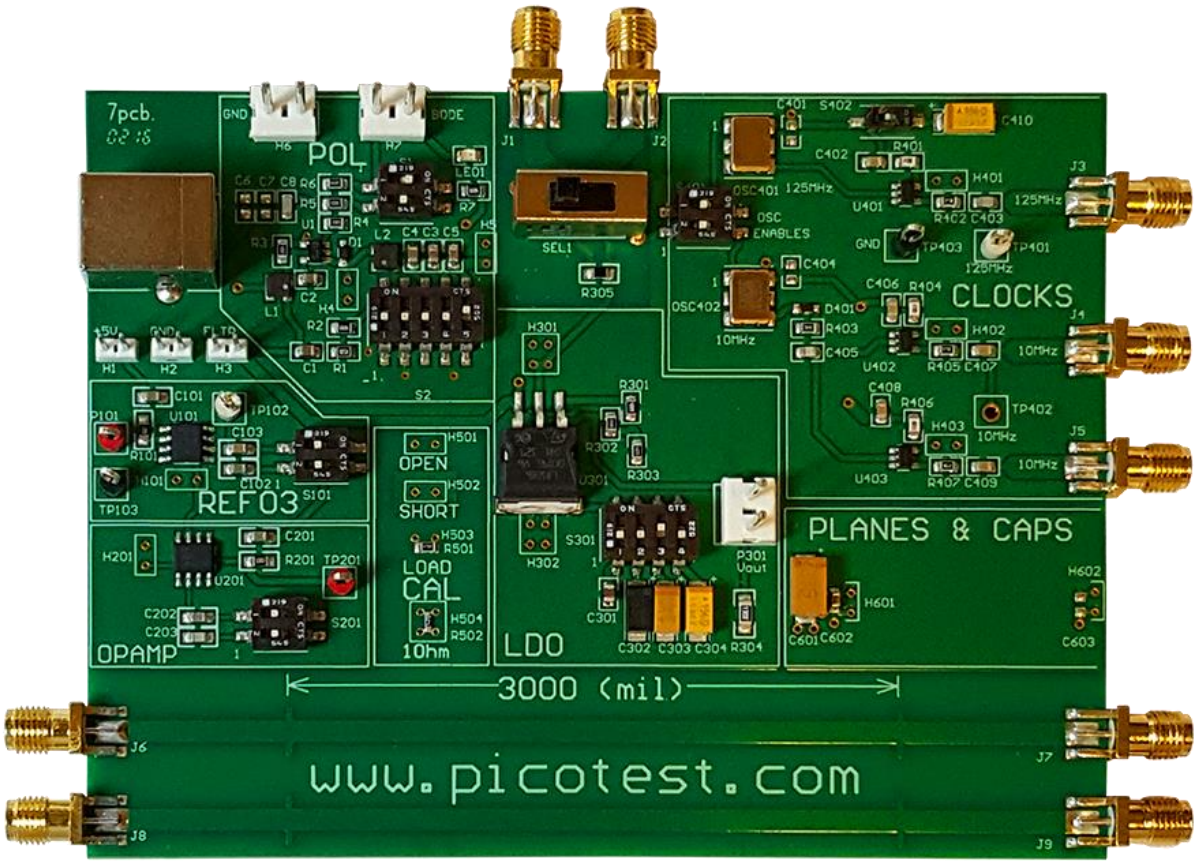


Fig. 2. A section of the Picotest VRTS3 training board includes an LDO (U301), bulk capacitors (C301-C304), a decoupling capacitor (C402) and a 125 MHz clock (OSC401). The connections are made by PCB traces.

The impedance of the power converter—in this case, the LDO—is measured at the decoupling capacitor in order to observe the power quality at the load (125 MHz clock) over frequency. It is shown in Fig. 3. The impedance

is measured with two different output capacitors and also with a 2.4 Ω resistor switched in series between the voltage regulator and the decoupling capacitor.

Yes, the insertion of the resistor significantly degrades the voltage regulation of the LDO and yet, the impedance seen at the clock is much lower with the series resistor added. This is the result of matching the impedance of the voltage regulator with the impedance of the circuit board and decoupling capacitor such that the circuit being powered (the clock) sees the power quality it needs.

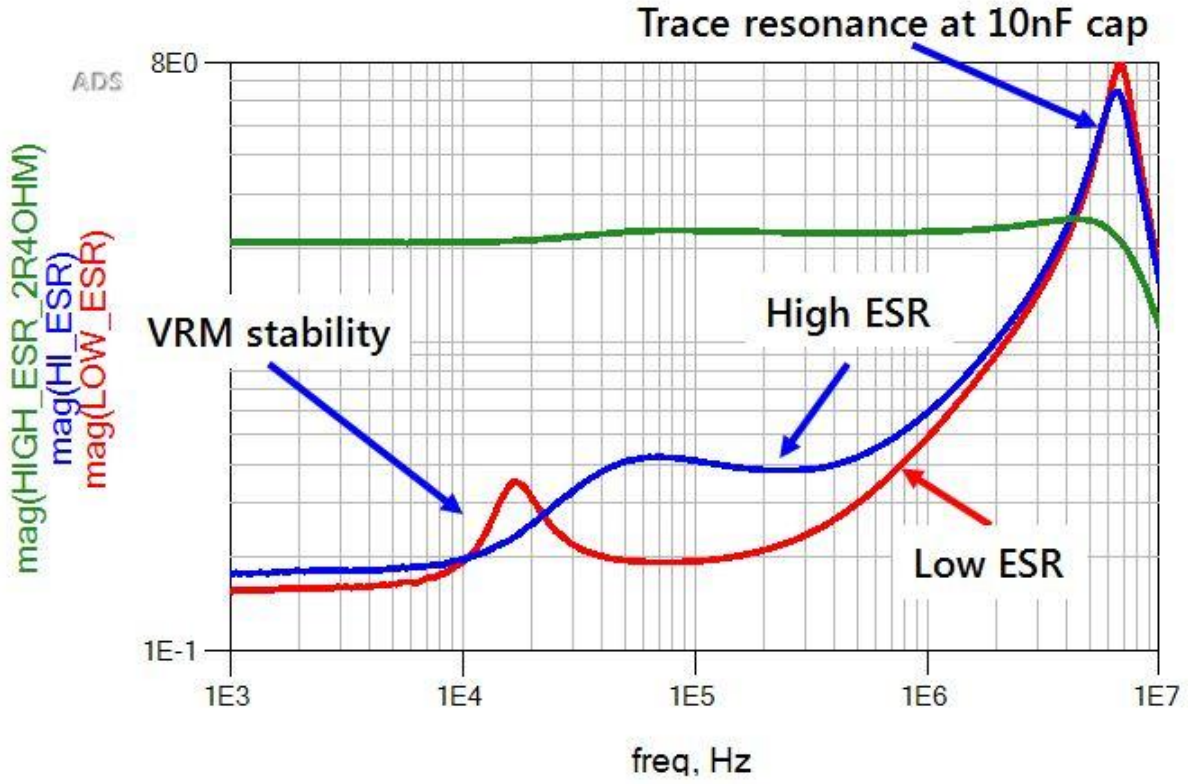


Fig. 3. The impedance is measured at the clock decoupling capacitor (C402) with two different output capacitors and with a 2.4 Ω resistor switched in series between the LDO and the decoupling capacitor. The red trace is the impedance with no resistor, the blue trace is the impedance with the resistor installed.

The impedance in the red trace is with a low-ESR capacitor that results in an impedance peak at approximately 15 kHz due to poor control-loop stability in the LDO. A second peak appears at approximately 7 MHz and is the result of the net inductance of the PCB trace resonating with the local decoupling capacitor (C402). Since there are two peaks, it is possible to generate a *rogue wave* by exciting both resonances simultaneously as seen in Fig. 4.

A rogue wave is the result of multiple step loads aligning in time to cause a forced response at the regulator (as opposed to a natural response) as illustrated in Fig 4. The rogue wave can be difficult to reproduce in test, yet can easily cause the power to exceed its regulation limits when it occurs in an application. Even one resonance can be excited if the step loads occur at the right time. This is why the impedance needs to be flat and why the power supply's output impedance must match the system it is connected to.

Certainly there are alternative methods of correcting this deficiency. One possibility is to replace the 10 nF capacitor with a larger decoupling capacitor. In this case, using the high-ESR regulator output capacitor and replacing the 10 nF decoupling capacitor with 0.47 µF with a 0.5 Ω ESR would also eliminate the impedance peak. The capacitor likely needs to be closer to 1 µF to overcome the dc bias effect of the ceramic capacitor. This solution adds more parts and the 0.47 µF ceramic might be significantly larger.

Another possibility is to move the regulator closer to the clock and possibly increase the width of the PCB trace or reduce the dielectric thickness of the PCB. The point is that the power converter, PCB and system have to be

designed as a unit. Designing a power converter in isolation of the system will only pass the problems on to someone else where it will ultimately result in a costlier solution.

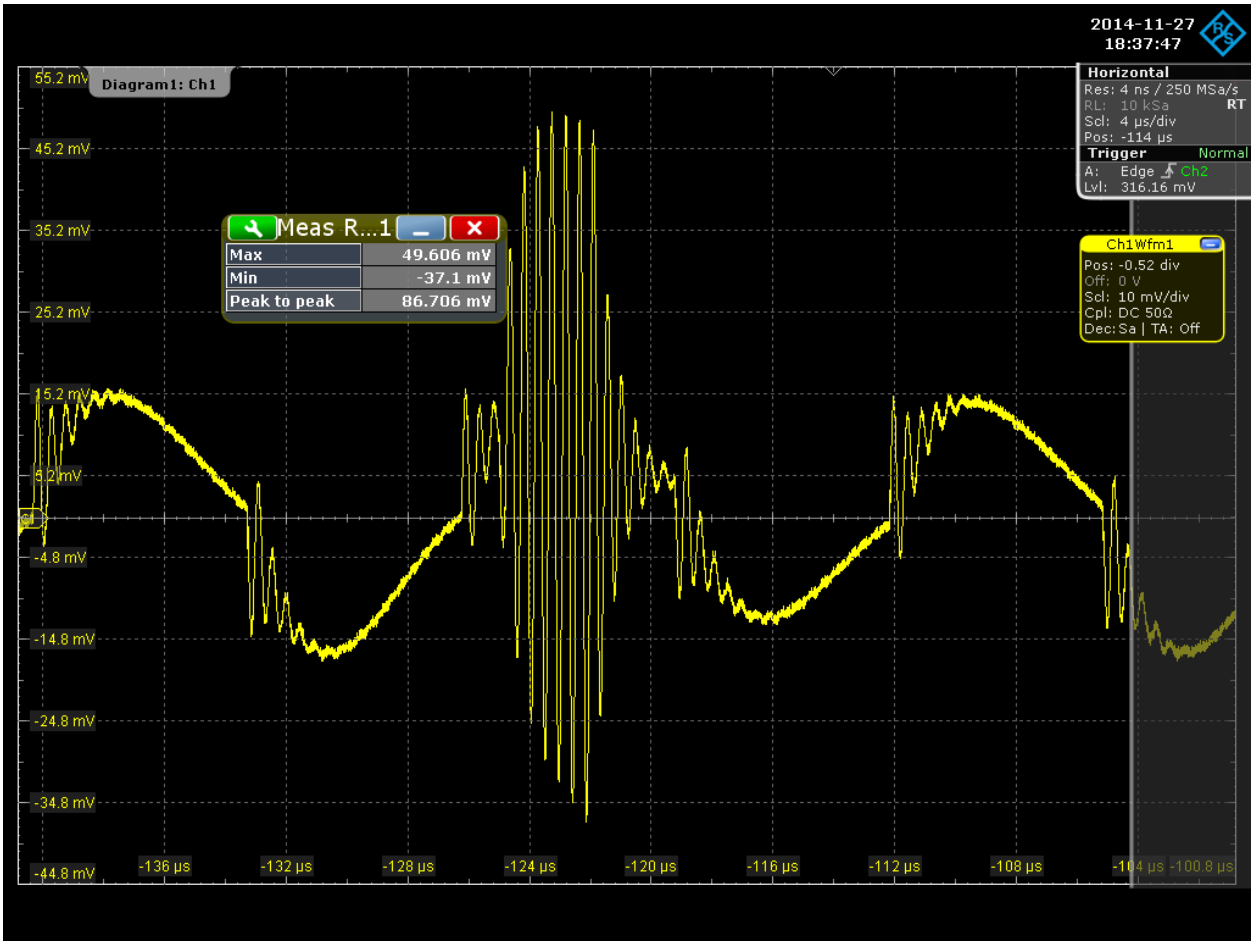


Fig. 4 Creating a load step that excites the forced resonance at the lower frequency, followed by an appropriately timed burst at 7 MHz results in a rogue wave with peak to peak voltage exceeding either resonance.

Selecting a lower-cost and higher-ESR capacitor results in the blue trace in Fig 3. The first sharp resonance at 15 kHz has been eliminated and note that while the ESR of the regulator output capacitor increased, the 7 MHz impedance at C402 is now lower than with the low-ESR capacitor. *So a regulator with higher output resistance produced a lower impedance at the load, which is counterintuitive.* Meanwhile, the 7 MHz peak is still large since the VRM output resistance is much lower than the characteristic impedance of the PCB and decoupling capacitors.

The clock spectrum is shown in Fig. 5 with and without the 2.4 Ω series resistor switched in. Without the series resistor, the clock shows strong 7 MHz sidebands while these sidebands are eliminated by switching in the 2.4 Ω series resistor.

Fig. 4. The clock spectrum shows strong sidebands at 7 MHz without the series resistor present, but these sidebands are eliminated when the series resistor is switched in.

Conclusion

Power integrity is misconceived as a system issue, but as we have shown, the voltage regulator and the system interact with each other. It is up to the circuit designer (i.e. the system or hardware designer) to make measurements of the power converter (regulator, switcher, LDO, etc.) by itself, since power IC and module manufacturers don't supply the required output impedance data. With this data in hand, not only can the designer make a simulation model, but they can also properly tune their PDN and load impedance to the performance of the power supply, and thus produce a system with good power integrity.

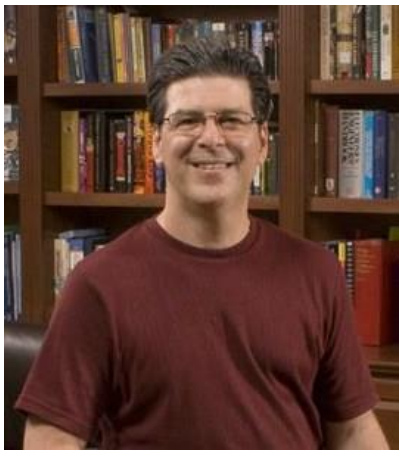
As for the power IC and power module designers, they have a role to play too. It's true that they cannot account for all the requirements of the customer's load in developing standard, off-the-shelf products. However, they can show their customers the importance of flat impedance for the regulator output and how to achieve it as well as how to control the magnitude of that impedance.

A well planned PDN saves time and money, as well as a great deal of aggravation and stress. The power converter, printed circuit board and circuits being powered are generally designed independently and on different time schedules. Nonetheless, it is important to determine the general power characteristics required by the load circuits. The primary characteristics include the voltage level and accuracy, ripple and noise voltage, operating load current and dynamic load current transients. These characteristics will help in determining the power supply impedance, printed circuit board plane impedance, and decoupling networks.

References:

1. "PDN Basics For Power Designers," a three-part video series by Steve Sandler, How2Power Today, September 2014.
    a. Part 1: What's A PDN. In this 4-min. video, Steve explains what PDNs are and why they matter, particularly to developers of POLs and VRMs.
    b. Part 2: Keep Impedance Flat. In this 6-min. segment, Steve discusses power converter output impedance and why designers of board-level power converters need to keep their output impedance curves flat.
    c. Part 3: Impedance Matching Is Critical. In the last video, which runs 3 min., Steve explains why the output impedance of a power converter needs to be matched to the impedance of the PDN in which it is used.
2. "Troubleshooting Distributed Power Systems," an 8-part video series by Steve Sandler, How2Power Today, May 2013 through January 2014. The videos most relevant to this discussion on power integrity are:
    a. "Part 1: Why Stability Matters"
    b. "Part 2: Impedance Is The Critical Measurement"
    c. "Part 3: Measuring Impedance Using Vector Network Analyzers (One-Port Tests)"
    d. "Part 4: Measuring Impedance Using Vector Network Analyzers (Two-Port Tests)."

About The Author



Steven Sandler is the managing director of Picotest, a company specializing in precision test and measurement equipment. Sandler is also the founder and chief engineer of AEi Systems, where he leads development of high-fidelity simulation models for all types of simulators as well as the design and analysis of both power and RF systems.

Sandler has over 30 years of experience in engineering and is a recognized author, educator and entrepreneur in the areas of power, RF and instrumentation. His latest book, "Power Integrity: Measuring, Optimizing and Troubleshooting Power Related Parameters in Electronics Systems," was recently published by McGraw-Hill Education.

For further reading on power integrity, see the How2Power Design Guide and do keyword searches for "power integrity" and "power distribution network."