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Vertically Stacked MOSFETs And Other Tricks For Building A High-Density 30-A Point-of-Load Regulator

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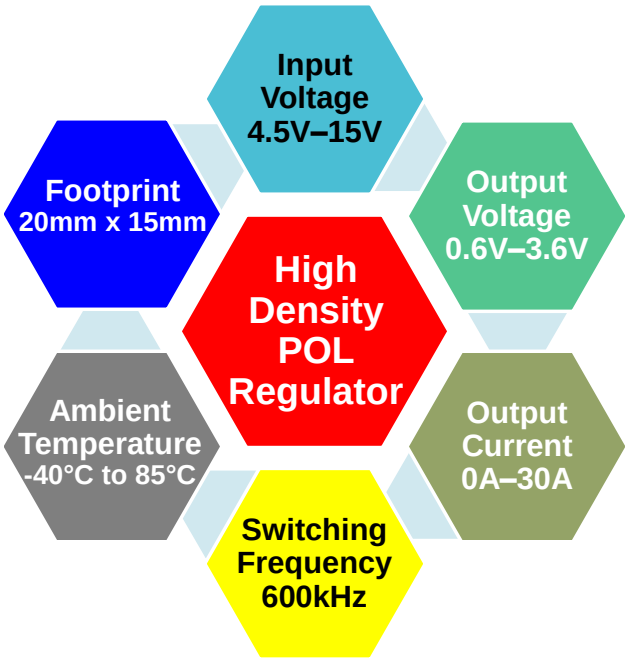
This article tackles the challenge of fitting numerous dc-dc regulators onto a dense system motherboard to power various high-current loads including FPGAs, ASICs, digital signal processors (DSPs) and microcontrollers (MCUs). These systems typically require numerous voltages for core, auxiliary and I/O rails and have limited board area dedicated to power management. One solution lies in a point-of-load regulator (POL) module that is designed to parallel stack onto a system motherboard in a mother-daughter configuration.

By way of example, we delve into a modular implementation with high density that provides 30 A of output current. Operating from a nominal 12-V input rail and with an output voltage adjustable from 0.6 V to 3.6 V, the design uses 3D-integrated MOSFETs, an efficient shielded inductor, ceramic capacitors and voltage-mode controller with integrated MOSFET gate drivers.[1] High density (200 A/in^3) and low bill-of-materials cost of less than $5 U.S. are the main tenets of the design.[2] The circuit schematic, board layout and experimental waveforms are provided, and relevant features of the major active and passive components are outlined.

High-Density POL Regulator

Fig. 1 includes a set of buck regulator specifications as well as fundamental strategies to achieve high density. The ambient temperature range is provided with the caveat of using adequate cooling airflow or appropriate output current derating to ensure maximum component operating temperatures are not exceeded.



Key Enablers of High Density

1. **High switching frequency**
   – Smaller inductive and capacitive filter components
   – Higher loop crossover frequency
2. **Efficient power MOSFETs**
   – Vertically stacked high- and low-side devices
   – Low $R_{DS(on)}$, Q_G and Q_{RR}
3. **Integrated, flexible PWM controller**
   – On-chip gate drivers with adaptive deadtime switching
   – Accurate, lossless current sensing
4. **Optimized PCB layout**
   – Minimize layout parasitics: tight power and gate loops
   – Thermal vias & SMT power connections for heat removal

Fig. 1. Buck regulator specifications and main attributes to achieve high density.

To meet the design specifications, a proposed solution represented by the schematic of Fig. 2 includes power MOSFETs, controller with integrated gate drivers and bias supply, current sensing, output voltage feedback and control-loop-compensation components.[3] The output voltage is set by a resistor from TRIM to S–. The schematic also identifies high-current connections, noise-sensitive nets and high-dv/dt circuit nodes in preparation for a printed circuit board (PCB) layout.

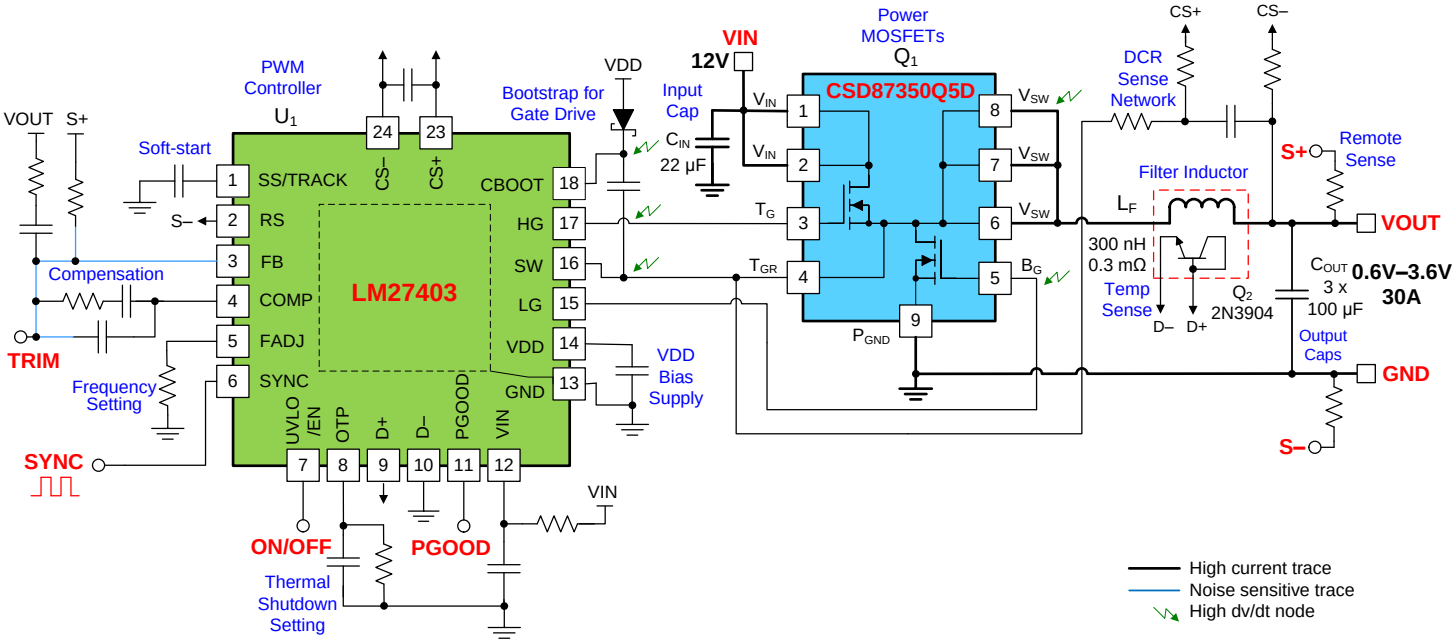


Fig. 2. Synchronous buck converter schematic.

Power Stage Components

The package size and manufacturer's recommended pad geometry of the most essential circuit components are detailed in Table 1, and a brief discussion of the salient features of these components follows. Any bulk storage capacitors associated with the input or the output are conveniently placed on the system board adjacent to the relevant module terminals and not necessarily placed on the module itself.

Table 1. Module circuit component package sizes and recommended pad geometries.

Component	Footprint and profile (mm)	Recommended land pattern outer dimensions (mm)
Dual power MOSFET	5.0 x 6.0 x 1.5	5.15 x 6.24
Controller	4.0 x 4.0 x 0.8 (WQFN-24)	4.2 x 4.2
Filter inductor	11.0 x 7.2 x 7.5	11.5 x 2.1
Output capacitor	3.2 x 1.6 x 1.8 (EIA 1206)	3.5 x 1.5
Input capacitor	3.2 x 2.5 x 2.7 (EIA 1210)	3.5 x 2.4
PCB edge-plated terminals	0.6 oz (1 mil/0.025 mm) thick	2.2 x 3.4 on system board

Power MOSFETs

One choice for power MOSFETs is the CSD87350Q5D,[4] a +30-V half-bridge arrangement of two co-packaged MOSFETs using 3D structure and package integration techniques.[6] Co-packaging of high- and low-side power MOSFETs reduces power-loop parasitic inductance, thereby improving switching performance. Using a system-optimized grounded leadframe, thick copper clips for input (V_{IN}) and switch (SW) power connections, and vertical die stacking, the asymmetric MOSFETs are optimized for low-duty-cycle operation, high efficiency and high power density at switching frequencies as high as 1 MHz.[4]

The low-side synchronous and high-side control MOSFETs have 1.2-mΩ and 5.0-mΩ effective on-resistances at 25°C, and gate charges of 20 nC and 8.4 nC, respectively[4]. With the common-source inductance of the high-side MOSFET essentially eliminated by making Kelvin gate connections, these low-charge parameters enable very low switching losses. Total MOSFET power dissipation at 1.8 V and 25 A output in this application, including conduction and switching loss contributions at 100°C junction temperature, is 2.5 W.

PWM Controller

A synchronous buck controller like the LM27403[3] provides integrated high-current gate drivers and a bias supply regulator. Additional features include a wide input-voltage range of 3 V to 20 V, voltage-mode control with input voltage feedforward, 1% feedback accuracy over the full temperature range, precision enable for programmable input undervoltage lockout (UVLO), user-defined thermal shutdown, output voltage remote sense, and inductor dc resistance (DCR)-based overcurrent protection.

A remote diode-connected transistor facilitates cost effective and accurate temperature measurement at the inductor. Controller power dissipation, including gate-drive losses at 600 kHz, is 0.25 W. The control-loop bandwidth is approximately 80 kHz at an output voltage of 1 V, but increases as output voltage increases. This is attributable to the ceramic capacitor's nonlinear class 2 dielectric and the rolloff of capacitance with increasing applied voltage. When switching at 600 kHz and low duty cycle, the LM27403's 30-ns minimum on-time is particularly advantageous.

Filter Inductor

Table 2 shows four possible choices for a ferrite inductor with single-staple winding. With the Wurth inductor for example, component power dissipation at 1.8-V and 30-A output, including copper and core loss at 75°C operating temperature, is 0.6 W. With continuous DCR current sensing, the setpoint for active peak-current limit is nominally 33 A. Change in inductor DCR with temperature is compensated by the controller's remote temperature-sense capability to generate a concomitant change in current limit threshold voltage with temperature.

Notwithstanding the inductor's extremely low DCR, a workable current-sense signal is available by advantageously employing the bus structure copper resistance in the output power path to increase the effective sensed-current signal amplitude.[5] Parenthetical to this, note that inductor designs with vertical standoffs to mount over other powertrain components are eschewed here as these are typically custom components and can degrade the thermal performance of the overall design.

Table 2. Options for filter inductor.

Inductor manufacturer and inductance	Wurth Electronik 250 nH	Cyntec 300 nH	Coilcraft 270 nH	Coiltronics 300 nH
Manufacturer's part number	744308025	HCB1175-301	SLC1175-271MEC	FP1107R1-R30-R
Inductor DCR at 25°C	0.37 mΩ ±7%	0.29 mΩ ±7%	0.24 mΩ ±5%	0.29 mΩ ±8%
Saturation current at 25°C	44 A	34 A	37 A	35 A
Dimensions, max.	10.6 x 7.4 x 7.0 mm	11.0 x 7.2 x 7.5 mm	11.0 x 7.6 x 7.2 mm	11.0 x 7.2 x 7.5 mm

Input And Output Capacitors

One 1210 ceramic capacitor provides input filtering with rated capacitance and voltage of 22 µF ±20% and 25 V, respectively. The input capacitor is specifically positioned close to the MOSFETs to minimize switching loop parasitic inductance. Three 1206 ceramic capacitors provide output filtering[7] with rated capacitance and

voltage of 100 µF ±20% and 6.3 V per device, respectively. Various choices for the input and output capacitors are detailed in Table 3.

Table 3. Options for ceramic capacitors.

Capacitor manufacturer	TDK	Murata Electronics	Wurth Electronik
Input cap manufacturer's part number	C3225X5R1E226K	GRM32ER71E226K	885012109014
Output cap manufacturer's part number	C3216X5R0J107M	GRM31CR60J107M	88501208005

Power Terminals

Edge-plated terminals are used for surface-mount connection to the system board. Three large-area power terminals, V_{IN}, V_{OUT} and GND, are provided for optimal electrical and thermal connection to the system PCB. The fact that the input and output ground connections are shared results in some current cancellation and conduction loss reduction. Seven signal terminals are available, specifically TRIM, S+, S–, SYNC, PGOOD, UVLO/EN, and SGND.

High-Density PCB Layout Considerations

The design specifications of the four-layer PCB, particularly with regard to surface-mount manufacturability, are given in Table 4. The solution occupies a total PCB area of 3 cm^2 (0.46 in^2) yielding a current density of 10 A/cm^2 (65 A/in^2). The PCB layout is depicted in Fig. 3. As components are placed on one side only, the design allows for component placement directly on the system board as a voltage-regulator "down" (VRD) implementation, if needed.

The critical aspects of the layout relate to the power stage. To the extent that it reduces parasitic inductance, tight layout of the switching loop comprising the input capacitor and power MOSFETs is vital to minimize the switch-node voltage overshoot and ringing that inevitably occur during MOSFET commutation.[8] Purposely locating the input capacitors close to the MOSFETs also mitigates ground noise and bounce associated with high slew rate current transitions in the switching loop.

Most important, the MOSFETs' gate drive and gate return traces (HG and SW for the high-side MOSFET, LG and GND for the low-side MOSFET) are routed as differential pairs with minimal loop area. These gate traces are very short as the controller is positioned immediately adjacent to the MOSFETs. The MOSFETs' SW connection adjoins the inductor terminal and the resulting small SW-node polygon connection area lessens radiated electromagnetic interference (EMI) and undesired coupling to sensitive control circuitry.

The internal PCB layers mainly constitute paralleled ground planes for heatsinking and conduction drop reduction. To conveniently connect to the internal ground planes and move heat away from the MOSFETs, multiple thermal vias with 12-mil diameter hole size are placed at the MOSFET ground tab (the source-down connection of the low-side MOSFET).

Table 4. PCB design rules and specifications.

Parameter		Specification
Spacing (min)	Pad to trace	6 mil (0.15 mm)
	Pad to pad	6 mil (0.15 mm)
	Trace to trace	6 mil (0.15 mm)
	Component body to body	10 mil (0.25 mm)
Trace width		8 mil (0.2 mm) min.
Finished hole size		6 mil (0.15 mm) min.
Via size		8 mil (0.2 mm) drill, 16 mil (0.4 mm) ring min.
Filed vias		No
Tented vias		Yes
Copper thickness		2-oz. copper, all 6 layers
Copper edge-plated terminals		0.6 oz (0.2 mm) min. thickness
PCB finish, all exposed surfaces		3-7 mil immersion gold over 100-150 mil electroless nickel
Solder paste stencil		6 mil

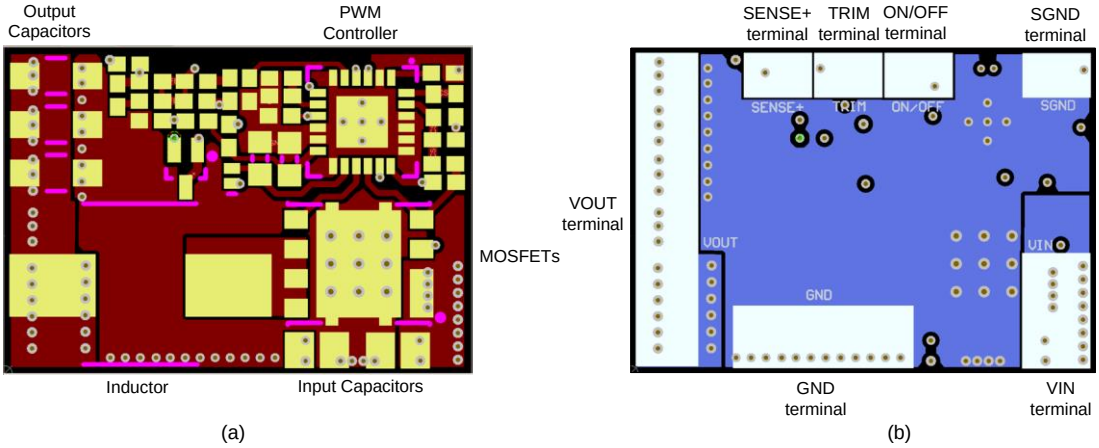


Fig. 3. PCB layout (top down view): top layer (a) and bottom layer (b).

A dedicated ground plane is placed on layer two and signal lines are placed on the top layer and layer three to maximize the available copper plane area. The small-signal components in 0402 footprint are located close to the controller with return traces routed directly on the top layer. Thus, power and signal grounds are effectively connected at one point, such as the controller ground pad.

Decoupling capacitors in 0603 footprint for the controller's V_{DD} and V_{IN} supply rails are also placed close to the relevant pins. It is imperative to keep vias for small-signal connections to an absolute minimum as these consume valuable board space. Those that are required are strategically positioned to avoid high-impedance points that could pinch off or compromise the effectiveness of wide copper plane and polygons areas.

Copper plating along the vertical edge areas of the PCB where the power and signal terminals are located enhances both the electrical and thermal connections to the system PCB and reduces the interlayer (z-axis) bus structure impedance. The output-voltage sense line is routed directly to the output terminal to optimize load regulation when output remote sensing is not required.

Fig. 4 shows an actual prototype of the POL module reflecting the design guidance provided here.

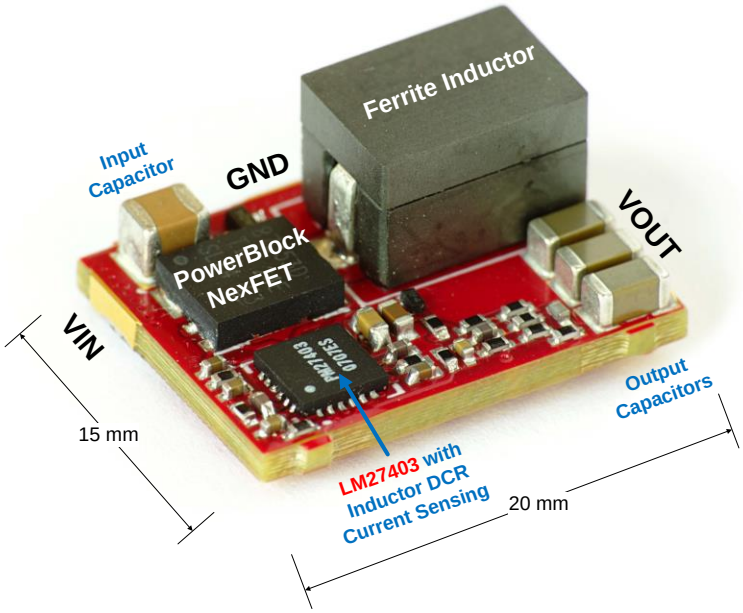


Fig. 4. An implementation a 30-A dc-dc regulator.

Thermal Management

The system board to which the surface-mounted POL module is soldered acts as a primary method of heatsinking. Conductive thermal dissipation and heatsinking are provided through the module's terminal connections. The heat-generating components can leverage the copper polygons, planes and thermal vias that are already available on the system PCB layer stackup to improve its thermal characteristics.

The wide, low-profile connection of the edge terminations from the module to the system board also enhance heat removal. The major power dissipating components, such as the MOSFETs and inductor, are positioned to purposely capitalize on whatever natural or forced convection is available in the application environment.

Experimental Results

The measured efficiencies at various output voltages are shown in Fig. 5. Experimental measurements, including load transient response, switch-node voltage, pre-biased startup, and output voltage ripple and noise, are recorded to evaluate circuit performance. These performance waveforms are collated in Fig. 6.

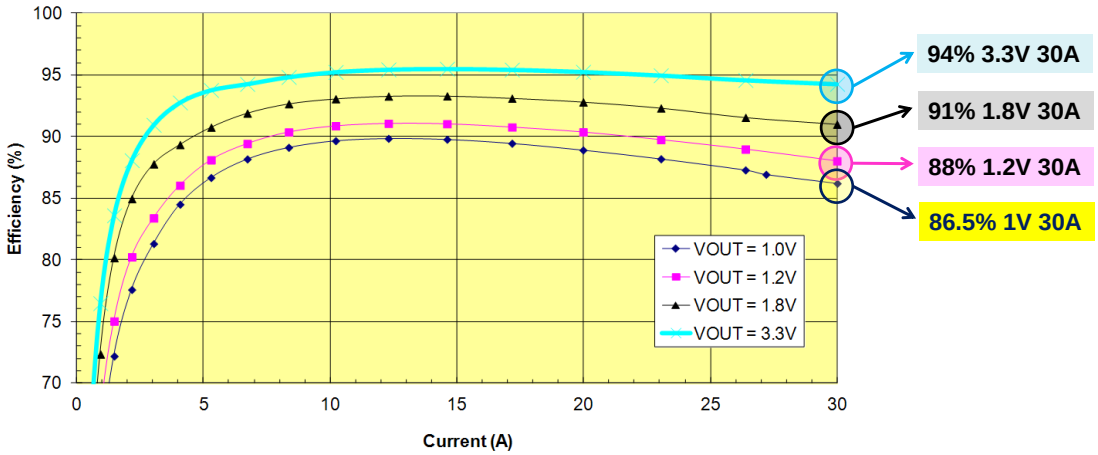


Fig. 5. Converter efficiency vs. load current at various output voltages. V_{IN} = 12 V and $T_{AMBIENT}$ = 25°C.

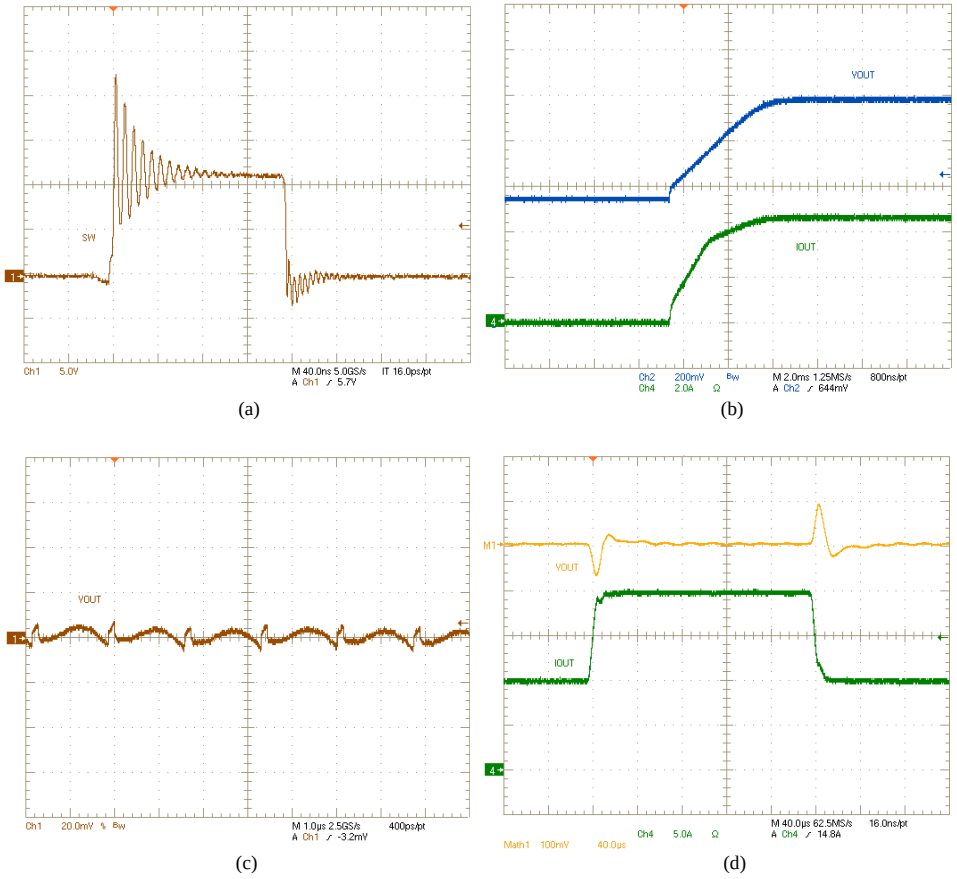


Fig. 6. Performance waveforms at V_{IN} = 12 V and V_{OUT} = 1.0 V: SW node voltage (a); output voltage monotonic startup with pre-bias (b); output voltage ripple, 20-MHz bandwidth (c); and load transient response, 10 A to 20 A to 10 A at 2 A/µs slew rate (d).

Summary

A primary objective of this article was to look closely at ways to achieve high-power density, knowing that it represents a critical aspect of the system power solution, and offer clear guidance on the factors related specifically to high-density synchronous buck converter implementations. Practical advice related to component choice and PCB layout was provided, and experimental results were reported.

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About The Author

Timothy Hegarty is a systems engineer in the Power Products Solutions Business Unit at Texas Instruments. He received his bachelor's and master's degrees in Electrical Engineering from University College Cork, Ireland. His areas of interest are integrated PWM switching converters and controllers for wide input voltage range applications, and system-level simulation for automotive and industrial applications. He is a member of the IEEE Power Electronics Society. You can reach Tim at ti_timhegarty@list.ti.com.

For further reading on point-of-load regulator design, see the How2Power Design Guide, locate the Power Supply Function category, and click on "DC-DC Converters."