Dealing With Nonlinear MOSFET Capacitances

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Since their introduction more than 30 years ago, MOSFETs have become the mainstay of high-frequency switching power conversion. The technology has been improving steadily and today we have low-voltage MOSFETs with sub-milliohm R_{DSON} values. For the higher-voltage devices it is quickly approaching single digits.

Two major developments in MOSFET technology that enabled these improvements were the trench gate, and the charge balancing structures.[1] Originally developed for high-voltage devices that resulted in superjunction MOSFETs, charge balancing is now getting extended to lower voltages as well.

While it reduces both R_{DSON} and all the junction capacitances dramatically, charge balancing makes the latter much more nonlinear. The effective stored charge and energy in the MOSFET are indeed reduced, and significantly so, but calculating these parameters or comparing different MOSFETs for optimum performance has become a rather complicated exercise.

As a result, the conventional approach to understanding MOSFET parameters such as C_{OSS} and C_{RSS} is no longer valid. This article explains why and presents some guidance on how to better evaluate a MOSFET's performance within its operating environment based on principles of stored charge and energy.

Three Capacitances

The basic definitions of the three capacitances associated with a MOSFET are shown in Fig. 1. Measuring these capacitances as a function of V_{DS} is not straightforward and requires some of them to be shorted or left floating during the process. What is finally measured and given on the datasheet is a set of three values defined as

$C_{ISS} = C_{GS} + C_{GD}$

$C_{OSS} = C_{DS} + C_{DG}$

$C_{RSS} = C_{GD}$

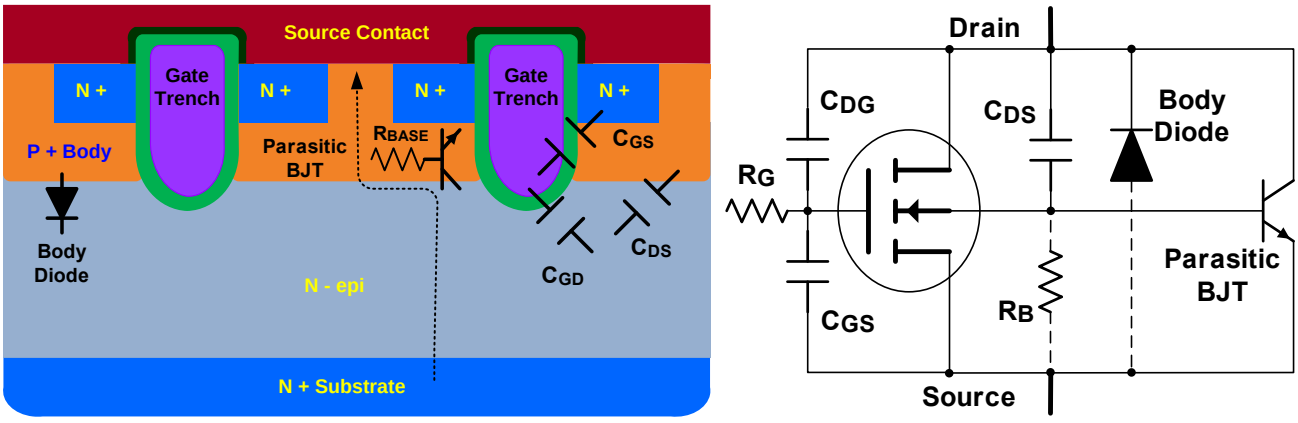

Fig. 1. Structure of a trench MOSFET and its capacitances (a) and the same capacitances shown schematically with other transistor elements (b).

Of the three, the input capacitance C_{GS} is the least nonlinear. It is the capacitance between the gate structure and the source and is not subject to much variation as a function of V_{DS}. On the other hand, C_{GD} is extremely

nonlinear, varying by almost three orders of magnitude within the first 100 V for superjunction devices. It also contributes the slight step seen at V_{DS} = 0 for C_{ISS}.

Recently there has been a lot of interest in understanding the nature of C_{OSS} and the impact it has on high-frequency switching. There are several reasons for this interest. The C_{OSS} stored charge and loss have become the biggest challenges in implementing high-frequency ac-dc converters. In general, any capacitance-related loss is proportional to the square of the applied voltage. As pointed out in [3], the same capacitor has 2100 times more stored energy, and loss, at 550 V compared to 12 V.

With the focus on reducing R_{DSON}, the conduction losses have come down significantly, but the reduction in C_{OSS} has not been proportional. For example, the lowest R_{DSON} for a 600-V MOSFET in a TO-220 used to be 340 mΩ in earlier days. Today it is down to 65 mΩ for 600-V superjunction devices. For capacitance it is more relevant to compare devices with similar R_{DSON} values across different technologies.

Fig. 2 compares the capacitances for the SiHP17N60D, a planar device, with the SiHP15N60E, a superjunction MOSFET with close, but slightly lower R_{DSON}. Note that the values are plotted on a logarithmic scale. C_{OSS} at 100 V has reduced from 136 pF to 67 pF for the superjunction device, but it has also become much more nonlinear. The ratio of C_{OSS} at V_{DS} = 0 V to C_{OSS} at 100 V, which was 25:1 in case of the planar device, has now risen threefold to 75:1. It is not uncommon to have C_{OSS} values more than the input capacitance C_{ISS}, at V_{DS} = 0 V.

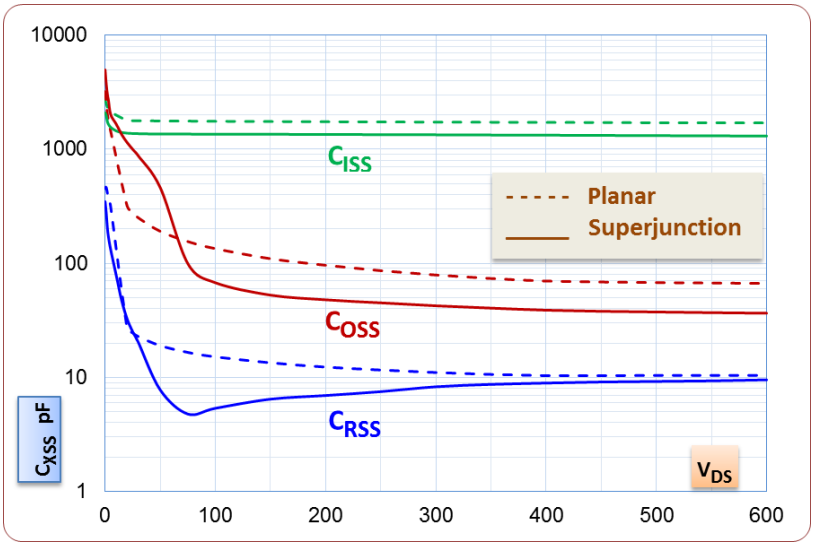

Fig. 2. Comparing capacitances for planar versus superjunction MOSFETs.

Efforts To Explain The Nonlinearities

Several attempts have been made[4-9] to explain the nonlinear nature of C_{OSS} and provide new insights on the impact it has on high-frequency switching. At the end of the integrations, simulations and other complex processing of the C_{OSS} curve, most of them merely re-assert the nonlinear nature of the capacitance. The terms "small signal" and "large signal" capacitance have been introduced, simulated and analyzed. Besides being technically incorrect, the new nomenclature does not offer any differentiation from industry practices.

It can be shown that the so-called large signal capacitance is nothing other than the time-related value C_{OTR} that the MOSFET industry has been specifying for years following reference [4]. The differences highlighted between the results of elaborate simulations and datasheet values are well within the tolerances involved in the characterization and mass production of MOSFETs.

Another line of analysis proposes a hidden resistance in series with C_{OSS}, called R_{OSS}, to account for all unexplained losses associated with the nonlinear capacitance.[10] This is contradictory to basic circuit theory, which clearly states that capacitor charging and discharging losses are defined entirely by the energy stored in it and independent of the value of any series resistance.

Furthermore, no semiconductor-level explanation or experimental validation is provided for R_{OSS}, and the waveforms provided in the paper clearly show the MOSFET body diode in conduction, which provides a much simpler, if less exotic, explanation for the losses. Body diode conduction is, in fact, an elementary consideration in the analysis of any bridge circuit with an inductive load.

In other recent, peer-reviewed conference publications [11] and [12], it has been suggested that both stored charge and energy in C_{OSS} have a hysteresis, and can be different depending on the path taken by voltage. The implication of such hysteresis would be that the principle of conservation of charge does not hold for power MOSFETs.

A Different Approach

Instead of challenging fundamental laws of physics, it might be more instructive to revisit them and verify that they are being applied correctly, and in context. The investigation can be made a little more interesting with a puzzle:

If two capacitors are connected in parallel, charged to the same voltage and carry exactly the same stored charge, does it necessarily follow that they are also storing the same energy?

Going by the well-known formulas of $Q = CV$ and $E = ½ CV^2$, the answer should be a firm yes. It might appear that the result will hold at any voltage, even if the capacitances are nonlinear.

Unfortunately, the familiar formulas for stored charge and energy are not universally valid and hold true only for the special case of constant capacitances. The more fundamental relations define capacitance as the rate of change of charge with respect to voltage, and voltage itself is the measure of change in energy per unit of charge. In other words, the basic relations are

$C = dQ/dV$ and $V = dE/dQ$

The simple equations for charge (Q) and energy (E) were derived with the implicit assumption of constant capacitance. For nonlinear capacitances, charge and energy must be derived by integrating capacitance and charge respectively, over the voltage.

To illustrate this further, consider the two capacitors drawn in Fig. 3. The reference is provided by the capacitor C_{REF}. The other capacitor C_V varies linearly from 1.5 x C_{REF} to 0.5 x C_{REF}. At 100 V, they will carry the same charge. This is clear from looking at the total C x V area for both the capacitors and is also verified by integrating capacitance values over voltage.

The stored energies, however, are quite different. If the stored charge is integrated over voltage, it will turn out that C_{REF} has only 83.3% of the stored energy at 100 V. It can also be shown that at 75 V, C_V has 10% more stored charge but same energy as C_{REF}.

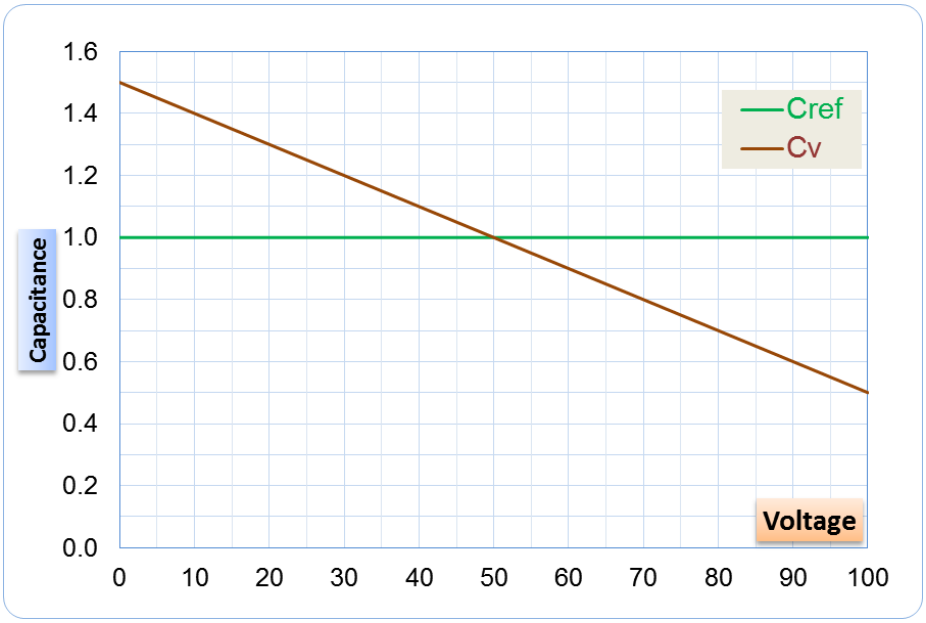

Fig. 3. Constant vs. variable capacitances.

MOSFET manufacturers have been doing these integrations for years, but instead of specifying them as charge and energy, they convert them to two different equivalent capacitances.

C_{OTR} – a fixed capacitance that has the same stored charge as C_{OSS} when charged to 80% V_{DSS}

C_{OER} – a fixed capacitance that has the same stored energy as C_{OSS} when charged to 80% V_{DSS}

An "effective" C_{OSS} at 80% of the rated voltage was empirically described in [4], same as the time-related equivalent capacitance. However, the application note did not distinguish between C_{OTR} and C_{OER}, which have now become much more diverse and need to be treated individually.

Note that both C_{OTR} and C_{OER} are themselves functions of voltage; any integration of a nonlinear function will always produce another nonlinear function. Therefore, datasheets define them at some specific voltage like 80% of rated V_{DS} or 400 V. The fact that two different "equivalent" values exist for the same C_{OSS}, one for stored charge and another for energy, more or less answers the puzzle.

C_{OTR} and C_{OER} are not only different, the extent of their divergence can serve as a measure of the nonlinearity. In our example, the 1.5:0.5 capacitance range results in a 16.7% difference between C_{OTR} and C_{OER}. The same C_{OTR}/C_{OER} ratio for the SiHP15N60E is almost 3.6. For other superjunction devices, the capacitance range can be wider than 100:1 and the C_{OTR}/C_{OER} ratio can be higher than 10. Fig. 4a highlights the difference in stored charge and energy for SiHP15N60E.

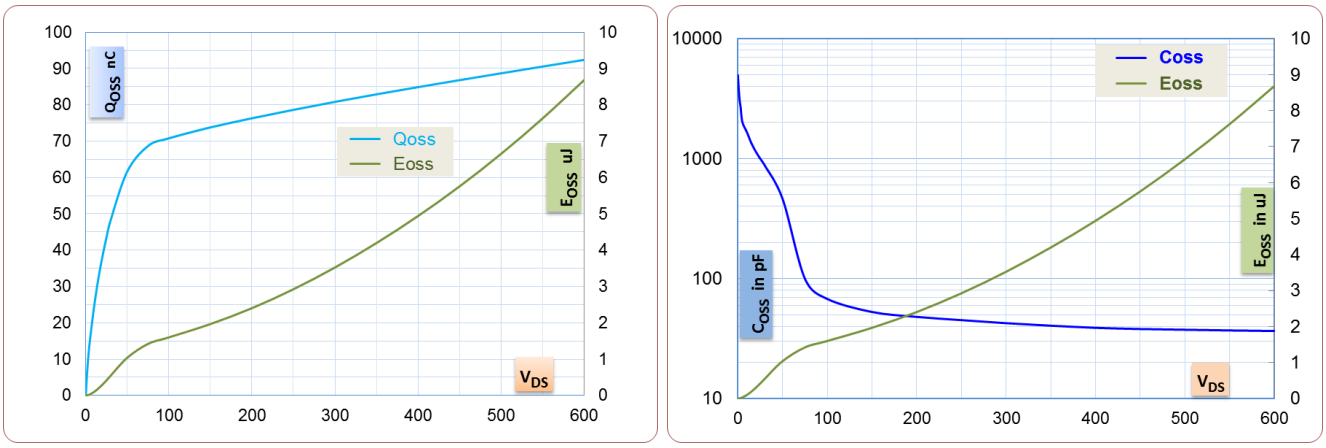

Fig 4. C_{OSS} stored charge and energy vs. voltage (a) and capacitance and stored energy vs. voltage (b) for the SiHP15N60E superjunction MOSFET.

The rate of change for these two related parameters, as a function of voltage, is dramatically different. The extra-large C_{OTR}, and by implication total stored charge, needs to be taken into account in all the bridge configurations, especially those that operate in ZVS mode. Discharging the output capacitor of the MOSFET is not quite the same as de-energizing it, and the design calculations should be done based on the C_{OTR} rather than C_{OER}. Of course, C_{OER} and the energy calculations are still required for switching loss calculations.[3]

Focusing On Stored Charge And Energy

It should be clear by now that the absolute value of C_{OSS} at any voltage is no longer meaningful. Or required by the users. It is not capacitance by itself that interacts with the circuit, but the stored charge and energy that define the behavior. If you look at any design calculations that involve C_{OSS}, you will find that somewhere it gets converted to stored charge or energy by multiplying with the relevant voltage factors.

To aid the system designers further, some MOSFET manufacturers including Vishay, now offer complete E_{OSS} curves in their high-voltage datasheets, as shown in Fig. 4b, in addition to C_{OTR} and C_{OER}. Q_{OSS} at 50% is also commonly specified for 100-V MOSFETs to help with deadtime analysis in 48-V ZVS bridges.

Similar considerations apply to the gate-drain capacitance C_{RSS}, but its value is much less than that of C_{OSS}. By definition, the value is already included in the measurements of C_{OSS} as mentioned in the beginning. The nonlinear nature of C_{RSS} was in fact identified as an issue long ago and has been accounted for in the literature. The Q_{GD} component of the gate charge curve is nothing but the total stored charge in C_{RSS} that needs to be injected into or removed from the gate during turn-on or turn-off.

Note that the piecewise linear segmentation of the gate-charge curve is not due to any nonlinearity of the capacitances involved. The process of turning on a MOSFET involves charging two different capacitors which have different voltages across them during the off state.[2]

While dealing with MOSFETs it is useful to remember that their capacitances do not consist of two electrodes separated by a dielectric. They are transient in nature, coming into play largely during the switching intervals when the device is subject to high dV/dt.

The capacitances shown in equivalent circuits are representations of the interactions between active electric fields across semiconductor materials and their currents. The representation is meaningful only so long as the relationship is linear. With the kind of extreme nonlinearities we see in today's MOSFETs, it would not be an exaggeration to say that there is no such thing as a C_{OSS} or C_{RSS} anymore. Integrating the capacitance curves does not reveal anything about how they interact with the rest of the circuit. Instead of trying to linearize and

somehow straighten the curve, the designers need to focus on the basics and work directly with stored charges and energies.

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About The Author

Sanjay Havanur currently serves as the senior manager of System Applications for Vishay Intertechnology. He is a member of IEEE, holds seven patents in the field of power conversion, and has authored several papers. Havanur holds a bachelor's degree in electrical engineering and a master's degree in power electronics from the Indian Institute of Technology.

For further reading on MOSFET characteristics and operation, see the How2Power Design Guide, select the Advanced Search option and select "Power Transistors" in the Component category.