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Building An Average Model For Primary-Side Regulated Flyback Converters

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Ac analysis is well covered in the literature for a classical flyback topology involving an optocoupler associated with a shunt regulator like the popular TL431. With the emergence of smartphones and other tablets, the adapter market and more precisely the travel adapter market, the trend is to reduce the size and cost of this "black box" connected to the mains. What are the possibilities to meet these goals?

One option is to simplify the feedback chain and adopt a primary-side regulated type of structure. While regulation through a primary-side winding is a well-known principle, several improvements have been introduced such as better overall accuracy and the ability to control the output current without actually measuring it. These primary-side-regulated (PSR) controllers are now found in a variety of applications and compete against existing optocoupler-based designs. However, the compensation is not covered at all in the literature for the PSR topology. To compensate a power supply, an ac analysis has to be performed by using an average model for instance.

This article will describe the main differences between a classical flyback converter with optocoupler and a PSR flyback. Then we will see how we can build an average model for the PSR flyback (one that includes the required sample-and-hold network) and simplify it without impacting the transfer function. The transfer function will be evaluated and results obtained with Mathcad plots of the transfer function will be compared with simulations of the converter. Finally, the loop compensation will be plotted and calculations needed to adjust the phase margin detailed.

Classical Flyback Versus PSR

The term classical flyback implies a loop built around a secondary shunt regulator—the TL431 for instance—and an optocoupler used to convey the information to the primary side. The typical schematic of such converter is shown in the Fig. 1.

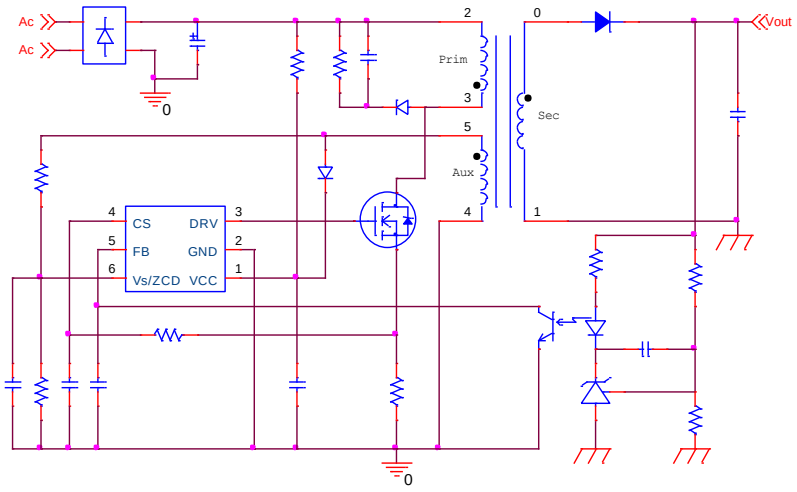

Fig. 1. Simplified schematic of a classical flyback structure.

In this configuration, the output voltage is directly sensed on the secondary side. By modulating the optocoupler LED current, the regulation information is sent back to the primary-side controller, which adjusts the frequency and/or the primary peak current to keep the output voltage at its nominal value.

However, the optocoupler is a relatively expensive part which consumes more PCB space than simple SMD resistors or capacitors (such as those in an 0603 package.) And because millions of travel adaptors are shipped with a cell phone every year, removing the secondary-side circuit and the optocoupler would lead to a substantial economy for the manufacturers. For this reason, new solutions have been developed to eliminate these components as shown in Fig. 2 while maintaining regulation accuracy similar to that achieved by the classical flyback.

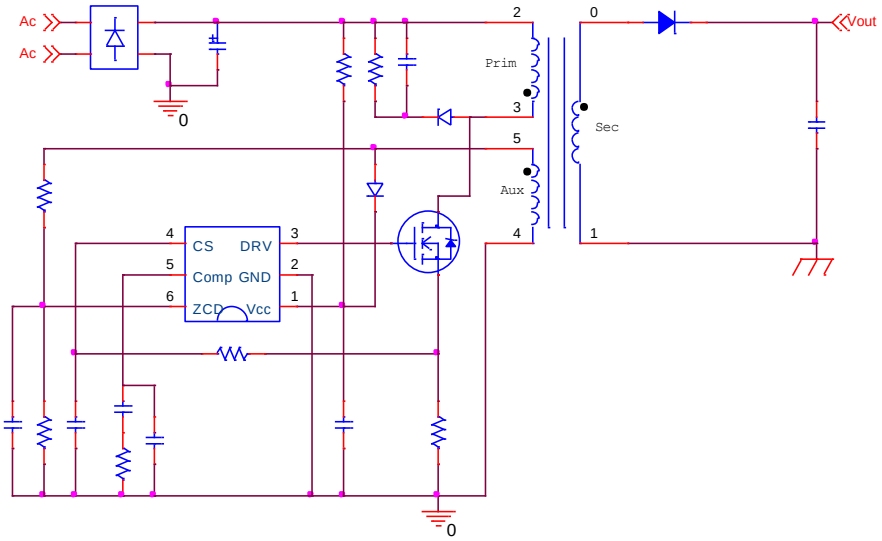

Fig. 2. Simplified schematic of a PSR-based flyback structure.

The PSR Principle

Looking at the schematic in Fig. 2 we can see that the only connection between the primary side (high voltage) and the isolated secondary side (low dc voltage) is the transformer. From a safety and reliability point of view, the elimination of the optocoupler brings advantages: optocouplers are known to drift as they age (such as current-transfer ratio (CTR) degradations) and they can also be susceptible to external perturbations.

What is the operating principle of a primary-side-regulated structure? Let's have a look at signals around the transformer as shown in Fig. 3.

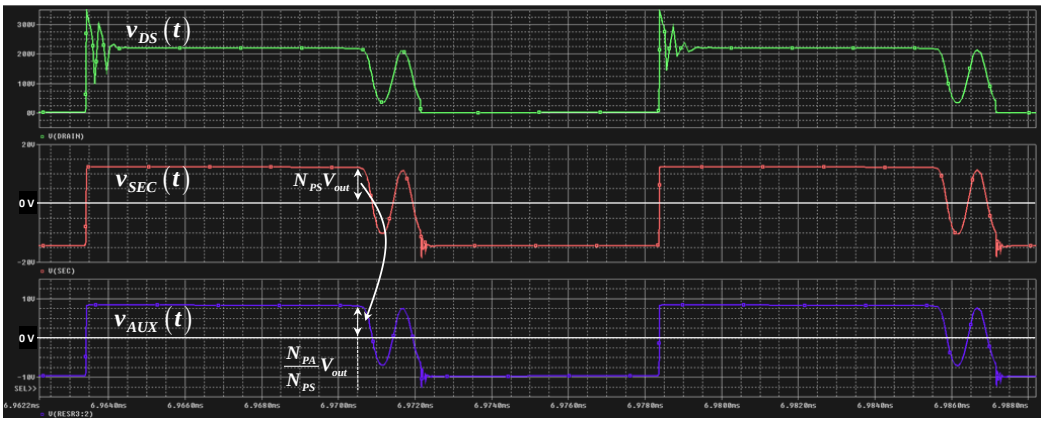

Fig. 3. SPICE waveforms measured on or near the flyback transformer.

During the off time, the drain voltage (V_{DS}) is the sum of the input voltage and the output voltage as affected by the primary-to-secondary turns ratio designated by N_{PS} ($N_{secondary}/N_{primary}$).

Now we will focus our attention on the secondary winding voltage (V_{SEC}). The voltage during the off time, i.e. when the primary-side MOSFET is turned off, equals the output voltage plus a voltage determined by the output rectifier and output capacitor. During the t_{off} phase, the output rectifier diode conducts to supply the load and charges the output capacitor. If we zoom-in on the secondary winding voltage as shown in Fig. 4, we can see that the voltage decreases according to the diode current. This slope comes from the diode dynamic resistance r_d.

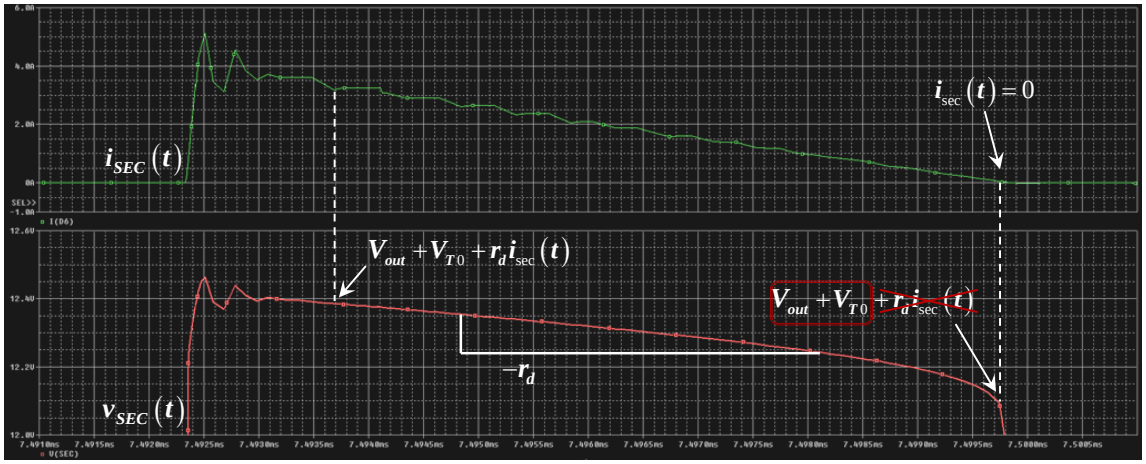

Fig. 4. The effect of diode dynamic resistance on the secondary winding voltage (simulation curves.)

Indeed, the voltage drop across a diode is the sum of two parameters:

- The conduction threshold: V_{T0}
- The drop across the dynamic resistance: $r_d . i_{sec}(t)$.

V_{T0} is a technology-dependent parameter while r_d depends on the operating point of a given diode. The voltage on the auxiliary winding will exhibit the same shape as that of the secondary winding voltage but its voltage value is affected by the auxiliary turns ratio. With the help of Fig. 4, we can easily see that if the primary-side controller samples the voltage at the beginning of the demagnetization time (where the first dotted vertical line appears in Fig. 4), the output voltage information will be affected by the current. At full load, the output voltage will be lower than in light-load operation. The presence of the dynamic resistance explains this difference.

In order to correctly inform the controller, our PSR circuit precisely detects the end of the core demagnetization —the auxiliary voltage knee—before sampling this voltage. This technique naturally produces a faithful representation of the output voltage. In practice, inside the controller die, a sample-and-hold circuit is connected to the Vs/ZCD pin—the pin used to detect the zero crossing of the auxiliary voltage and perform the CV regulation—to implement this feature. The sampled signal is then compared to a reference voltage and generates constant-voltage regulation through an (operational transconductance amplifier) OTA as illustrated in Fig. 5.

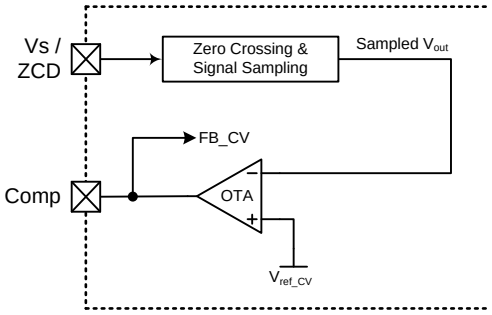

Fig. 5. A simplified schematic for constant-voltage regulation.

The waveform on Fig. 6 shows the curves related to the sampling process. The signal connected to the OTA (red curve) is compared to the reference voltage and is refreshed cycle by cycle without being impacted by the output current. Thanks to this method, the constant voltage regulation is accurate over the output load or input voltage. Load-regulation performance is presented in Fig. 7: we achieved better than 0.5% over the output power range, which is something a conventional, simple auxiliary-based converter could not reach.

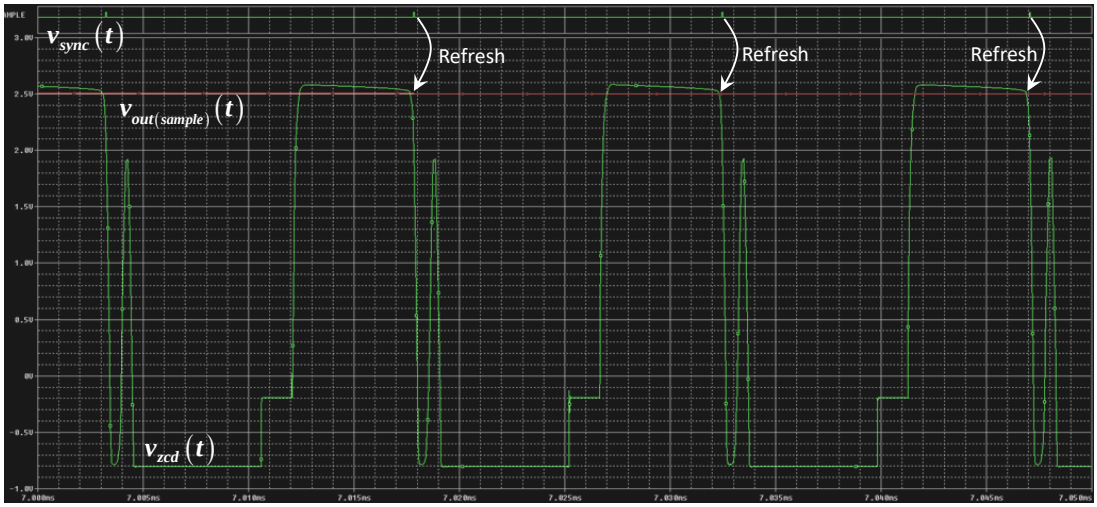

Fig. 6. Refresh of the voltage for CV regulation.

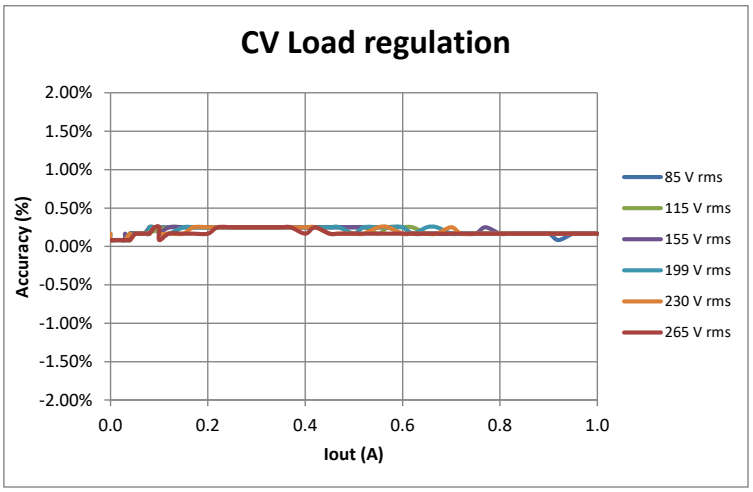

Fig. 7. Constant voltage regulation as a function of load current and input voltage for a PSR controller measured in the lab.

Power Stage Average Model With Primary-Side-Regulation Topology

One option for studying the stability of our converter is to use an average model. To create this model, we will use the pulse width modulation (PWM) switch model introduced in the 90s and adapted to quasi-resonant (QR) operation in reference [1]. The principle behind the PWM switch is to model a cell made of the diode and the primary MOSFET which introduce a discontinuity during the switching event. This approach lead to a simple large-signal three-pin model later linearized for study of the frequency response. Since this method is well covered in the literature (see references [1] and [2]), we will not spend more time on this topic.

Using the PWM switch model for the QR flyback topology, the schematic in Fig. 8 can be drawn.

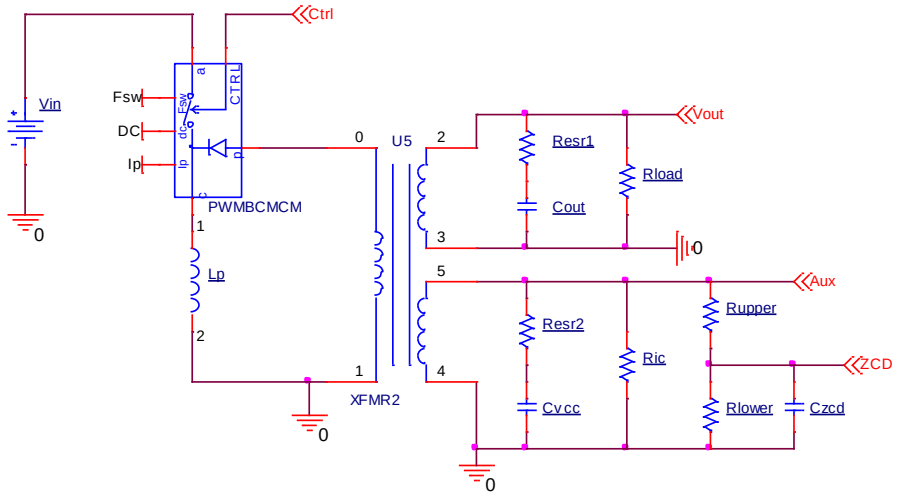

Fig. 8. The PWM switch model in a flyback converter.

This schematic integrates all components around the transformer without simplification for now. Connected to the secondary winding, we can identify the output capacitance (C_{out}) with its equivalent series resistance (R_{esr1}) and the output load (R_{load}). On the auxiliary winding, the V_{cc} capacitor (C_{Vcc}) in series with its ESR (R_{esr2}) is

visible. In parallel, the IC consumption has been modeled with the R_{IC} resistance. Finally, the resistors connected between the auxiliary winding and the ZCD pin are also present. Simulating this schematic in SPICE, we can extract the control-to-output Bode plot of the power stage (C_{trl} node to V_{out}). Fig. 9 displays the results. Please note that while the component values used in simulating the Fig. 8 schematic are not shown, these values are representative of a practical application.

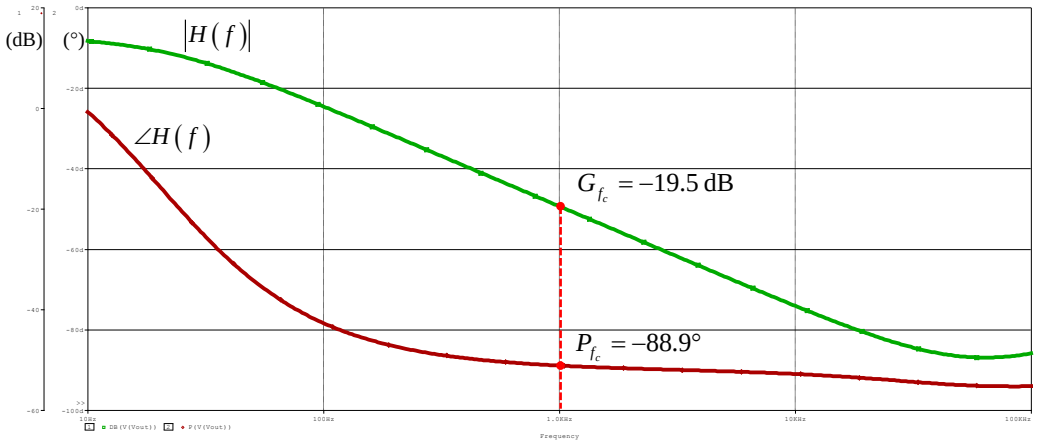

Fig. 9. Power stage transfer function.

Let's select a crossover frequency f_c at 1 kHz. This is a good tradeoff between a quick transient response and good noise immunity. The right half-plane zero (RHPZ) present in a DCM current-mode flyback converter is far away and does not bother us. At this cutoff frequency, the power stage attenuation is measured as 19.5 dB and the phase as -88.9°.

As the feedback signal is built from the auxiliary winding, we need to build the same Bode plot with the output observed on the V_{aux} node (Fig. 10.) The phase shape is not changed but the magnitude curve is affected by the transformer turns ratio:

$$G_{diff} = 20\log\left(\frac{N_{PA}}{N_{PS}}\right) = 20\log\left(\frac{0.083}{0.123}\right) = -3.4\,\text{dB} \qquad (1)$$

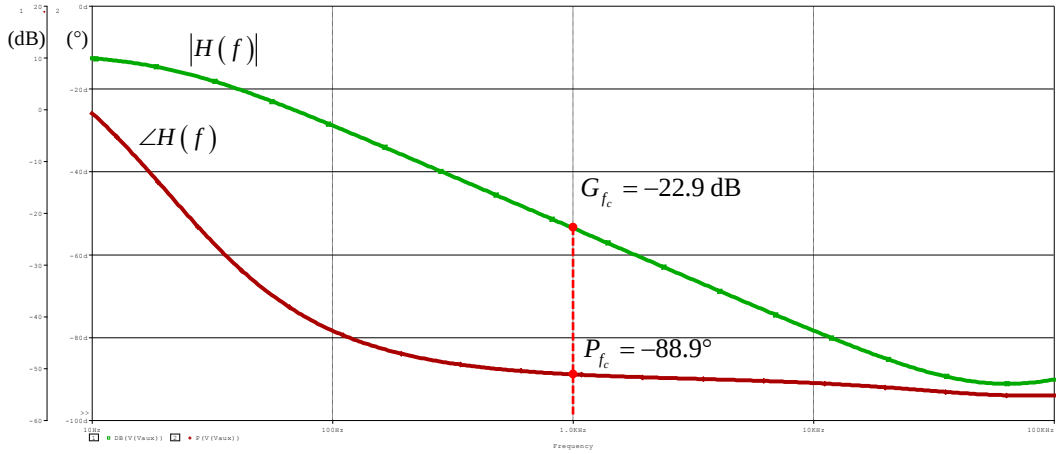

Fig. 10. Transfer function observed on the auxiliary winding.

Using this average model configuration, all components present on the output are automatically reflected to the auxiliary winding. Here, both diodes have negligible dynamic resistances and are treated as short circuits.

Simplification Of The Power Stage Average Model

The next step will consist of simplifying the schematic and reducing the number of components without altering the transfer function. Looking at the schematic in Fig. 8, we see three windings: the first one is the primary winding, the second is related to the power delivery (secondary power winding) and the third one is used for output voltage measurement. It is also designed to supply the controller (auxiliary winding.)

Since the final goal is to plot the open-loop transfer function, we will try to simplify the transformer with a single secondary-side winding. All Bode plots will not be shown in this article but the first step was to remove the IC consumption resistance and then the V_{CC} capacitor. The last possible simplification is to reflect the components connected to the secondary side to the auxiliary winding.

Let's focus our attention around the transformer as shown in Fig. 11. Compared to Fig. 8, the number of components connected to the auxiliary winding is now limited to the ZCD pin bridge resistances. The turns ratios linking the primary to the power secondary and auxiliary windings are respectively labeled N_{PS} and N_{PA}

where $N_{PS} = \frac{N_S}{N_P}$ and $N_{PA} = \frac{N_{aux}}{N_P}$.

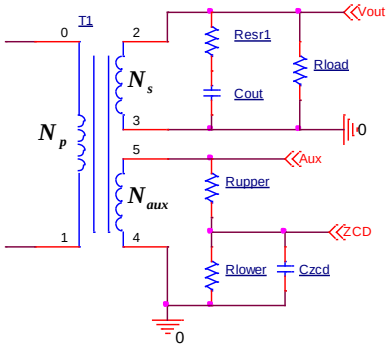

Fig. 11. The transformer and secondary components. Simplifying this schematic will allow us to simply the power stage average model.

To clarify what we're doing, we will divide this exercise into two steps. First, the output capacitor and resistive load are reflected to the primary side as illustrated in Fig. 12. Then later, these elements will be reflected from the primary to the auxiliary winding.

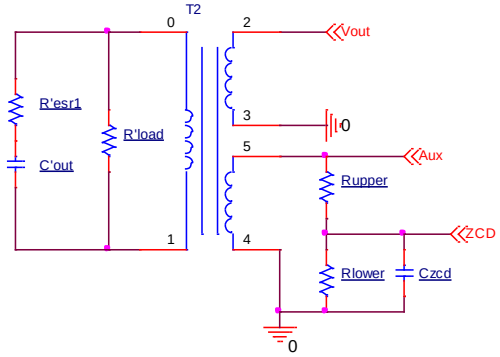

Fig. 12. Output capacitor and load reflected to the primary side.

Reflecting Components Around The Transformer

How can these components be reflected across the transformer if we treat the circuit components as ideal, particularly allowing the diodes to have a 0-Ω dynamic resistance? Let's have a look at the equation around an ideal transformer drawn in Fig. 13.

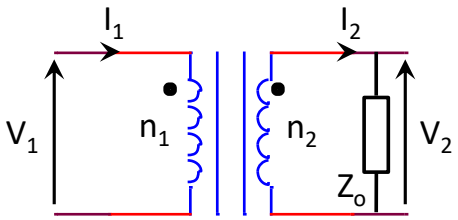

Fig. 13. Ideal transformer.

$$N = \frac{n_2}{n_1} = \frac{V_2}{V_1} = \frac{I_1}{I_2} \quad (2)$$

Ohm's law gives us a chance to write:

$$Z_o = \frac{V_2}{I_2} \quad (3)$$

Rearranging (2), we know that:

$$V_2 = NV_1 \quad (4)$$

$$I_2 = \frac{I_1}{N} \quad (5)$$

Substituting (4) and (5) into (3):

$$Z_o = \frac{NV_1}{\frac{I_1}{N}} = \frac{V_1}{I_1} N^2 = Z_i N^2 \quad (6)$$

Input impedance Z_i can be extracted:

$$Z_i = \frac{Z_o}{N^2} \quad (7)$$

Now that the relationship between the load and its reflected equivalent is established, we can easily apply it to our schematic in Fig. 12 where

$$R'_{load} = \frac{R_{load}}{N_{PS}^2} \quad (8)$$

$$R'_{esr1} = \frac{R_{esr1}}{N_{PS}^2} \quad (9)$$

$$C'_{out} = C_{out} N_{PS}^2 \quad (10)$$

By applying the same method, we can now move the impedance from the primary side to the auxiliary winding using the new turns ratio (N_{PA}):

$$R''_{load} = R_{load}\frac{N_{PA}^{\ 2}}{N_{PS}^{\ 2}} \tag{11}$$

$$R''_{esr} = R_{esr}\frac{N_{PA}^{\ 2}}{N_{PS}^{\ 2}} \tag{12}$$

$$C''_{out} = C_{out}\frac{N_{PS}^{\ 2}}{N_{PA}^{\ 2}} \tag{13}$$

We can update Fig. 8 according to the previous simplification. The result is shown in Fig. 14.

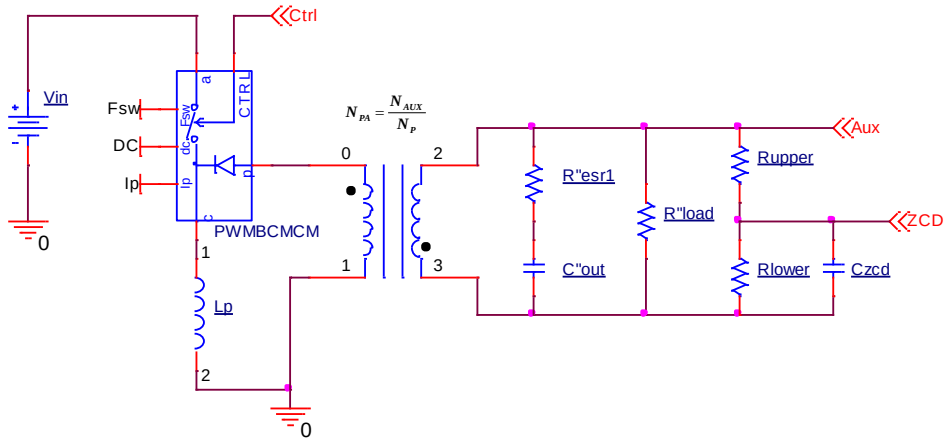

Fig. 14. Simplified PWM switch model.

The corresponding Bode plot is shown in Fig. 15. The magnitude and phase curve of the original schematic have been superposed (dashed red trace for the gain and dashed blue trace for the phase). Both curves are identical.

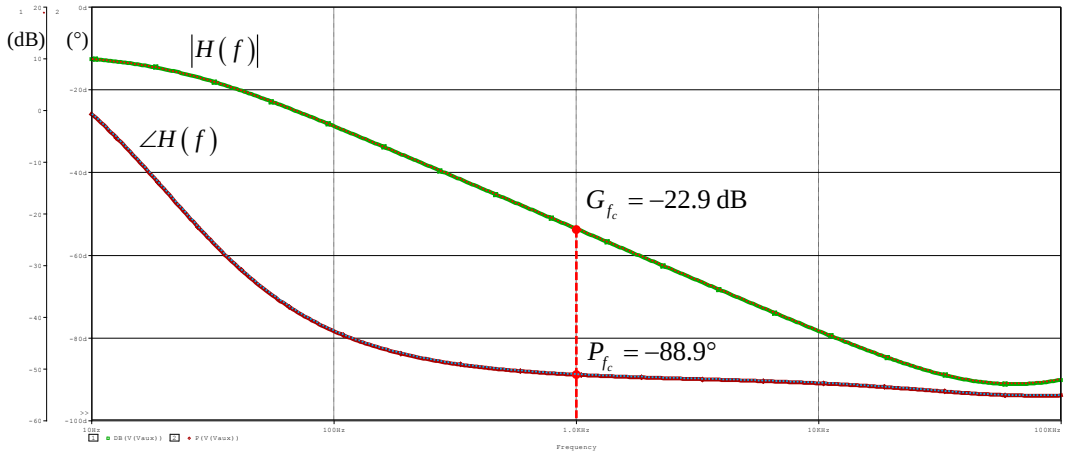

Fig. 15. Transfer function (Ctrl node to Vaux) obtained with the simplified schematic.

Sample-And-Hold Network In The Power Stage

The last part that needs to be introduced in the power stage is the sample-and-hold network. Indeed, as explained at the beginning of this article, the constant voltage regulation depends on this network being inserted between the ZCD pin and the OTA.

A sample-and-hold network transfer function can be modeled in the frequency domain by a zero-order hold (ZOH). The ZOH transfer function T_{ZOH} can be described by the following Laplace transform expression:

$$T_{ZOH}(s)=\frac{1-e^{-sT_{sw}}}{sT_{sw}} \quad (14)$$

In (14), we can identify the numerator as the original signal plus an inverted delayed signal. The denominator is an integration function. Following reference [3], the equivalent circuit in Fig. 16 can be assembled. Please note that this circuit cannot deliver a dc component and can only be used for a pure ac analysis.

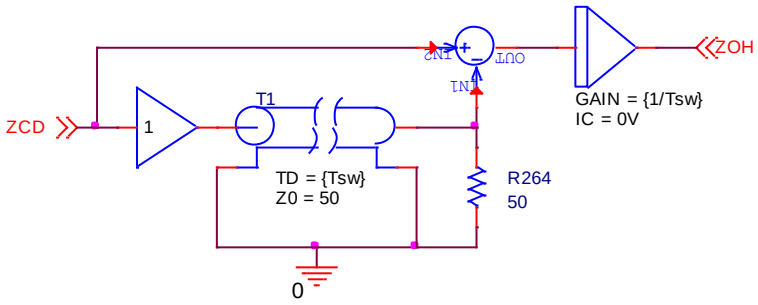

Fig. 16. ZOH modeling with delay line plus an integrator.

By including the ZOH in our primary-regulated converter, we have completed the conversion chain and we can update our average model (Fig. 17.)

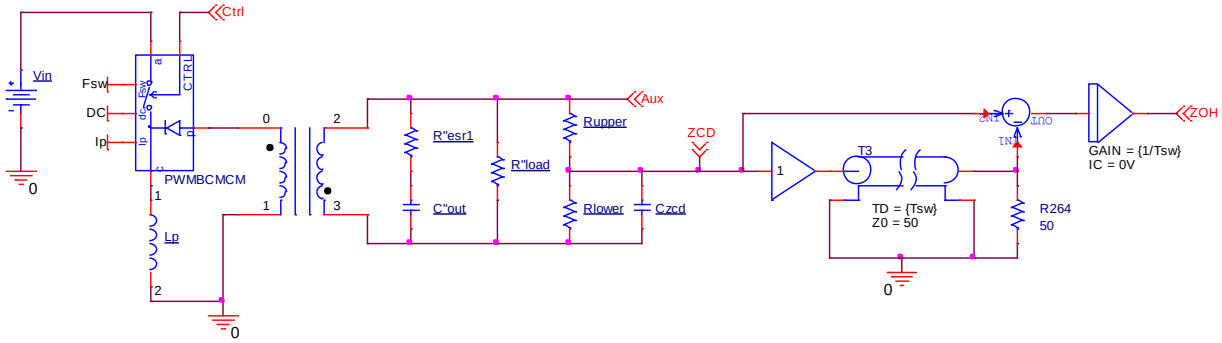

Fig. 17. Average model of the power stage including the sample-and-hold network.

The Ctrl node to ZOH output gain and phase curves can be plotted as in Fig. 18. At the selected crossover frequency (i.e. 1 kHz), the gain and phase can be extracted. Both values will be needed to dimension the compensation network.

$$G_{Fc}=-32.8\,\text{dB} \quad (15)$$

$$P_{Fc}=-91.4° \quad (16)$$

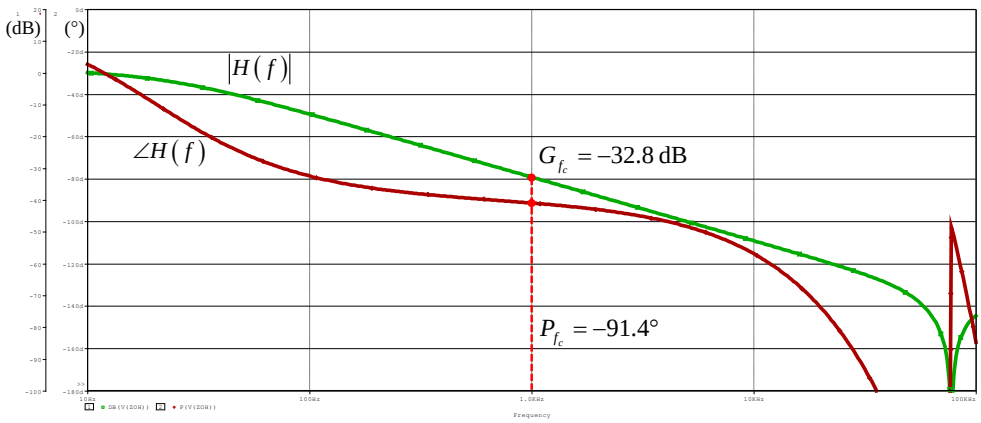

Fig. 18. Transfer function of the power stage now including the internal sample-and-hold network.

Derivation Of Control-To-Output Transfer Function

Now that we have determined the proper simulation architecture, we need to determine an expression for the control-to-output transfer function. The power stage will be divided in several parts. Then each individual transfer function will be computed and then multiplied to form the complete power stage response.

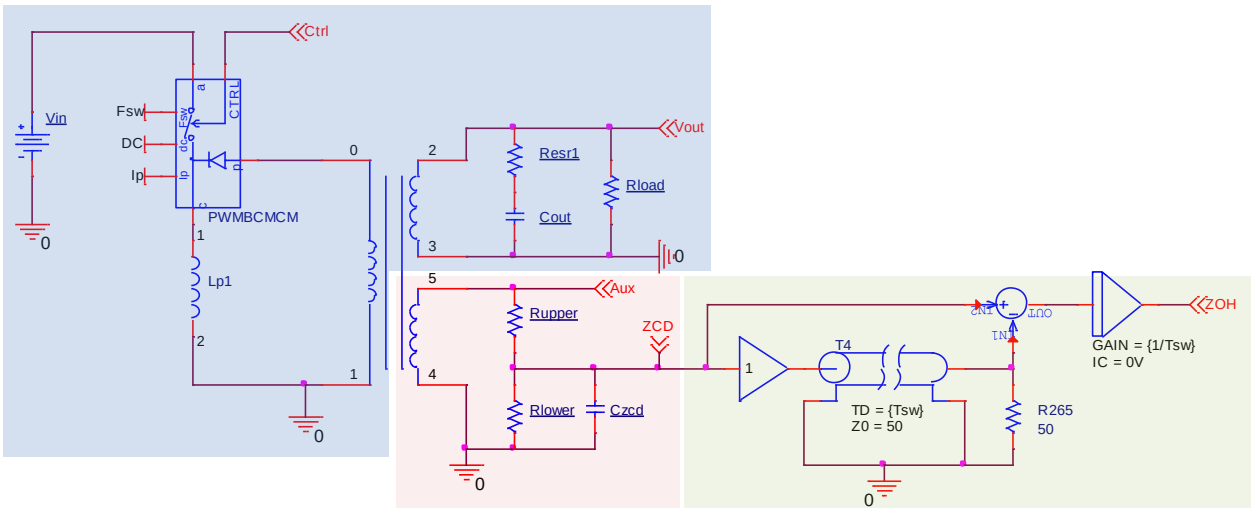

Fig. 19. The power stage is divided into three main sections—the power stage, the auxiliary winding structure, and the sample-and-hold network.

Let's start with the power stage only, considering the control voltage (V_{ctrl}) to the output voltage V_{out}. The transfer function of a borderline (or boundary) conduction mode (BCM or QR for quasi-resonant) current-mode flyback converter is:

$$H_1(s)=\frac{V_{out}(s)}{V_{ctrl}(s)}=H_0\frac{\left(1+\frac{s}{s_{z_1}}\right)\left(1-\frac{s}{s_{z_2}}\right)}{\left(1+\frac{s}{s_{p_1}}\right)} \qquad (17)$$

By using the loss-free network concept described in reference [1], we can identify:

$$H_0 = \frac{R_{load}}{2K_{comp}N_{PS}R_{sense}\left(2\frac{V_{out}}{N_{PS}V_{in}}+1\right)} \quad (18)$$

$$f_{p_1} = \frac{1}{2\pi R_{load}C_{out}}\frac{2\frac{V_{out}}{N_{PS}V_{in}}+1}{\frac{V_{out}}{N_{PS}V_{in}}+1} \quad (19)$$

$$f_{z_1} = \frac{1}{2\pi R_{esr}C_{out}} \quad (20)$$

$$f_{z_2} = \frac{R_{load}}{{N_{PS}}^2 2\pi L_p}\frac{1}{\frac{V_{out}}{N_{PS}V_{in}}\left(1+\frac{V_{out}}{N_{PS}V_{in}}\right)} \quad (21)$$

Please note the parameter K_{comp} in the dc gain H_0 is related to the internal divider between the OTA output and the control voltage.

The ac response shown in Fig. 20 is obtained by plugging equation 17 into a Mathcad sheet. The values used are the same ones used in the SPICE simulation of Fig. 9. The magnitude and phase curves of the simulation file depicted in the first part of this article (Fig. 9—dashed blue trace for the gain and dashed red trace for the phase) are a perfect match.

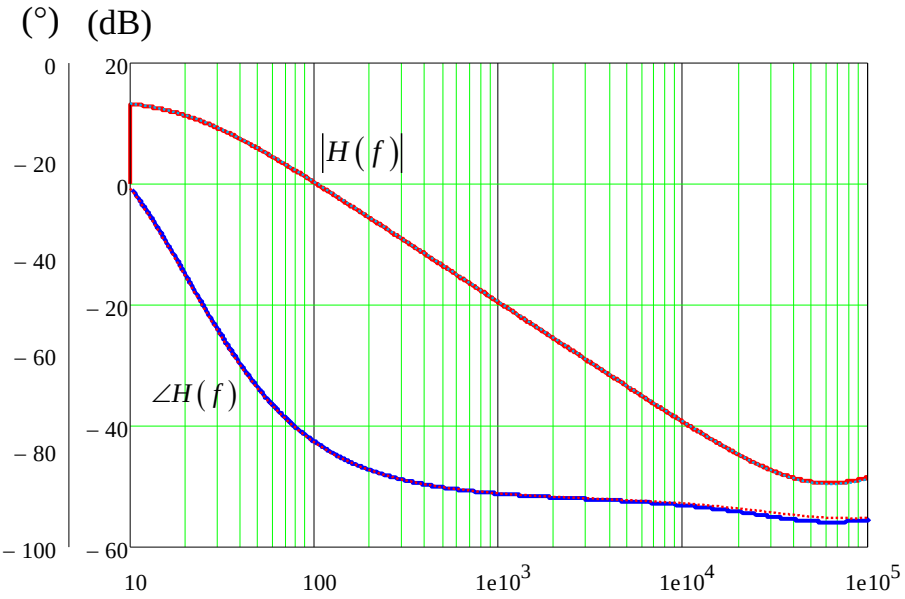

Fig. 20. Power stage transfer function plots generated using Mathcad.

The impact of the transformer is easy to calculate. It is a dc gain called K_{T0} linked to the turns ratio between the primary and the secondary N_{PS} and between the primary and the auxiliary winding N_{PA}:

$$K_{T0} = \frac{N_{PA}}{N_{PS}} \tag{22}$$

The next step is related to the red frame in Fig. 19. The network used to adjust the output voltage is performed by the R_{upper} and R_{lower} resistances plus the filtering capacitor C_{ZCD}. This capacitor is adjusted to turn the MOSFET on when the drain-source voltage is at its minimum thus reducing switching losses. The transfer function of the network can be easily calculated by using the Fast Analytical Techniques described in [4]:

$$K_D(s) = K_{D0}\frac{1}{1+s\tau_1} \tag{23}$$

where $K_{D0} = \frac{R_{lower}}{R_{lower}+R_{upper}}$ and $\tau_1 = \frac{R_{lower}R_{upper}}{R_{lower}+R_{upper}}C_{ZCD}$.

The last block is related to the sample-and-hold network that we already tackled above. It enters the equation as a multiplicand as shown below**.**

$$H_3(s) = H_1(s)K_{T0}K_D(s)T_{ZOH}(s) = K_{T0}H_0K_{D0}\frac{\left(1+\frac{s}{s_{z_1}}\right)\left(1-\frac{s}{s_{z_2}}\right)}{\left(1+\frac{s}{s_{p_1}}\right)}\frac{1}{1+s\tau_1}\frac{1-e^{-sT_{sw}}}{sT_{sw}} \tag{24}$$

The last step and the most important one is to check that both Mathcad and simulation responses are identical. The curves appear in Fig. 21.

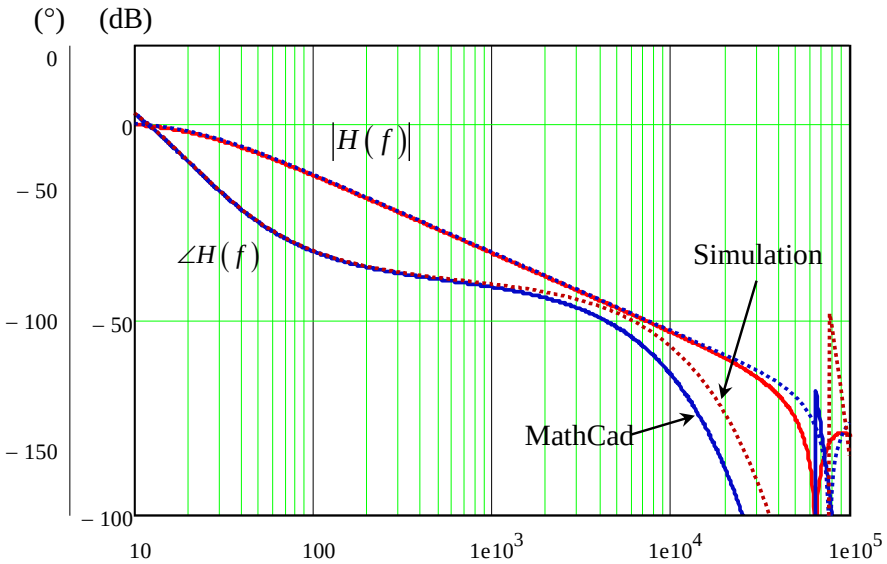

Fig 21. Power stage ac response including the internal ZOH block.

We can see that the magnitude curves are identical up to 20 kHz. The addition of the ZOH contribution clearly appears beyond 2 kHz where a noticeable deviation shows up in the phase. The compensation exercise will not be affected by these deviations as we plan to fix the crossover frequency around 1 kHz. From the graph, we can extract the numbers below,

$$G_{Fc} = -33.0\,\text{dB} \tag{25}$$

$$P_{Fc} = -92.5° \quad (26)$$

which are to be compared with the measurement done with the simulation model:

$$G_{Fc} = -32.8\,\text{dB} \quad (27)$$

$$P_{Fc} = -91.4° \quad (28)$$

Now we have a match between a SPICE simulation and a Mathcad analysis, we can look at the compensation strategy. The compensation of our primary-side-regulated controller is done around an OTA. Looking at the open-loop phase response at the selected crossover frequency, we see there is a need for some phase boost to meet the minimum requirement of a 45° phase margin. The type-1 compensation only affects the magnitude curve and does not provide phase boost. Therefore the study that follows will thus focus on the type-2 architecture.

Transfer Function Of OTA With Type-2 Compensation

A typical OTA configuration appears in Fig. 22 where the output drives a capacitor connected in parallel with an RC network.

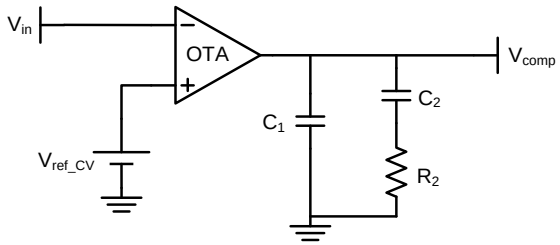

Fig. 22. OTA with type-2 compensation.

Let's start by calculating the impedance offered by the three passive components: C_1 in parallel with the series connection of C_2 and R_2:

$$Z_{eq}(s) = \frac{\frac{1}{sC_1}\left(R_2 + \frac{1}{sC_2}\right)}{\frac{1}{sC_1} + R_2 + \frac{1}{sC_2}} \quad (29)$$

By developing and rearranging, we have

$$Z_{eq}(s) = \frac{1 + sR_2C_2}{s(C_1 + C_2)\left(1 + sR_2\frac{C_1C_2}{C_1 + C_2}\right)} \quad (30)$$

One more step to format the equation is to factor sR_2C_2 in the numerator:

$$Z_{eq}(s) = \frac{R_2C_2}{C_1 + C_2}\frac{1 + \frac{1}{sR_2C_2}}{1 + sR_2\frac{C_1C_2}{C_1 + C_2}} \quad (31)$$

The output current flowing out of the OTA is the differential input voltage affected by the transconductance parameter g_m:

$$I_{out(OTA)} = (V_+ - V_-)\, g_m \tag{32}$$

In Laplace notation, the reference voltage is fixed and its small-signal response is 0 V. Therefore

$$I_{out(OTA)}(s) = -V_{in}(s)\, g_m \tag{33}$$

Applying Ohm's law, we can write:

$$V_{comp}(s) = I_{out(OTA)} Z_{eq}(s) \tag{34}$$

Substituting (31) and (33) in (34) implies:

$$V_{comp}(s) = -V_{in}(s)\, g_m \frac{R_2 C_2}{C_1 + C_2} \frac{1 + \dfrac{1}{sR_2 C_2}}{1 + sR_2 \dfrac{C_1 C_2}{C_1 + C_2}} \tag{35}$$

From (35), we extract the transfer function:

$$\frac{V_{comp}(s)}{V_{in}(s)} = G(s) = -\frac{g_m R_2 C_2}{C_1 + C_2} \frac{1 + \dfrac{1}{sR_2 C_2}}{1 + sR_2 \dfrac{C_1 C_2}{C_1 + C_2}} \tag{36}$$

From this expression, we can identify the mid-band gain G_0, the zero and the pole:

$$G_0 = \frac{g_m R_2 C_2}{C_1 + C_2} \tag{37}$$

$$\omega_z = \frac{1}{R_2 C_2} \tag{38}$$

$$\omega_p = \frac{1}{R_2 \dfrac{C_1 C_2}{C_1 + C_2}} \tag{39}$$

Now, we need to define the position of the pole and zero so that the open-loop gain crosses 0 dB at the cutoff frequency with the expected phase margin. Several tools can be used to build the compensation network like the manual placement offered in [4] or the "k factor" method introduced by Dean Venable in the 90s.[5] The second solution will be used for this article. It consists of determining the position of zero and the pole with respect to the crossover frequency so that adequate phase boost is produced. The number k is defined by:

$$k = \tan\left(\frac{boost}{2} + 45°\right) \tag{40}$$

where the *boost* parameter is the needed compensation phase boost determined as:

$$Boost = PM - PS - 90° \quad (41)$$

In this equation:

- PM is the desired phase margin at selected crossover frequency f_c
- PS is open-loop phase of the converter at the selected crossover frequency f_c
- -90° is incurred by the origin pole.

The pole and zero locations can be now calculated like the compensation network:

$$f_z = \frac{f_c}{k} \quad (42)$$

$$f_p = kf_c \quad (43)$$

$$C_1 = \frac{1}{2\pi R_2 f_p} \quad (44)$$

$$C_2 = \frac{1}{2\pi R_2 f_z} \quad (45)$$

$$R_2 = \frac{G_0 (C_1 + C_2)}{g_m C_2} \quad (46)$$

If we consider, $C_1 << C_2$, R_2 becomes:

$$R_2 = \frac{G_0}{g_m} \quad (47)$$

Numerical Example

Let's apply these formulas to our design goal of a 1-kHz crossover frequency with a 70° phase margin. Our design data are the following:

$$f_c = 1\,\text{kHz}$$
$$PM = 70°$$
$$PS = -92.5°$$
$$G_{f_c} = -33\,\text{dB}$$
$$G_0 = 10^{\frac{-G_{fc}}{20}} = 10^{\frac{-(-33))}{20}} = 44.7$$

From these values, we can calculate:

$$Boost = 70 - (-92.5) - 90 = 72.5° \quad (48)$$

$$k = \tan\left(\frac{72.5°}{2} + 45°\right) = 6.5 \quad (49)$$

Now that the *k*-factor is known, the pole and zero frequency can be evaluated:

$$f_z = \frac{1000}{6.5} = 154\ \text{Hz} \tag{50}$$

$$f_p = kf_c = 6.5 \times 1000 = 6.5\ \text{kHz} \tag{51}$$

Finally, we can calculate the type-2 compensation network component values:

$$R_2 = \frac{44.7}{200\mu} = 223.5\ \text{k}\Omega \tag{52}$$

$$C_1 = \frac{1}{2\pi \times 223.5k \times 154} = 4.62\ \text{nF} \tag{53}$$

$$C_2 = \frac{1}{2\pi \times 223.5k \times 6.5k} = 110\ \text{pF} \tag{54}$$

The normalized values will be 220 kΩ for R_2, 4.7 nF for C_1 while C_2 will equal 120 pF. The Mathcad dynamic response appears in Fig. 23. The crossover frequency is measured as 960 Hz with a 69.8° phase margin.

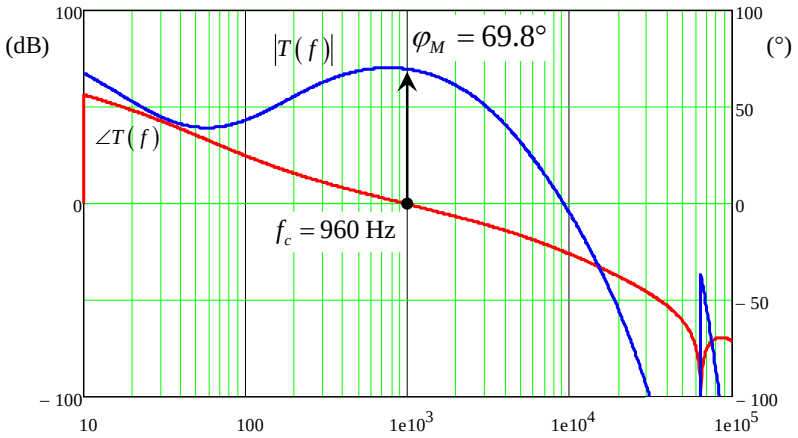

Fig. 23. Ac response generated in Mathcad for a converter with a type-2 compensation network.

The final step is to compare these curves to the simulation model. The following schematic in Fig. 24 shows the OTA with the type-2 compensation consisting of C_1, C_2 and R_2. The compensation loop is broken between the comp signal and the internal K_{comp} divider in order to inject the ac modulation.

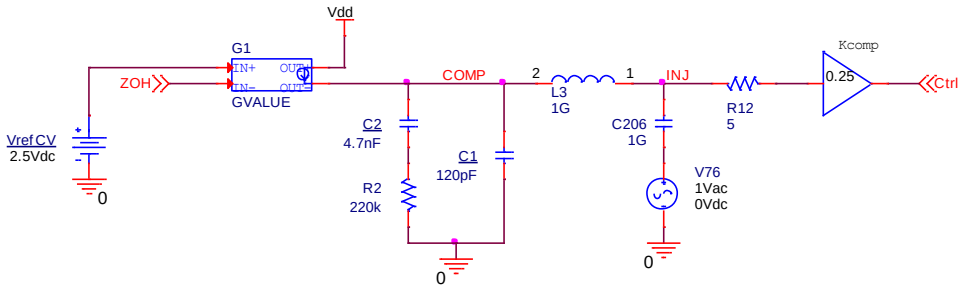

Fig. 24. Type-2 compensation schematic with the internal K_{comp} divider.

We can now import this schematic into the power stage schematic presented in Fig. 17 to obtain the complete open-loop gain of the converter. This is what Fig. 25 shows.

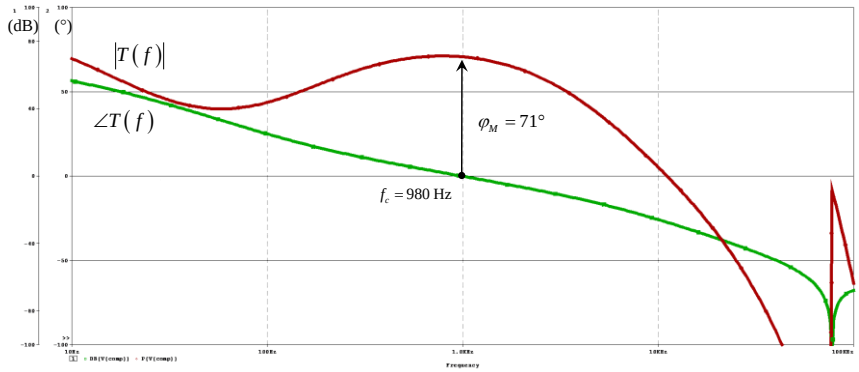

Fig. 25. PSpice open-loop gain of the BCM flyback converter operated in PSR mode

The crossover frequency and the corresponding phase margin are almost identical between the Mathcad file implementing the transfer function and the simulation model, which confirms the validity of our approach.

Practical Application

A PSR converter based on the NCP1365 has been assembled as shown in Fig. 26. The component values calculated in above have been adopted for the compensation section and soldered onto the board. The 5-V output is subject to a load step from 1 A to 2 A in 1 µs. As confirmed by Fig. 27, the transient response is excellent regardless of the input voltage.

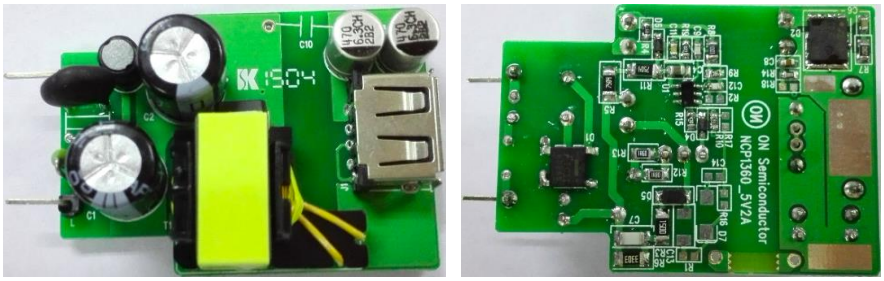

Fig. 26. A PSR board using ON Semiconductor's NCP1365 has been assembled. It delivers 5 V and up to 2 A of output current.

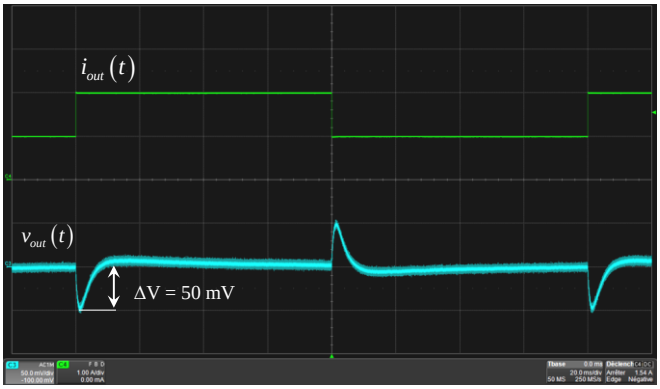

Fig. 27. The transient response measured at low- and high-line conditions confirms the excellent stability of the converter.

Conclusion

This article has addressed two mains topics: operation of the flyback converter under primary-side regulation and use of the power stage average model to analyze its operation. We have progressed in the modeling process by first simulating a simple QR power stage to which we have added an auxiliary winding. Finally, the sample-and-hold circuit has been brought in to complete the picture.

With modern primary-side-regulated controllers, the difference between the classical flyback topology and the PSR lies in the way the regulation is performed. With a carefully-designed transformer, the performance in regulation and stability is very close to that of an optocoupler-based power supply.

In the second part of this article, we showed the calculation of the transfer function of a primary-side regulated converter with the integration of the internal sample-and-hold network within the controller IC. Thanks to the Mathcad software, we were able to build the Bode plot from the transfer function and compare it to the simulation model presented earlier in the article. Both waveforms showed similar results.

Finally, the needed compensation network has been defined and dimensioned to match the phase margin requirement. Thanks to this article, you are able to design the type-2 compensation network for a converter using PSR. Of course, the same method can be used for other topologies like those used to implement power factor correction.

Practically speaking, some PSR controllers are internally compensated so the designer does not have this design option. But with the ON Semiconductor PSR controller cited in this article (and others that may follow), the ability to design the external compensation network through modeling will eliminate the trial and error approach that designers may have relied on previously.

References

1. "Switch-Mode Power Supplies: SPICE Simulations and Practical Designs" 2nd edition by Christophe Basso, McGraw-Hill, New-York, 2012.
2. "Simplified analysis of PWM converters using the model of the PWM switch, parts I (CCM) and part II (DCM)" by Vatché Vorpérian, Transactions on aerospace and electronics systems, vol. 26, no. 3, May 1990.
3. "Generic average modeling and simulation of discrete controllers" by Daniel Adar and Sam Ben-Yaakov, Applied Power Electronics Conference, 2001.
4. "Linear Circuit Transfer Functions: an Introduction to Fast Analytical Techniques" by Christophe Basso, Wiley, 2016.
5. "The k-Factor: A New Mathematical Tool for Stability Analysis and Synthesis" by Dean Venable, Proceedings of Powercon 10, 1983, pp 1-12.

About The Author

Yann Vaquette has been an application engineer at ON Semiconductor in Toulouse, France since 2011.In this role he has developed several switching controllers dedicated to the flyback topology. After working on the design of high-frequency quasi-resonant flyback converters, he has developed a high-density version of a 45-W notebook adapter. He now handles the primary-side regulated controllers family dedicated to travel adapter applications. Yann graduated from the CESI engineering school. During his study, Yann worked part time with ON Semiconductor in Toulouse for three years before being hired as an application engineer in the ac-dc business unit.

For further reading on modeling flyback converters, see the How2Power Design Guide and do a keyword search on "primary side regulation".