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Circumventing Loss In An RC Circuit Leads To More Efficient Power Converters

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The charging of a capacitor in a simple RC loop incurs losses in the resistive portion of the circuit. However, the efficiency of the charging circuit varies widely with the initial voltage on the capacitor at the start of charging. If the capacitor in question is a supercapacitor, which results in long time constants, we can take advantage of this relationship between circuit efficiency and capacitor voltage fact to create novel ac-dc converters with improved efficiency.

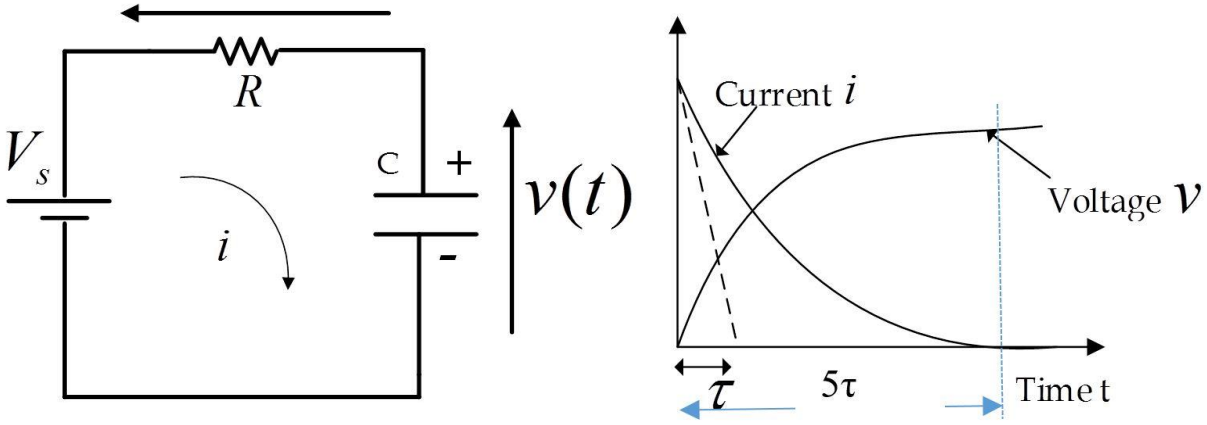
After reviewing the behavior of the simple RC circuit with supercapacitors, this article describes two novel ways in which the RC circuit can be combined with power converters to negate the resistive loss of the RC circuit. One approach replaces the resistive part of the circuit with a useful resistance, which could be a loaded dc-dc converter or voltage regulator. The other approach places a supercapacitor ahead of a linear voltage regulator as a lossless voltage dropper, which improves the regulator's efficiency by minimizing its input voltage.

This linear regulator technique has been dubbed the supercapacitor-assisted low dropout regulator (SCALDO). After explaining the key principles of operation of a SCALDO, we present a prototype implementation to demonstrate its performance.

A Quick Review Of Basic RC Loop Behavior

A simple RC circuit powered by an ideal voltage source was an important subject where we spent several hours to a few days during our undergraduate courses in electrical or electronic engineering. The RC time constant, exponential charging curve for the capacitor voltage versus time, gradually decaying loop current starting from V/R, decaying down to zero within five time constants were some essential basic topics our professors wanted us to learn and apply.

So what is so fancy about re-visiting that simple circuit? Let us start with the simple basics of the electrical physics textbook. Fig. 1 shows this simple circuit, where the capacitor starts from a zero initial charge. At the end of approximately 5τ seconds, where τ is the circuit time constant (RC), the capacitor reaches the full voltage V, with an accumulated energy of $0.5CV^2$.



(a) (b)

Fig. 1. Behavior of the simple RC circuit (a) is depicted with the familiar graph of capacitor voltage and loop current versus time (b).

A not so obvious fact about this circuit is that the resistor in the loop dissipates the same amount of energy as the stored energy in the capacitor, if the capacitor started charging from zero voltage. So this circuit could be 50% efficient in charging an ideal capacitor. It is very important to visualize that the charging efficiency is not dependent on the ohmic value of the loop resistance. Whether the resistance is large or small the 50% loss remains the same.

As shown in Fig. 1b, to charge the capacitor fully it takes a little more than five time constants (5 τ), and the current in the loop starts from V/R decaying down to zero in the same time period. If the capacitor and resistor are 1 µF and 1 Ω respectively, the time constant is 1 µs. Now, if the capacitor is changed from 1 µF to 1 F, which is a small value supercapacitor, with a loop resistance of 1 Ω, the time constant becomes 1 second and 5 τ = 5 seconds. In this case you can plot the behavior of the capacitor charging using your wristwatch!

Now let us move into a more detailed discussion about this RC circuit that is relevant to our diode-capacitor based ac-dc converters. In simple ac-dc converters, the capacitor does not discharge down to zero during a half cycle of the ac mains waveform and in general our diode-capacitor-combination-based ac-dc converters achieve high efficiency, by maintaining the average capacitor voltage at a relatively high value such as 85% to 95% of the peak ac voltage.

Now let us look at the case of a generalized RC circuit. In Fig. 2 the capacitor is rated for V_{Cpeak} and the input voltage source voltage is at V_s where $V_s > V_{Cpeak}$. If we analyze this circuit, we will see that the capacitor charging efficiency varies over a huge range.

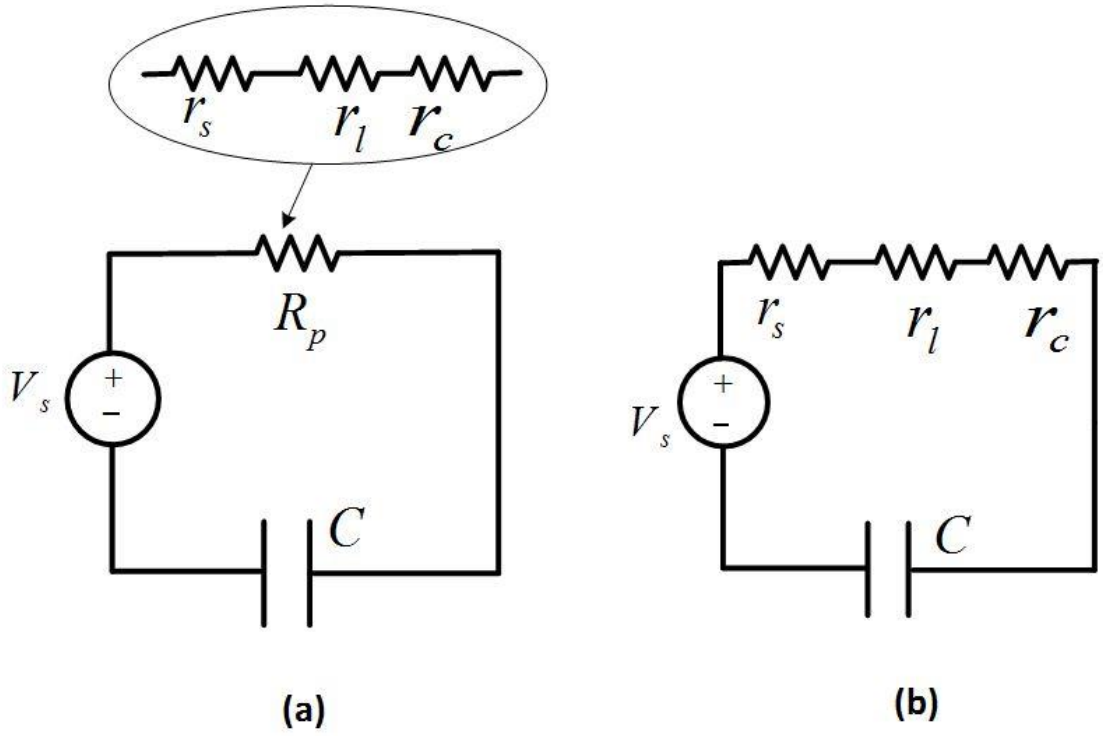


Fig. 2. Generalized capacitor charging circuit leading to results in Table 1. In the basic circuit (a), the total parasitic resistance R_p can be broken down into three parts consisting of source internal resistance, r_s, loop resistance, r_l, and the equivalent series resistance (ESR) of the capacitor r_c, as shown in (b).

Without detailing the analytical steps of math, capacitor charging efficiency will vary with the source voltage as well as the pre-charge voltage of the capacitor as per the details in Table 1. You might wonder why we use the condition of $V_s > V_{Cpeak}$, which means we will allow the capacitor to overcharge and kill itself! But in

supercapacitor-based circuits, where the time constant is very large, we can practically use that configuration, with a voltage monitoring circuit to stop overcharging the capacitor.

As we see from Table 1, the efficiency of a capacitor charging circuit can vary over a wide range, where charging efficiency increases with the capacitor starting with a non-zero initial voltage. In our simple ac-dc converters, we can practically use this property to maintain a good conversion efficiency, by not allowing the smoothing capacitor to discharge to low values. In the simple RC loop circuit shown in Fig. 2, resistive loss is contributed by three components: internal resistance of the energy source (r_s), total resistances of connecting components between source (r_l) and capacitor and the equivalent series resistance (r_c) of the capacitor.

If a designer deeply concentrates on the wasted energy in the RC loop, creative new design approaches to circumvent this problem can be achieved. The tip of the iceberg of this approach is presented in the next part of this article.

Table 1. Capacitor charging efficiency for the circuit in Fig. 2 at different source voltages for a capacitor final voltage of 10 Vdc.

DC source voltage (V_S)	Initial capacitor voltage ($V_{Cinitial}$)	Percentage charging efficiency (η)
10	0	50
10	2	60
10	5	75
10	8	90
10	9	95
10	10	100
12	9	79
12	5	63
12	0	42
15	0	33

Novel Approaches To Overcoming Energy Losses In An RC Loop

Based on the concepts described above, two novel approaches for designing high-efficiency converters within the simple RC loop have emerged:

- Inserting a useful resistance within the loop to circumvent the resistive loss
- Using a very large capacitor as a lossless dropper.

We will explore each of these concepts in the following sections.

Inserting A Useful Resistance In The RC Loop

If one looks at the case in Fig. 2, and modifies the case by inserting a "*useful resistance*" into the loop, as in Fig. 3, we can achieve some significant efficiency gains in capacitor charging. Here we make the useful resistance, R_L absorb a significant part of the dissipation within the three parasitic elements in Fig. 2b. This useful resistance could be a heater, a resistively loaded dc-dc converter, a loaded inverter or an LED lamp load.

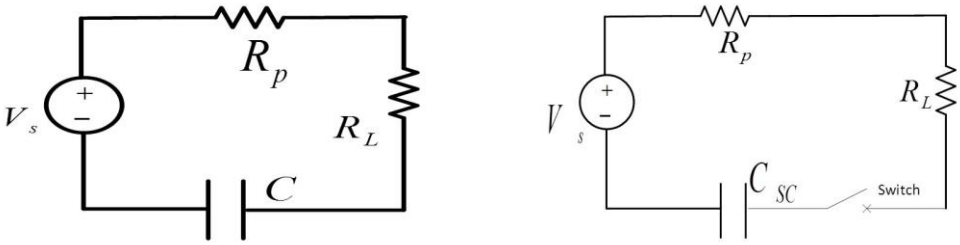


Fig. 3. Insertion of a useful resistive load in the capacitor charging loop to increase the charging efficiency of a simple circuit (a) where R_p is the parasitic loop resistance and R_L is the inserted useful load. An additional switch can be inserted to prevent overcharging the capacitor (b), when the dc source voltage is higher than the rated dc voltage of the capacitor (applicable to the case of a supercapacitor used in the circuit).

In Fig. 3a this resistance R_L and the combined "unavoidable parasitic resistances," (r_s, r_l and r_c), are shown as a single resistance R_p. In a circuit of this nature, if the ratio R_L/R_p is large, we could move the losses in parasitic resistances into the useful load to achieve an overall efficiency larger than in the case of Fig. 2 and Table 1.

Table 2 depicts this efficiency gain in Fig. 3, where the efficiency is calculated by combining the capacitor charge and the consumption in the useful load, which are considered as one single useful quantity.

Table 2. Overall efficiency of powering a useful load within the loop while charging a capacitor.

DC source voltage – (VS)	Ratio $\frac{R_L}{R_p}$	Final voltage of capacitor (V_C peak)	Initial capacitor voltage (V_C initial)	Percentage efficiency- η
10	1:1	10	0	50
10	1:1	10	2	60
10	1:1	10	5	75
10	1:1	10	8	90
10	1:1	10	9	95
10	9:1	10	10	100
12	9:1	10	9	79
12	9:1	10	5	63
12	9:1	10	0	42
15	9:1	10	0	33

Fig. 3b is an extension of the case in Fig. 3a where we could use a very large capacitor (such as a supercapacitor) with a switch, to avoid any possible overcharge, when the source voltage could exceed the rated dc voltage of the capacitor. With the availability of supercapacitors (SCs) (which are also known as ultracapacitors or electrical double layer capacitors (EDLCs)), in the range of 1 F to 7500 F in a single cell, we can come up with very large time-constant circuits.

The circuit configuration in Fig. 3b is quite practical with an added switch to stop overcharging the SC. The last few rows of Table 1 are applicable to the case in Fig. 3b, where the dc source voltage is higher than the maximum rated voltage of the capacitor, which is 10 V dc in this case.

Fig. 4 depicts, in a generalized way, this loss minimization approach based on some useful loads being inserted into the RC loop. In this case we take an example where the dc power source is m times larger than the maximum capacitor voltage, and, the capacitor commences its charging from an initial voltage higher than 0 V, where *k* is the ratio of capacitor initial voltage to capacitor maximum (rated) voltage. Ratio *m* is always larger than one and *k* is always less than one.

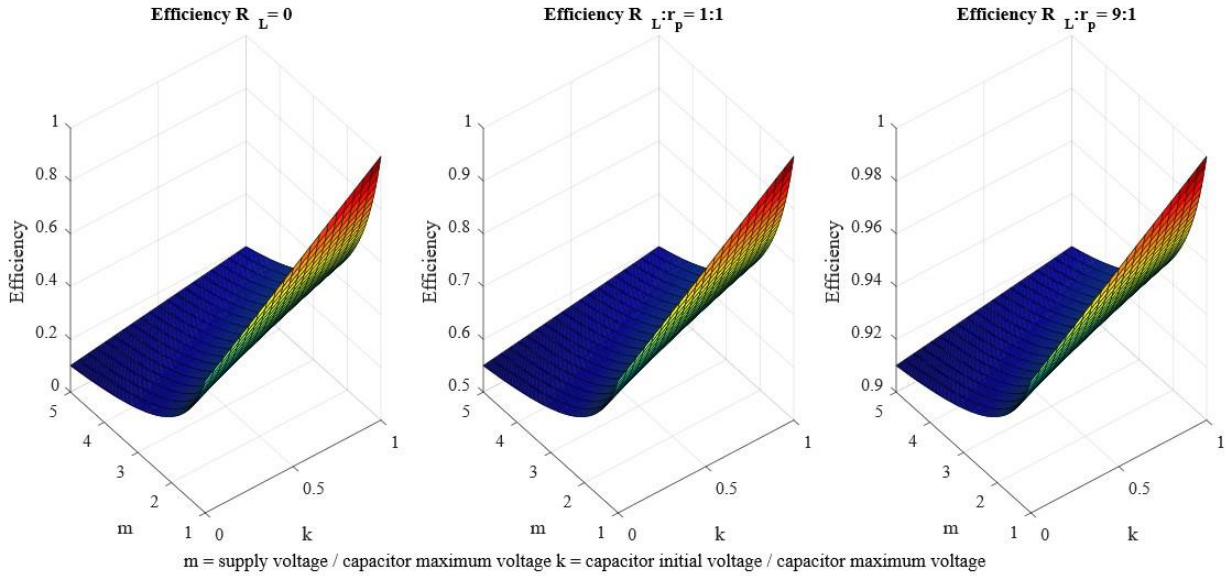
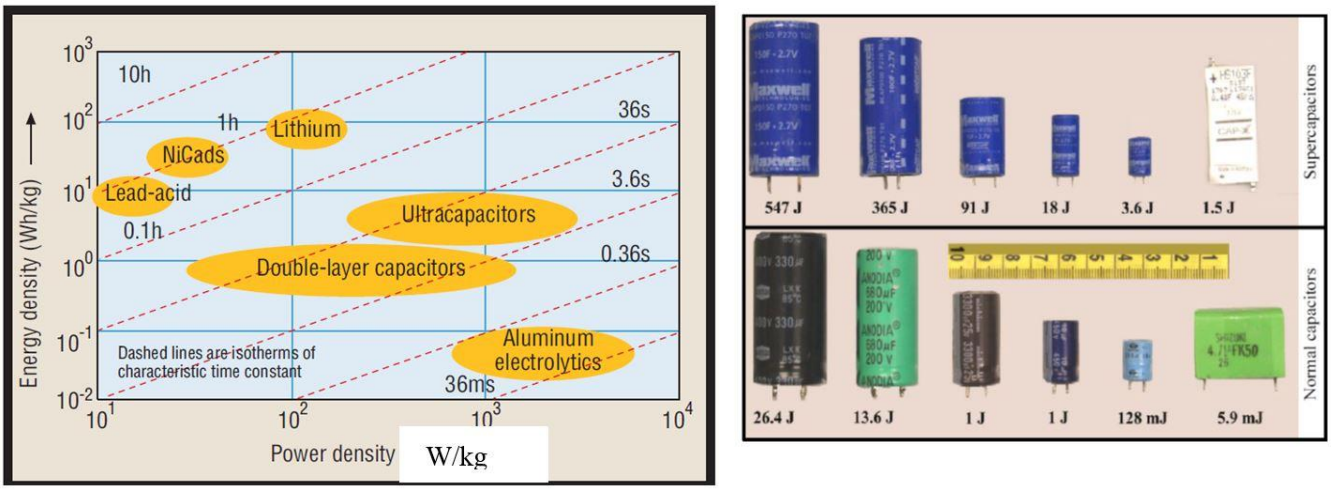


Fig. 4. Overall efficiency of powering a useful load within the loop while charging a capacitor. A higher dc voltage source is used in all cases compared to the maximum dc voltage rating of the capacitor, and a switch is to be used to stop overcharging the capacitor.

Insertion Of A Large Capacitor As A Lossless Dropper

Given the above discussion, we see the potential of inserting a useful resistive load within the capacitor charging loop. Now we can think of replacing the capacitor in the loop with one several orders of magnitude larger, making use of the commercially available supercapacitors. Based on the Ragone plot shown in Fig. 5a, we recognize that the SCs have lower energy density than the rechargeable batteries and they come with higher power density than batteries.



(a) (b)

Fig. 5. Ragone plot comparing batteries, SCs and electrolytic capacitors and a physical size comparison of SCs and electrolytic capacitors.

In general, commercially available SCs come in capacitance values varying from 0.2 to 7500 F in single-cell devices, and they usually come with capacitance values on the order of approximately one million times the values of electrolytic and other common capacitors for the same volume. Fig. 5b depicts a pictorial view of this comparison. In general, their ESRs are in the range of 0.3 to 100 mΩ, which is about one order smaller than the electrolytic caps. And the larger the supercapacitor, the smaller the ESR.

One major disadvantage of SCs is their very low dc voltage rating, which typically ranges from 0.7 V to about 4 V. But their leakage properties are very good and, in general, they can retain almost 80% of the charge after about 8 hours.

With the simple case of an RC circuit with 1-Ω resistance and a 1-μF capacitor we achieve a time constant of 1 μs. This circuit, if fed by a dc source of 5 V it will take approximately 5 μs to fully charge the capacitor assuming that the capacitor didn't have any charge to begin with. Now let us replace this 1-μF capacitor with an SC of 1 F. The time constant increases by one million times, and the circuit will take about 5 seconds to fully charge the capacitor.

Consider the situation where an SC is connected in series with a simple 5-V linear regulator, which has good line-regulation characteristics to maintain the output voltage at 5 V for the input range of 5.5 V to 12 V. In general, this circuit's end-to-end efficiency (ETEE) will vary from approximately 5/5.5 to 5/12 which will be in the range of 91% to 42%, neglecting the losses in the feedback control circuits, etc.

Fig. 6 depicts this scenario, and in Fig. 6a we insert an SC of 1 F with a pre-charge voltage of 6 V in the series path of the linear regulator. If the linear regulator supplies a load current of 1 A, the capacitor will keep charging towards 6.5 V and it will take a time Δt of 0.5/1*1 = 0.5 seconds. Now if we remove this series capacitor before it is fully charged to its maximum value of 6.5 and discharge it to the linear regulator we can disconnect the input source for a while, increasing the efficiency of the overall dc-dc converter circuit. Fig. 6b depicts the discharge of that accumulated extra energy in to the same linear regulator.

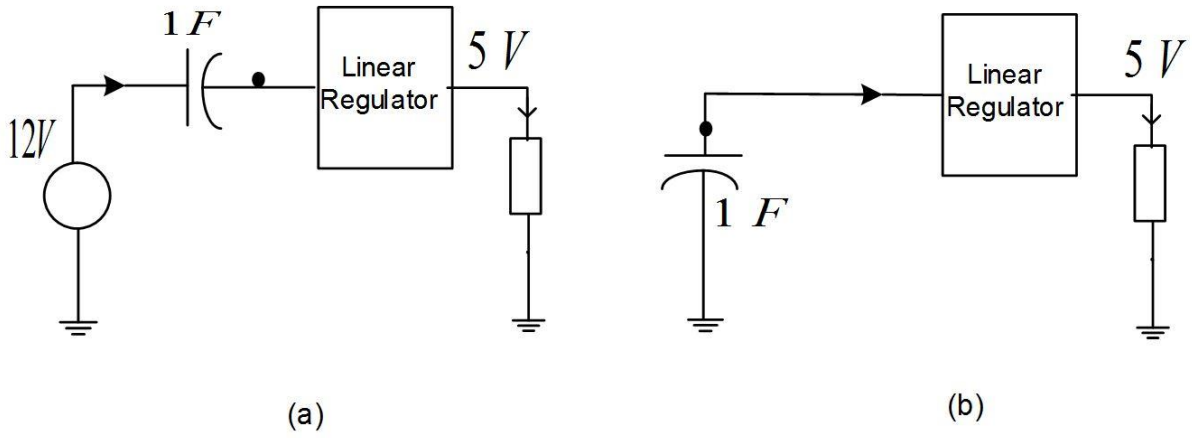


Fig. 6. A supercapacitor helps us build a highly efficient linear regulator (a) by adding a series SC of 1 F pre-charged to 6 V in the series path of a 5-V linear regulator with good line regulation from a 5.5-V to 12-V input and releasing the accumulated extra charge/energy back to the same linear regulator (b).

The above discussion now shows the practical possibility of modifying the RC charging circuit by inserting a loaded linear regulator to gain a significant end-to-end-efficiency (ETEE) advantage. In the case of Fig. 6a, a very large capacitor gets charged without much waste of energy, since the loaded linear regulator acts as a useful resistive load.

If you look at from a different angle, when our SC is an ideal circuit element, with zero ESR, all that it does in the series charging path of Fig. 6a is to act as a lossless-voltage-dropper to improve the overall efficiency of the

12-V to 5-V converter. In practice by switching the configuration between Fig. 6a and 6b, we maintain the charge balance of the SC and hence we halve the time that the linear regulator is disconnected from the 12-V dc source.

Fig. 7 shows the simple concept of the patented linear regulator technique, now generally known as the supercapacitor assisted low dropout regulator (SCALDO).

SCALDO Regulator—Basic Facts And A Prototype Implementation

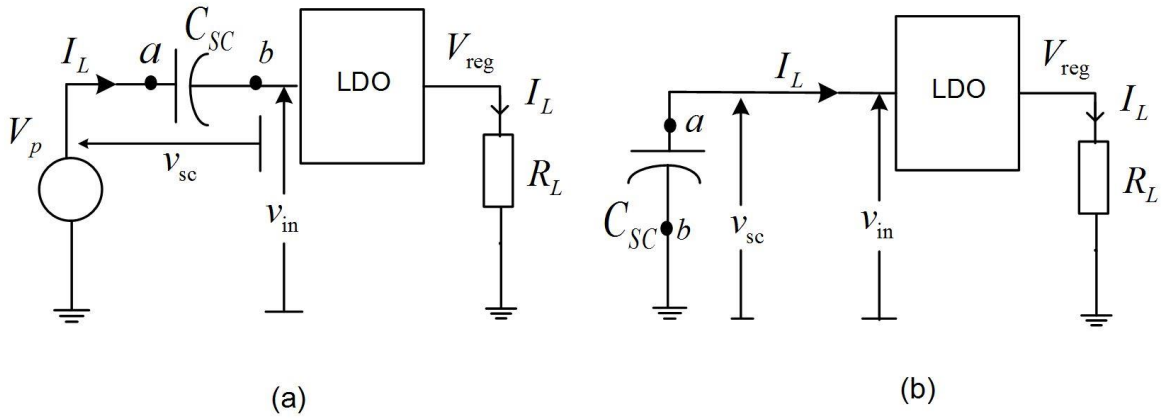


Fig. 7. Conceptual illustration of a supercapacitor-assisted low dropout regulator. Inserting an SC as a dropper element in the series path of a commercial LDO (a) and discharging the SC to release the stored energy to power the LDO in the next cycle (b).

As per Fig. 7a, in the first phase of the operation, a pre-charged SC (C_{sc}) precedes as a series voltage dropper in a commercial low dropout regulator (LDO) circuit, where the voltage change across the supercapacitor due to the input current I_{in} is given by

$$\Delta V_{SC} \approx \frac{I_L \Delta t}{C_{SC}}$$

The series supercapacitor charges until V_{in} reaches the V_{in}^{min} while the voltage across the capacitor reaches (V_p-V_{in}^{min}) at the end of the charging time. In order to discharge this supercapacitor later down to V_{in}^{min} it should satisfy the criteria $V_p > 2V_{in}^{min}$. At the end of the charging, the stored energy in the supercapacitor can be released as shown in Fig. 7b discharging continuously until the LDO input voltage drops back to V_{in}^{min}.

Based on the overall charge balance in the supercapacitor, for the case of $V_p > 2V_{in}^{min}$ the efficiency is given by,

$$\eta = \frac{P_{out}}{P_{in}} = \frac{I_L V_{reg}}{V_P (I_L/2)} = \frac{2V_{reg}}{V_p}$$

For example, a typical 5-V linear regulator operating from 12-V input can achieve only a theoretical maximum efficiency of 42%, whereas in the SCALDO version of the same linear regulator a maximum theoretical efficiency of 84% can be achieved.

Fig. 8a shows a block diagram representation of a 12-V to 5-V SCALDO regulator, which is an implementation of a version with the $V_p > 2V_{in}^{min}$ basic topology. Switches S1 and S3 are kept closed at the start, placing the supercapacitor in its charging configuration; S2 and S4 are kept open at this time. The voltage level at the LDO input is monitored continuously by a microcontroller (MCU).

When V_{in} decays to V_{in}^{min}, S1 and S3 are opened and the switches S2 and S4 are closed. Now the stored energy in the supercapacitor discharges to the regulator's input terminal. When the LDO input voltage reaches the minimum input voltage V_{in}^{min} of the regulator, S2 and S4 open and S1 and S3 closed. This cycle repeats to keep the overall regulator circuit working continually.

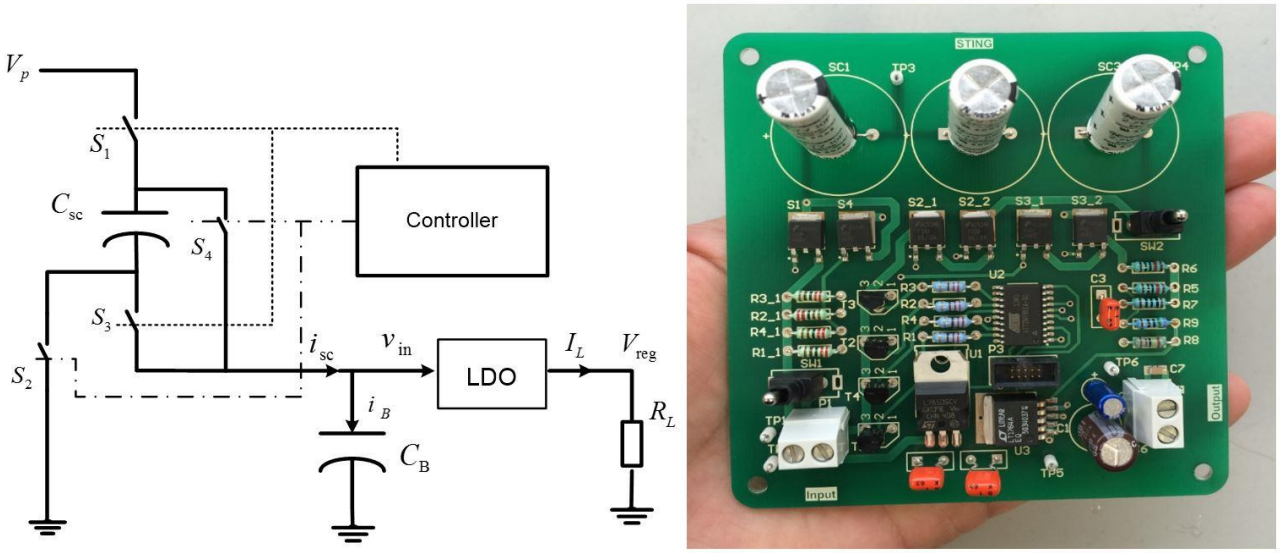


Fig. 8. A 12-V to 5-V SCALDO regulator. Shown here are a conceptual representation with a controller (a) and a prototype implementation of a 12-V to 5-V, 2-A converter.

In the 12-V to 5-V prototype shown, an LDO of the type LT1764A from Linear Technology is used and the V_{in}^{min} value is maintained at 5.4 V. Three 10-F/2.7-V supercapacitors from Nesscap supercapacitors are used in this design to achieve the resultant capacitance of 3.3 F/8.1 V.

To implement four switch positions S1, S2, S3 and S4 using MOSFET switches, which are controlled by a 5-V microcontroller S1, S3 and S4 were chosen as PMOS type and S2 was chosen as NMOS type. Nevertheless, if four single MOSFET switches are used, in the charging phase of the supercapacitor when S1 and S3 are on, there is a conduction path through the body diode of S2 as well.

This additional conduction path jeopardizes the predicted SCALDO operation. Similarly, in the discharging phase of the supercapacitor when S2 and S4 are on, there is another conduction path through the body diode of switch S3 as well. To eliminate this problem, back-to-back p-channel MOSFETs of the type FDD4685 as S3 and back-to-back n-channel MOSFETs of the type FDD6670A as S2 are used in this prototype as shown in Fig 8b.

Four NPN transistors (BC546B) are placed between the MOSFETs and the MCU to drive the MOSFETs. The ATtiny861A microcontroller is used to drive the MOSFETs on and off. An independent 5-V regulator (L78S05CV) was connected to supply the power for the microcontroller. To keep the linear regulator powered during the transitions, an electrolytic capacitor (as a buffer) was connected between the LDO input terminal and the ground terminal. This design is able to achieve a maximum load current of 2 A.

Fig. 9 shows the efficiency improvement achieved in the prototype. As seen from the middle trace of Fig. 9, the 12-V to 5-V SCALDO prototype achieves overall end-to-end efficiencies in the range of 70.7% to 87.8%, compared to the maximum theoretical efficiency of 71.4% to 88.5% for a SCALDO theoretical regulator. The graphs indicate a 0.7% to 0.9% difference between the theoretical and measured power efficiencies for this lossless-dropper supercapacitor technique.

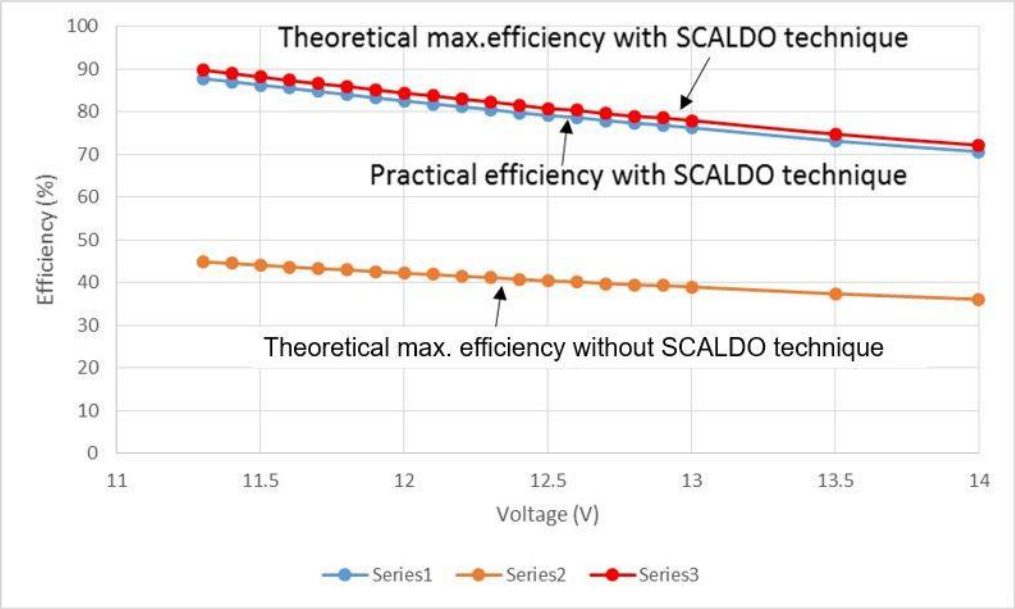


Fig. 9. 12-V to 5-V SCALDO regulator efficiency improvement.

In the 12-V to 5-V example shown here, the circulation frequency increases from 0.01 to 2.8 Hz with the increase of the load current from 100 to 2000 mA. Since the SCALDO technique does not operate at high frequencies, it has no RFI/EMI issues and the load experiences the high slew rate capable low-noise output of a linear regulator.

It is important to indicate here that the technique does not necessarily require a digital control loop based on a microcontroller, but the prototype example discussed here was developed to show the value of this loss-circumvention principle applied into the basic RC converter to achieve RFI/EMI free linear regulators with high end-to-end efficiency. Currently the research team is in the process of implementing the technique in the form of a silicon IC. More details on the SCALDO converter are available in the references.[1-7]

Supercapacitors required by this technique are in the range of 1 to 100 F in general, and these are not too expensive or large in size compared to electrolytic types. Given this condition, and given that the SCALDO technique can be applied in high-current regulators, this technique could be less costly than a typical switch-mode converter. A switch-mode converter typically requires an inductor, a switching transistor, its drive circuit, and an RFI/EMI filter as the bare minimum of parts where some parts will be still discrete components.

If the SCALDO technique is implemented in silicon, it requires a modified version of an LDO, with two to four very low-speed switching transistors, and these can be implemented in a single chip. A digital controller as shown in this discrete parts implementation is not mandatory. The digital controller in the example is just for the convenience of demonstration.

An SC and a small electrolytic may be on the PCB, for cases up to about 3 A with the rest of the circuits' implementation in a silicon monolithic IC. If the output current specs for a design call for a high-current implementation (5 to 50 A), a high-current-capable pass transistor and the low-speed switches can be discrete transistors, where the SCALDO controller can be a single chip silicon IC. Currently the research team is working with Southampton University to come up with a silicon implementation of a SCALDO circuit. In a future article more details will be presented.

Wider Implications Of The RC Circuit And The Loss-Circumvention Principle

SCALDO is only an example application of the loss circumvention principle applied in the well-known RC circuit. In a follow-up to this article, we will discuss how this can be usefully applied in many different power electronic converter circuits and protection techniques such as SCASA, SCATMA, SCAHDI and SCALED.

References

1) "High current voltage regulator" by N. Kularatna and J. Fernando, U.S. Patent 9707 430 B2, March 15, 2011.

2) "Analysis on supercapacitor assisted low dropout regulators" by K. Gunawardane, The University of Waikato, New Zealand, Ph.D. thesis, 2014.

3) "Laplace Transform-Based Theoretical Foundations and Experimental Validation-Low Frequency Supercapacitor Circulation for Efficiency Improvements in Linear Regulators" by K. Kankanamge, N. Kularatna, and D. A Steyn-Ross, IET Power Electronics, 2012, 5(9) pp. 1785–1792.

4) "Improving the end-to-end efficiency of DC-DC converters based on a supercapacitor assisted low dropout regulator (SCALDO) technique" by K. Kankanamge and N. Kularatna, Transactions on IEEE Industrial Electronics, 2013, 61(1), pp. 223 – 230.

5) "Supercapacitors Improve the Performance of Linear Power-Management Circuits: Unique new design options when capacitance jump from micro-farads to farads with a low equivalent series resistance" by N. Kularatna, IEEE Power Electronics Magazine, 2016, 3(1), pp. 45-59.

6) "Supercapacitor assisted LDO (SCALDO) technique—an extra low frequency design approach to high efficiency DC-DC converters and how it compares with the classical switched capacitor converters" by K. Kankanamge and N. Kularatna, Proc. IEEE Applied Power Electronics Conference, March 2013, pp 1979-1984.

7) "Implementation aspects of a new linear regulator topology based on low frequency supercapacitor circulation" by K. Kankanamge and N. Kularatna, Proc. IEEE Applied Power Electronics Conference, 2012, pp. 2340 – 2344.

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Nihal Kularatna (SM'98) is an associate professor in electrical engineering lecturer in the School of Engineering at the University of Waikato, New Zealand. A recipient of the New Zealand innovator of the year award for 2013, his electronic engineering career spans 42 years. He is currently active in research in supercapacitor applications, power supply topologies, transient propagation and the power conditioning area in power electronics.

Kularatna has contributed over 130 papers to journals and international conference proceedings. He has authored or co-authored eight books and several of them are in power electronics. His latest book, "Energy Storage Devices for Electronic Systems: Rechargeable Batteries and Supercapacitors," was published in 2015 by Elsevier AP, USA. Multiple patents were granted for his supercapacitor-assisted circuit topologies after 2011. Prior to migrating to New Zealand in 2002, Kularatna was the CEO of the Arthur C Clarke Institute for Modern Technologies in Sri Lanka.

Kosala Gunawardane is currently a lecturer in electrical and electronics engineering at the Auckland University of Technology, New Zealand. Her research interests are analog circuit design, low-dropout regulators, supercapacitor-based applications, superconductor applications in power engineering and dc-microgrid. Gunawardane received the B.Sc.(Hons.) degree in electronics and telecommunication engineering from the University of Moratuwa,

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For further reading on the design of dc-dc converters and linear regulators, see the How2Power Design Guide, select the Advanced Search option, see the Power Supply Function category and select "DC-DC converters" and "Voltage regulators".