

Beware The Pitfalls Of Power Supply Hipot Testing

by Kevin Parmenter, Chair, and James Spangler, Co-chair, PSMA Safety and Compliance Committee

What is hipot (high potential) testing and what is it for? A dielectric withstanding voltage test is used to determine the ability of equipment with an installed power supply to protect against electrical shock. The dielectric withstand voltage test is typically referred to as a hipot test and involves applying a specified high voltage between the points being tested and measuring the resultant leakage current.

The test has been with us a long time. However, as power supplies have developed and EMC requirements have become more stringent in, for example IEC 60601 4th edition EMC and 62368, we have seen customers needing more guidance in the proper application of the testing. Moreover, it should be emphasized that for switching power supplies, the hipot test should be considered a destructive test. What is meant by this?

It does not mean that it will destroy the device under test immediately but rather that hipot testing is not like testing 1% resistors with a DMM where you can apply the test as many times as you like and leave the applied test in place without damage. You also cannot assume that the test conditions are irrelevant as when using the DMM.

For example when measuring a resistor the user of the instrument typically does not inquire into the methodology of the test and the voltages and currents involved. Yet with hipot testing, it seems everyone wants to get in on the fun and make sure they are doing due diligence when it comes to testing and to verify that anything under their control conforms to standard and is safe. Unfortunately, this widespread concern for compliance actually leads to problems as we'll discuss.

Let's start with the power supply itself and observe a typical hipot testing process it may undergo when ordered by a customer. First, let's assume that a quality maker of power supplies will test the power supply in production 100%. Next, let's say that it goes to a value added distributor, which receives the power supply and decides to do hipot test on it during incoming inspection. This power supply is then sent to a customer who does hipot again during their incoming inspection. Finally, after the end equipment is built, that system is subjected to a hipot test before the end system is shipped.

Recall that the purpose of the test is to validate the safety of the power supply and the end equipment it's installed in. This is the right goal. Yet, what is being tested in the power supply? With hipot, the creepage and clearance isolation barriers are what you wish to test. For the most part, these isolation barriers can withstand the testing just fine if designed and rated properly, and if the test is designed and carried out properly.

The issue is that EMC components, namely safety capacitors (also known as Y capacitors), are also in the test path. So in many cases you are not only testing the isolation barriers, you are damaging the capacitors while testing. Then when the product fails hipot, the customer thinks they have caught a problem: "Ah hah! It's a good thing we tested because we found something." But that conclusion is often incorrect. In our example, the testing induced damage.

The key is understanding that you have finite limits of amplitude, duration and number of applications of the hipot test before you are no longer testing for existing faults but rather creating them.

Of course, no one wants to induce damage in a product before they ship it. One of the possible solutions is to use dc equivalent testing, which will still test creepage and clearance, yet is much less damaging to the UUT. In general, dc equivalent hipot testing will not damage safety capacitors as long as you stay within the manufacturer's guidelines.

High-voltage ac applied to capacitors often simply turns the dielectric into a plasma and compromises it so that you will see leakage due to the capacitive reactance and the energy of turning the dielectric into a plasma. So you get leakage and fail the hi pot test even though the creepage and clearance isolation barriers are fine.

So what's the proper course of action for power supply users?

1. Work closely with your power supply manufacturer and ask ahead of time what the recommended limits are.

2. Use dc equivalent testing. The nationally recognized testing laboratories (NRTLs) and specifications all allow for dc hipot testing vs. ac hipot testing. Going with dc will allow more testing with less damage and you get the same quality result. To determine the dc test voltage, simply multiply the ac you were going to apply by $\sqrt{2}$ or approx. 1.414. In other words, use the peak value of the ac voltage for your dc value.
3. Only apply the dc voltage for the length of time needed to make the test and watch the test time application. It's not infinite.
4. Watch the number of times the test is applied. That's not infinite either.
5. After doing a dc equivalent test make sure and discharge the test points so you don't leave dangerous charges on the capacitors for safety sake. Make sure these caps are discharged.

It can't be overstressed that you need to work with your power supply maker or system provider to insure your hipot testing is actually testing product safety rather than creating problems and potentially shipping damaged products to your customers.

For those working at power supply companies, consult with your customers to ensure they understand the issues surrounding hipot testing. Doing so will ultimately save your company time and resources, while helping to keep your customers happy.

About The Authors



Kevin Parmenter is an IEEE Senior Member and has over 20 years of experience in the electronics and semiconductor industry. Kevin is currently vice president of applications engineering in the U.S.A. for Excelsys, an Advanced Energy company. Previously, Kevin has served as director of Advanced Technical Marketing for Digital Power Products at Exar, and led global product applications engineering and new product definition for Freescale Semiconductors AMPD - Analog, Mixed Signal and Power Division based in Tempe, Arizona.

Prior to that, he worked for Fairchild Semiconductor in the Americas as senior director of field applications engineering and held various technical and management positions with increasing responsibility at ON Semiconductor and in the Motorola Semiconductor Products

Sector. Kevin also led an applications engineering team for the start-up Primarion where he worked on high-speed electro-optical communications and digital power supply semiconductors.

Kevin serves on the board of directors of the [PSMA](#) (Power Sources Manufacturers Association) and was the general chair of APEC 2009 ([the IEEE Applied Power Electronics Conference](#).) Kevin has also had design engineering experience in the medical electronics and military electronics fields. He holds a BSEE and BS in Business Administration, is a member of the IEEE, and holds an Amateur Extra class FCC license (call sign KG5Q) as well as an FCC Commercial Radiotelephone License.



Jim Spangler is a Life Member of the IEEE with over 40 years of electronics design experience and is president of Spangler Prototype Inc. (SPI). His power electronics engineering consulting firm's priority is helping companies to place products into production, assisting them to pass government regulations and agency standards such as UL, FCC, ANSI, IES, and the IEC.

For many years, he worked as a field applications engineer (FAE) for Motorola Semiconductor, On Semiconductor, Cirrus Logic, and Active Semiconductor, assisting customers in using semiconductors. He published numerous application notes and conference papers at a variety of conferences: APEC, ECCE, IAS, and PCIM. Topics included power factor correction, lighting, and automotive applications. As an FAE, he traveled internationally giving switch-mode power supply seminars in Australia, Hong Kong, Taiwan, Korea, Japan, Mexico, and Canada.

Jim has a Master's Degree from Northern Illinois University (NIU), and was a PhD candidate at Illinois Institute of Technology (IIT). He taught senior and first-level graduate student classes: Survey of Power Electronics, Fields and Waves, and Electronic Engineering at IIT and Midwest College of Engineering.

Jim is a member of the IEEE: IAS, PELS, PES; the Illuminating Engineering Society (IES), and the Power Sources Manufacturers Association (PSMA) where he is co-chair of the Safety and Compliance Committee.