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Dual Buck Doubles The Duty Cycle For Ultra Low-Voltage Applications

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The large microprocessors (Intel, Sun, IBM) require a high current and a low voltage. A core voltage of 0.6 V at 200 A is not uncommon. It can be an even lower voltage in sleep mode.

Typically the topology used to supply this voltage is a multiphase buck with 8 to 12 phases. The input voltage is 12 V and in this example where the output voltage is 0.6 V, the buck has to work at a duty cycle close to 5%. The duty cycle gets even lower in sleep mode where the output voltage can be 0.3 V. At a duty cycle below 5%, the on-time barely exists and efficiency is very low.

This article presents an alternative multiphase buck topology that performs the same voltage transformation as the conventional multi-phase buck but without some of the drawbacks. As illustrated in the simplified power stage diagram in Fig. 1, this topology consists of two bucks ganged with *paralleled* and sequenced *outputs*. The inputs work as if they were *in series* and share the 12-V input voltage. Each buck works with 6 V instead of 12 V and the duty cycle is multiplied by 2.

The inputs are not really in series but the effect is the same. There is a large capacitor charged at Vin/2 in series in the middle of the first buck. This 6 V is subtracted from the 12 V and the buck operates with the 6 V that is left. Current flows for the first buck follow the red and purple paths in Fig. 1.

The second buck works with this same 6-V capacitor as an input so it also operated from 6 V. Current flows for this buck follow the green and blue paths in Fig. 1. The second buck is sequenced so that the two bucks operate in alternate mode (180 degrees out of phase). Both bucks work with 6 V and hence have a duty cycle twice that of a standard buck converter.

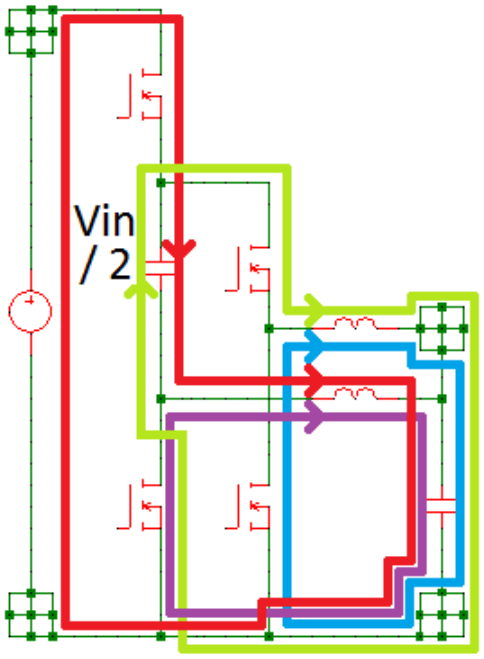

Fig. 1. Simplified schematic for dual buck power stage.

Fig. 2 is the simulation schematic for the dual buck and Fig. 3 shows the resulting simulated waveforms. The two top waveforms IL 1 and IL 2 are the inductor currents. They have the same amplitude and are out of phase.

The red and green waveforms are the top and bottom of the Vin/2 capacitor. They are the phase nodes of the first buck and are associated with IL 1. The blue waveform is the second phase node and is associated with IL 2.

With this design, the efficiency is higher than the conventional multiphase buck since the duty cycle is doubled and hence not at 5% or under. Since efficiency is the critical parameter, a key design goal is satisfied. Meanwhile, the number of power semiconductors in the power stage remains the same as 12 phases are reduced to six but with four switches per phase and this design can still use the same controller. So cost is not affected. The patent for this circuit was assigned to Volterra, which is now owned by Maxim.

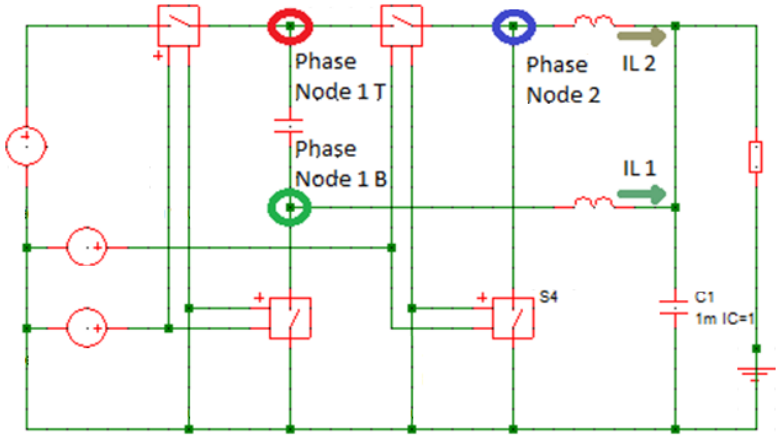

Fig. 2. Simulation schematic for the dual buck with duty cycle doubler.

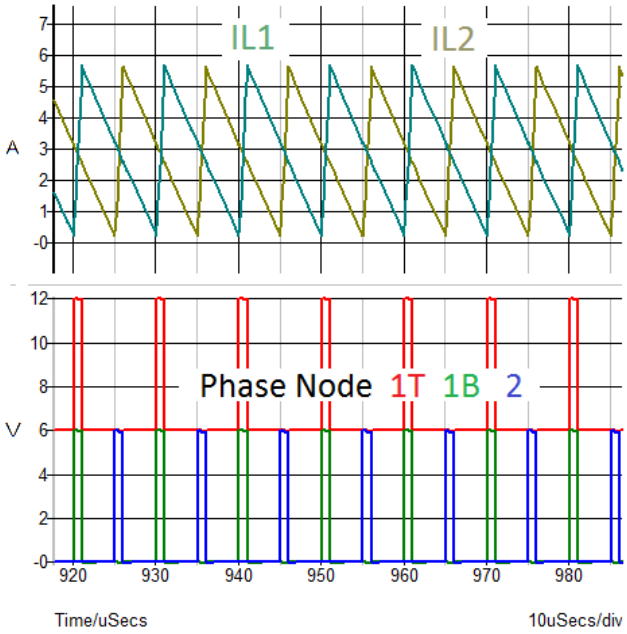

Fig. 3. Simulation waveforms for the dual buck with duty cycle doubler.

About The Author

Patrice Lethellier is a consultant with "It Can Be Done" where he specializes in presenting unconventional ways of doing the designs, while also consulting on most other aspects of power conversion. Results oriented, all of his consulting work relates directly to proactive and productive design. Patrice has over 40 years of experience in industry as a power supply design engineer in OEM and merchant power supply companies and as an application engineer in power semiconductor companies. Since 2014 Patrice has been a senior engineer with Wave, where he has developed wireless battery charging solutions from 50 kW to 200 kW for electric buses.

Prior to this, he served as an application engineer with notable power semiconductor companies such as Volterra, National Semiconductor and Semtech. Before that, he worked as a design engineer at various power supply and system companies including C&D Power Technology, Pioneer Magnetics, Elgar and Unisys. Patrice holds a total of 20 patents in various fields with some currently in process. He has an Engineer Diploma from ISEN in Lilles, France.

The technique described in this article was used by the author when he was an engineer at National Semiconductor in Chandler, Ariz.

For more information on current-mode control, see How2Power's Design Guide, locate the Design Area category and select "Control Methods".