Achieve Precise High Current Monitoring Using Standard Surface-Mount Resistors

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High accuracy current monitoring is essential and necessary for a wide range of applications. Examples of applications include overcurrent protection, server power management, and prevention of exothermic events, which can even include equipment catching on fire. There are a variety of high-side (hot wire) current monitoring ICs providing precision conversion of a dc biased ("high side") sensor voltage to a single ended (referenced to ground) signal. In low-voltage, high-current applications, in which sensor voltage drop may noticeably impact power distribution efficiency, designers are required to use very low (sub-milliohm) resistance sensors.

High power rated sub-milliohm sensors often come with Kelvin connect terminals, which simplify their layout, but take up more PCB space, and are less accurate and more expensive than standard precision surface-mount (SM) parts. Lower monitoring accuracy requires larger margins in the designs, impacts server system performance, and complicates power distribution arrangement. Because of these factors and the higher cost of four-terminal parts, designers generally prefer to select standard SM resistors.

When connected in parallel, conventional SM two-terminal parts can support the sub-milliohm resistance range of the sensor. With proper PCB trace routing and summing signals of paralleled sensors a much better (1%) current signal monitoring accuracy can be achieved even without calibration. The specifics of achieving optimal sensing accuracy and paralleled sensor signal routing are discussed in this article.

The Equal Current Path Method

Let's assume the monitored current *I* flows through two identical paralleled SM resistors Rs1 and Rs2, each having the same value R_s. For the theoretical (ideal) case, the voltage drop V_{ri} across Rs1 or Rs2 is:

$$V_{ri} = I*R_s/2 \quad (1)$$

To accurately sense this voltage level in a real application the current path lengths can be made equal for each of the paralleled resistors. In this case the current signal can be accurately monitored via a single pair of Kelvin connections placed immediately adjacent to the target resistance, as illustrated in Fig. 1.

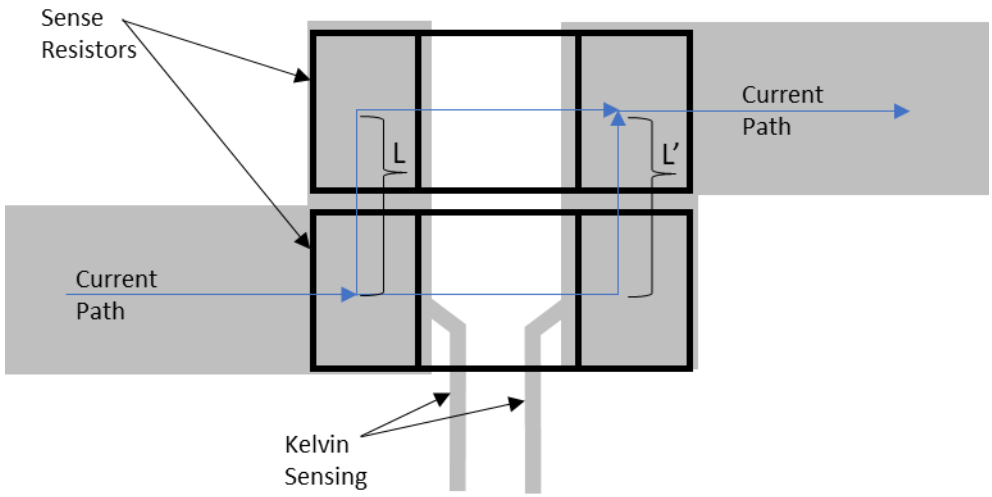


Fig. 1. With equal current path lengths (L = L') for each of the paralleled resistors accurate current sensing can be provided with a single pair of Kelvin connections.

Such an arrangement also provides natural power dissipation balance, which is important when sensor power rating is marginal. However, in many applications such an arrangement of current carrying traces may not be feasible due to layout constraints. In cases with unequal sensor current paths, a more detailed study of current monitoring is needed.

Dealing With Unequal Current Path Lengths

If current paths for each of the resistors are different (Fig. 2), the monitoring accuracy will be impacted by trace resistance. This will occur because the sensed current will not split equally between the paralleled resistors. The sensed signal will exceed the projected level when sense lines are connected to one resistor or across the resistors (shown with dashed line in Fig. 2), which causes an offset error in the sensed signal and inaccuracy attributable to trace resistance. To better understand the inaccuracy of the sensing circuit this offset needs to be quantified.

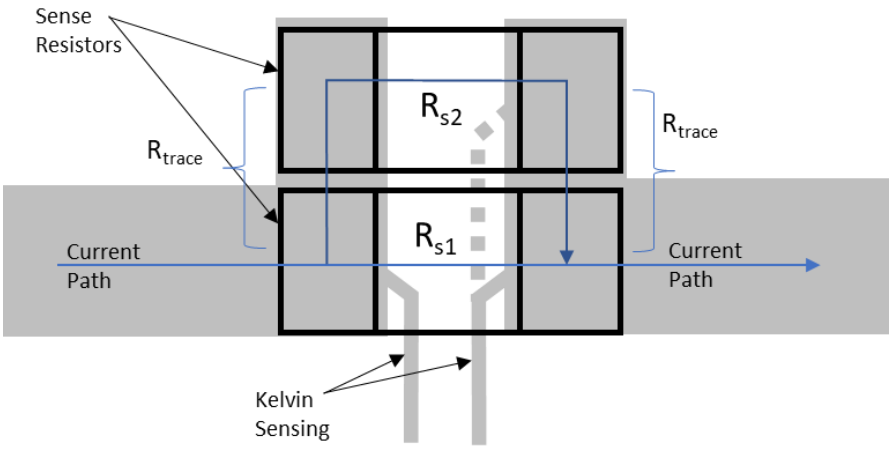
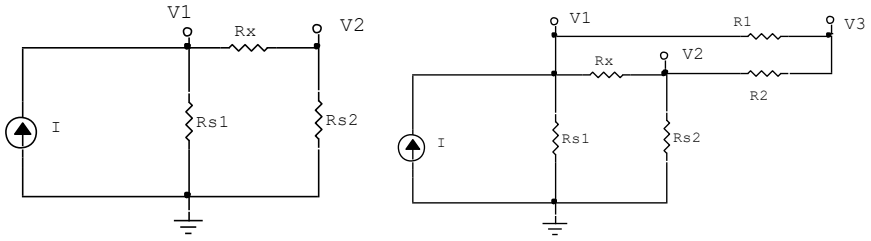


Fig. 2. With unequal current path lengths for each of the paralleled resistors single Kelvin pair sensing accuracy will be impacted by trace resistance and this error needs to be taken into account.

If the sensing branch lengths are significantly different, then designers also need to consider the difference in sensor power dissipation, which can impact resistor power rating. The sensor with the shortest current path (e.g. the bottom sensor in Fig. 2) will have the highest power stress.

The Fig. 3 diagram contains two identical sensors Rs1 and Rs2 with equal values of R_s. The voltage source supplying power and the load determining its current are replaced with an equivalent current source I. The equivalent resistance of the traces connecting the sensors is represented by resistor Rx.



(a) *(b)*

Fig. 3. Simplified equivalent schematic of paralleled sensors having different current path lengths (a) and the same circuit with summing resistors added (b).

Assuming that Kelvin traces (shown in Fig. 2) are sensing the most thermally stable voltage signal V_1 across Rs1, the equation for a voltage drop V_{rs} across this resistor is:

$$V_{rs} = I*R_{e2} = I*R_s//(R_x + R_s) = I*R_s*(R_x+R_s)/(2R_s+R_x), \quad (2)$$

where R_{e2} is the equivalent resistance of the two paralleled sensors. Normalized offset error can be calculated as V_{rs}/V_{ri}-1, where V_{rs} is determined by equation (2), and V_{ri} is sensor voltage in the ideal case (where $R_x = 0$) given by equation (1).

In the sensor with the shortest trace length, the dissipated power is proportional to the voltage squared across it, which means that the increase in power dissipation is $(V_{rs}/V_{ri})^2$ - 1. Trace offset error and power dissipation increase as functions of the trace/sensor resistance ratio as shown in Fig. 4.

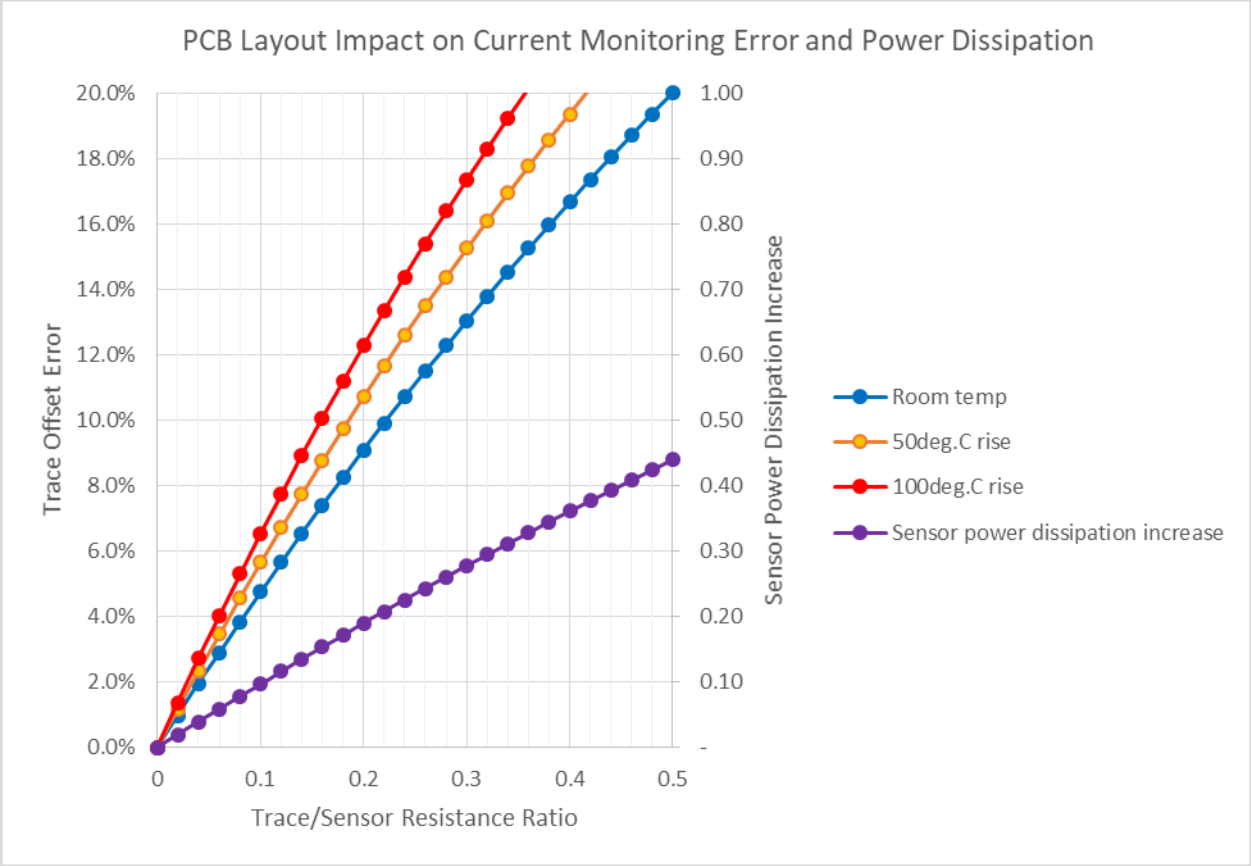


Fig. 4. The impact of PCB layout on the monitoring offset error and on sensor power dissipation increase. Even with only two paralleled sensors sensing accuracy and power dissipation can be noticeably impacted by trace resistance.

Fig. 4 shows the trace offset error at room temperature and for 50°C and 100°C rises in trace temperature, assuming a copper trace resistance thermal coefficient RTC of 0.4%/°C. The results show that unequal path lengths have a major impact on monitoring accuracy.

For example, a 100-mil wide, 0.1-in long trace has a resistance of 243 μΩ at a copper layer thickness T = 2 oz/ft^2. This 243 μΩ is comparable to a sense resistance value in a high-current-sensing application and even with R_s = 1 mΩ, which is a relatively high value for a high-current sense resistance, the trace resistance results in greater than 10% error. However, if the effects of layout resistance and power dissipation are accounted for in the design stage, and assuming the thermal drift is acceptable for a specific application, then

the current signal can be sensed with just one pair of Kelvin connections attached to the inner edges of the SM resistor contact pads, as shown in Fig. 2.

Expressions for errors with three and four paralleled sensors in a similar resistor-ladder type of network are given below:

$$Err_3 = \frac{3\left[\left(\frac{R_x}{R_s}\right)^2 + 3\frac{R_x}{R_s} + 1\right]}{\left(\frac{R_x}{R_s}\right)^2 + 4\frac{R_x}{R_s} + 3} - 1 \qquad Err_4 = \frac{4\left[\left(\frac{R_x}{R_s}\right)^3 + 5\left(\frac{R_x}{R_s}\right)^2 + 6\frac{R_x}{R_s} + 1\right]}{\left(\frac{R_x}{R_s}\right)^3 + 6\left(\frac{R_x}{R_s}\right)^2 + 10\frac{R_x}{R_s} + 4} - 1$$

Fig. 5 shows trace offset error and power dissipation at room temperature in three- and four-sensor cases. The error for a 2-paralleled-sensor case is also plotted for comparison.

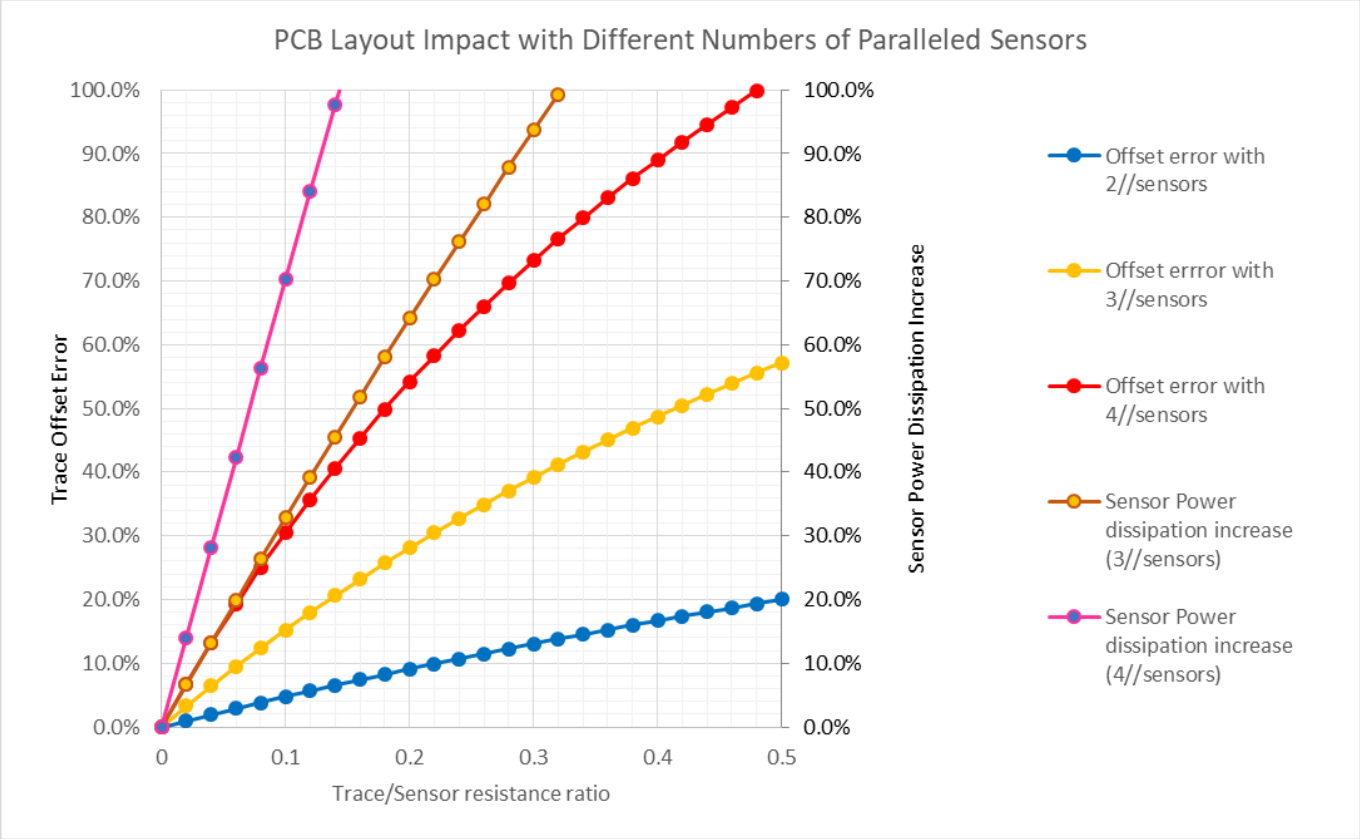


Fig. 5. Impact of PCB layout on the monitoring offset error with two, three and four paralleled sensors.

Fig. 5 shows that the offset error increases with the number of paralleled sensors. This means that if the layout associated offsets are not accounted for, the current sense amplifier will generate signal levels significantly higher than projected and/or the overcurrent protection will trip prematurely, especially at elevated temperatures.

Power dissipation also increases with the number of paralleled sensors. For example, for four paralleled sensors and a 0.1 trace/sensor resistance ratio the power dissipation increase exceeds 70% as compared to the balanced case. Thus, for a larger number of paralleled sensors equalizing trace lengths becomes more critical.

Using Summing Resistors

If better accuracy is required when current path lengths are unequal, summing resistors, connected to the "Kelvin" points of each sensor, need to be used. These resistors form a Kelvin bridge-like arrangement. This case is illustrated by the equivalent circuit in Fig. 3b. This diagram is repeated below in Fig. 6 for the reader's convenience.

Let's evaluate the required tolerance for the summing resistor values so as to ensure their impact on current monitoring accuracy is negligible. If those resistor values are much larger than the sense resistors (R_1 and R_2 > 1000 x R_s), which is always the case, an expression for the sensed voltage V_3 (Fig. 6) at the common point and associated analysis can be simplified.

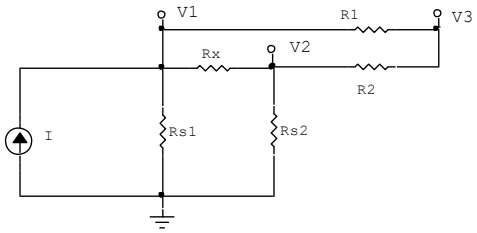


Fig. 6. Simplified equivalent schematic of paralleled sensors having different current path lengths with summing resistors added.

Similar to the layout offset impact evaluation, we consider sense voltage ratio V_{3i} in the ideal scenario ($R_1 = R_2$) to determine the error added by the summing resistor:

$V_{3i} = (V_1+V_2)/2$

and in the real case (where $R_1 \neq R_2$):

$$V_{3r} = \frac{V_1 \cdot R_2 + V_2 \cdot R_1}{R_1 + R_2}$$

Taking into account that: $V_1/V_2 = 1 + R_x/R_s$, we can get the expression for the error induced by the summing resistance tolerance:

$$\frac{V_{3i}}{V_{3r}} - 1 = \frac{\frac{V_2\left(1+\frac{V_1}{V_2}\right)}{2}}{V_2\left[\frac{\frac{V_1}{V_2}}{1+\frac{R_1}{R_2}} + \frac{1}{1+\frac{R_2}{R_1}}\right]} - 1 = \frac{\frac{2+\frac{R_X}{R_S}}{2}}{\frac{1+\frac{R_X}{R_S}}{1+\frac{R_1}{R_2}} + \frac{1}{1+\frac{R_2}{R_1}}} - 1$$

where R_1/R_2 can be used as a variable representing this tolerance.

The impact of summing resistor tolerance is shown in Fig. 7 for two cases: $R_1/R_2 = 1.02$ (0.98) and $R_1/R_2 = 1.1$ (0.904) representing ±1% and ±5% tolerance, respectively.

Fig. 7. Impact of summing resistor tolerance on the added current monitoring error.

If we assume a best-on-the-market sense resistor tolerance equal to 1%, Fig. 7 shows that a 1% summing resistor tolerance provides much lower monitoring error than the error due to sense resistor self-tolerance. This means that for most applications, in which equivalent summing resistor value is not impacted by its trace resistance, such a resistor tolerance can be considered acceptable. Power dissipation in the summing resistors is negligible, which means that they can have a very low power rating and do not take much space on the PCB. The sensing circuit arrangement with summing resistors is shown in Fig. 8.

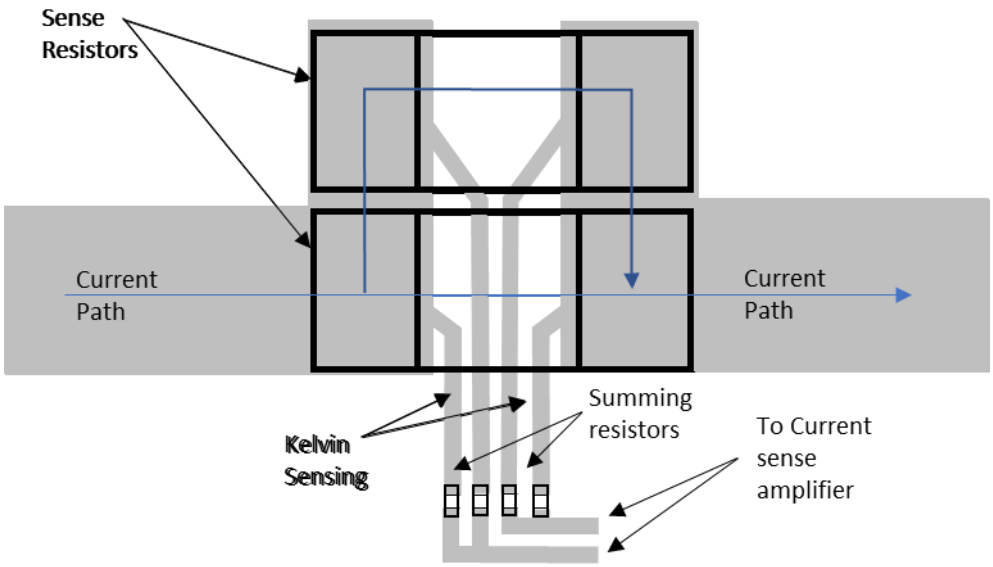


Fig. 8. Adding summing resistors to Kelvin sense lines and forming a Kelvin bridge-like arrangement eliminates monitoring error caused by PCB traces and by differences in current path lengths.

Such an arrangement of summing resistors can be used with virtually any practical number of paralleled sensors with widely varying current path lengths. Note that the summing resistors do not affect power dissipated in the sensors and the power dissipation difference due to unequal path lengths (Figs. 4 and 5) still needs to be considered.

Conclusions

In many cases when there are no layout restrictions, arranging equal current path lengths for each of the paralleled sensors provides sufficient current monitoring accuracy with a single pair of Kelvin connections. But with unequal current path lengths for each of the paralleled resistors, single Kelvin pair sensing accuracy is significantly impacted by trace resistance, especially with increases in the number of paralleled sensors. Adding summing resistors to Kelvin sense lines for high current monitoring eliminates errors associated with differences in current path lengths, PCB trace resistances, and their thermal drifts.

Increasing the number of paralleled sensors with unequal current path lengths results in larger differences in power dissipation. Therefore, in such cases, minimizing and equalizing paralleled sensor trace lengths becomes more critical.

About The Author

Viktor Vogman currently works at Power Conversion Consulting as an analog design engineer, specializing in the design of various power test tools for ac and dc power delivery applications. Prior to this, he spent over 20 years at Intel, focused on hardware engineering and power delivery architectures. Viktor obtained an MS degree in Radio Communication, Television and Multimedia Technology and a PhD in Power Electronics from the Saint Petersburg University of Telecommunications, Russia. Vogman holds over 50 U.S. and foreign patents and has authored over 20 articles on various aspects of power delivery and analog design.

For more information on current sensing techniques, see How2Power's Design Guide, and do a keyword search on "current sensing." Also locate the Design Area category and select Test and Measurement.