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## *Calibration Of Copper Sensors Enhances Accuracy Of Nonintrusive Current Monitoring*

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Nonintrusive current monitoring is important when power losses associated with sensing need to be minimized. Using copper power planes or traces as current sensors represents an attractive option for such a monitoring technique. Since it does not require adding resistors or FETs[1] in the current paths, this nonintrusive method offers an opportunity to provide reliable power monitoring without any impact on the efficiency of power delivery. But there are two main challenges associated with this method. Copper trace or plane impedances are temperature dependent and they have tolerances associated with their geometric (width and thickness) variations.

To address the temperature-dependency concern thermal compensation can be used.[2] Similar to how it is applied within power supplies[3] to eliminate the impact of sensor tolerance, sensor calibration can also be implemented with copper traces for sensing of system loads (such as CPU, memory, hard drives, etc.) in the power distribution network. However, applying conventional calibration methods to such low-resistance copper sensors typically requires using precision high-current electronic loads. Due to their large size and cost, these precision loads are not realizable on the PCB (e.g. computer or server baseboard) and necessitate use of bulky external equipment.

This article introduces a calibration method that corrects for errors caused by copper geometry and variations in signal processing network parameters without requiring high-power equipment. The advantage of this technique is that it can be implemented with a miniature circuit that draws only a few tens of milliwatts of power when active, and can be disabled once the calibration process is complete. This small circuit can be integrated into existing system components, such as server power supplies, on-board CPU- or memory voltage regulators to enable nonintrusive current monitoring. The details on how to implement this calibration technique are given in this article.

### *Accurate Current Monitoring—Where It's Needed*

In real applications a server power train can be overstressed by a power virus—a computer program that executes specific codes forcing excessive CPU power consumption, leading to a power supply overload, CPU overheating or a system crash. Designing power supplies and on-board voltage regulators to support such virus conditions would increase the size and cost of the server platform. Therefore, it is important to optimize these power delivery components by sizing them to support real workloads while protecting them against power virus conditions.

Such protection is most efficient when accurate real-time power (current) monitoring is provided in the power delivery segment closest to the board active elements, such as CPU or memory. When this current monitoring is in place a virus current spike can be suppressed close to its point of origin before it reaches and overstresses the voltage regulator (VR) and power supply components.

High accuracy for CPU power monitoring is also necessary for different power management techniques, such as Intel's Running Average Power Limit (RAPL) technology,[4] which allows users to manipulate processors to maximize a system's performance for a given power budget. Power measurement feedback for a closed-loop RAPL algorithm is typically provided via current monitoring at the voltage regulator (VR IMON signal),[4] which means that the measured current-sense signal is delayed from that of the actual CPU current signal.

However, it's possible to implement a load indicator output IMON feature with much lower latency using the same copper sensor, monitoring actual CPU current. This would greatly simplify requirements for the CPU VR. Real-time CPU current reporting with better accuracy achieved through calibration would also yield a platform with better "turbo" performance for the CPU. These aspects make it critical to develop a simple, reliable and user-friendly power monitoring calibration method that would provide the desired accuracy without using costly external equipment.

### *The Method*

The proposed method is based on generating identical ultra-low duty cycle current pulses through two resistive elements—the copper sensor and a precision reference resistor, and comparing the voltage drops across them. The method is illustrated in the Fig. 1 example of CPU VR-to-CPU package high-side current-path sensing.

In this block diagram the to-be-calibrated sensor $R_{path}$ represents a power plane that conducts current from the CPU voltage regulator to the CPU. During the calibration process, a current sink network (CSN) supplies a meaningful (sufficient for accurate measurement) current flow through $R_{path}$. The CSN is a circuit that generates an ultra-low duty cycle sequence of current pulses. Such a network can operate either in parallel with the installed CPU or in the absence of a CPU (i.e. when the CPU is not installed in its socket).

The CSN pulls the $I_{calib}$ current from the CPU VR. The current path for $I_{calib}$ is shown in Fig. 1 with a red dashed line. The voltage drop across $R_{path}$ is monitored by a current monitoring network (CMN), which is a current amplifier that senses the signal between VR output and the high-side remote sense point. Output of this amplifier represents a voltage pulse signal with magnitude $V_{sense}$.

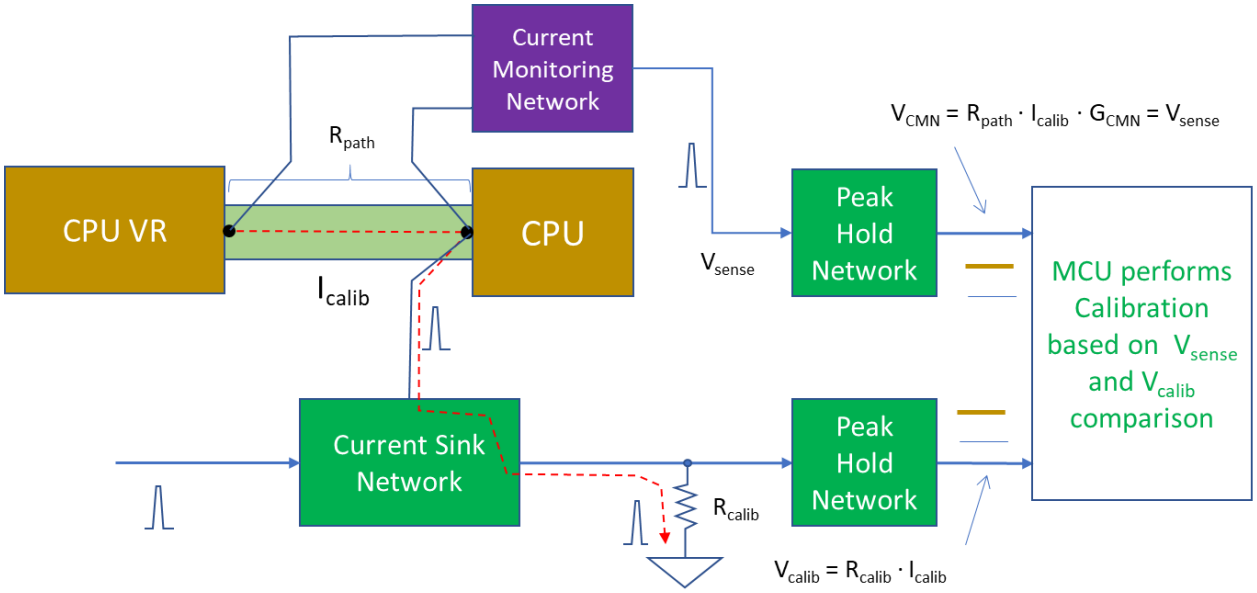


*Fig. 1. Block diagram depicting the proposed method for calibrating a copper trace used as a current sensor. In this case, this calibration method allows for more accurate monitoring of CPU load current.*

The same current flows through a precision resistor $R_{calib}$, across which a calibration voltage pulse signal $V_{calib}$ is generated. Two peak-hold networks convert the two pulse signals into constant voltages equal to the pulse magnitudes—$V_{CMN} = R_{path} \cdot I_{calib} \cdot G_{CMN} = V_{sense}$ and $V_{calib} = R_{calib} \cdot I_{calib}$, respectively. The timing diagram illustrating this process is shown in Fig. 2.

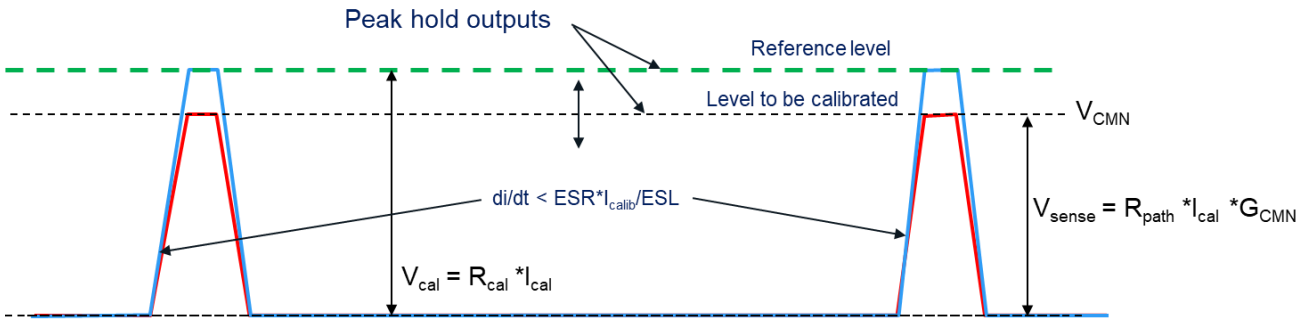


*Fig. 2. Calibration timing diagrams. In the calibration mode, the current signal magnitude $V_{sense}$ representing the amplified sensor signal can be adjusted by trimming the amplifier gain $G_{CMN}$ to match the design case*

The produced unvarying level signals can be polled by a VR controller or external microcontroller at a slow rate, over long time intervals.

To prevent peak-level distortions associated with inductive voltage spikes, the pulse edges must be made shallow as illustrated in Fig. 2. The calibration current slew rate limitation can be described as follows:

$(di/dt)_{max} < ESR \cdot I_m/ESL,$

where ESR and ESL are the resistive and inductive components of the sensor impedance, and $I_m$ is the magnitude of the current pulse.

Consider a reference coefficient that represents a ratio of the projected levels $V_{calib}$ and $V_{sense}$ in a nominal (design) case $R_{path} = R_{path.nom}$, $G_{CMN} = G_{CMN.NOM}$:

$$K_{REF} = V_{calib}/V_{sense.nom} = R_{calib} \cdot I_{cali}/R_{path.nom} \cdot I_{calib} \cdot G_{CMN.NOM} = R_{calib}/(R_{path.nom} \cdot G_{CMN.NOM}), \quad (1)$$

where $R_{path.nom}$ and $G_{CMN.NOM}$ are design sensor resistance and CMN gain, respectively. Similarly, we can express such a ratio for the actual case:

$$K_{ACT} = V_{calib}/V_{sense.act} = R_{calib}/(R_{path.act} \cdot G_{CMN.NOM}), \quad (2)$$

where $R_{path.act}$ is the actual sensor resistance.

Note that using Eqn. (2) with given design values $R_{calib}$, $G_{CMN.NOM}$ and computed voltage ratio $K_{ACT} = V_{calib}/V_{sense.act}$ the actual sense resistance $R_{path.act}$ can also be computed.

The $K_{ACT}$ value can be generated by the VR controller or external MCU by computing a ratio of the output signals of the two peak-hold circuits. This factor can be used for CMN calibration, e.g. current amplifier gain trimming. The amplifier gain needs to be trimmed so that the product ($R_{path.act} \cdot G_{CMN}$) would result in the same sensed voltage level as in the design case, i.e.:

$$R_{path.act} \cdot G_{CMN.SET} = R_{path.nom} \cdot G_{CMN.NOM}, \quad (3)$$

where $G_{CMN.SET}$ is the adjusted amplifier gain. Extracting $R_{path.act}$ and $R_{path.nom}$ from equations (2) and (1) and substituting them into equation (3), we get:

$$G_{CMN.SET} = R_{path.nom} \cdot G_{CMN.NOM}/R_{path.act} = G_{CMN.NOM} \cdot K_{ACT}/K_{REF} \quad (4)$$

Since $G_{CMN.NOM}$ and $K_{REF}$ values are fixed by design, equation (4) defines the required amplifier gain as a function of a computed ratio (2) of the output signals of the two peak-hold circuits $K_{ACT}$. This adjustment option is illustrated with the double-arrow line crossing $V_{CMN}$ level represented by the black dashed line in Fig. 2. As a result of the calibration, the CPU current level signal $V_{sense}$ becomes independent of the $R_{path}$ value variation.

For example, if nominal CMN gain is set so that at the nominal $R_{path}$ value the sensed and calibration voltages are supposed to be identical (i.e. $K_{REF}$ = 1; $R_{calib}$ = $R_{path.nom}$ ·$G_{CMN.NOM}$), but the actual $V_{sense\ act}$ = 0.95$V_{calib}$, (i.e. $K_{ACT}$ = 1/0.95 = 1.053), the CMN gain will be increased by 5.3% to compensate for this $R_{path}$ deviation from the design value.

If in the above example CMN output signal $V_{sense}$ is used by a protection circuit (comparator, MCU, etc.) then in a similar fashion the microcontroller can trim down a comparator threshold by 5% to compensate for such variation in $R_{path}$.

Note, that the $I_{calib}$ variable is not included in equation (4) for the adjusted gain, which means that calibration current variations do not impact calibration accuracy.

If current through $R_{path}$ is being monitored by the CPU (i.e. the current amplifier is integrated into the processor), a digitized version of this correction factor signal could be supplied over the SVID bus to the CPU to tune the gain of its built-in current monitoring network, similar to the power supply case.[3]

If calibrating components were to be integrated into the VR controller, then sensor calibration would be part of the converter start-up algorithm. After the calibration process is complete, the current sink gets disabled, and CMN continues to operate with the calibrated gain generating signal representing an accurate current value. A similar approach can be applied to nonintrusive current monitoring of other critical baseboard components.

## *A Proof-Of-Concept Prototype And Experimental Results*

Since the calibration current magnitude needs to be large enough to produce meaningful voltage readings, the goal of these experiments was to verify whether a high-accuracy calibration could be achieved with low power consumed by the network and whether the circuit could be implemented with small size. The schematic of the proof-of-concept prototype is shown in Fig. 3.

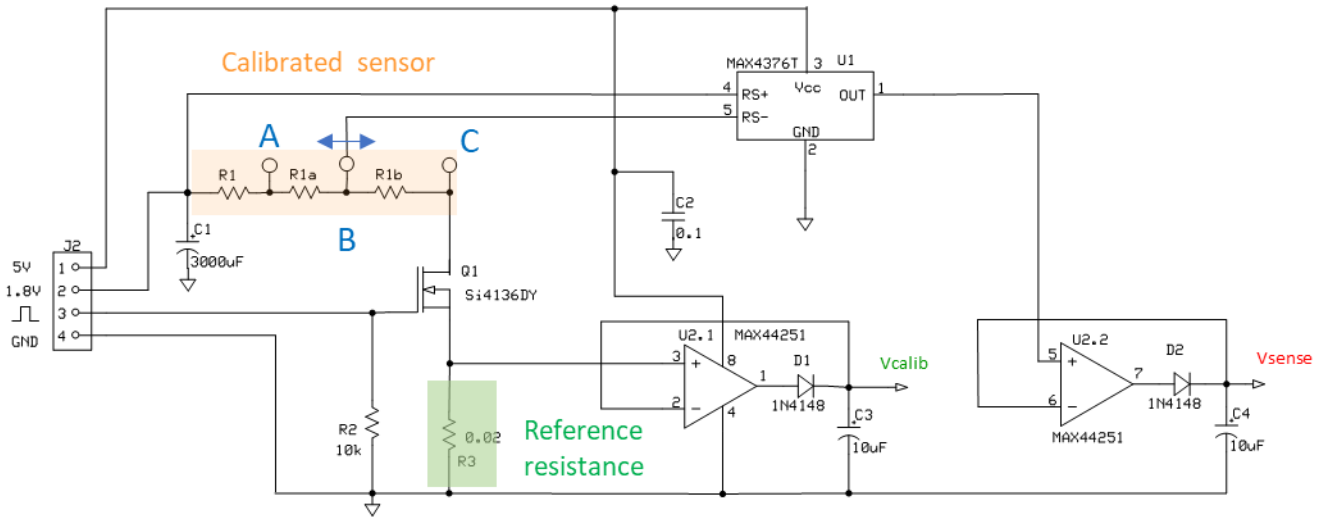


*Fig. 3. Schematic of the current-sensor calibration circuit prototype.*

In the prototype, the copper sensor was implemented with a 1-in x 3-in two-layer PCB and a 170-A rated Crown Clip bus bar connector (TE Connectivity p/n 1982995-1) shorting across the two outer copper planes. Sliding

this connector along the PCB made it possible to quickly change copper sensor resistance over approximately a 30% range.

In Fig. 3, terminals A, B and C represent three positions of the sliding shunt emulating $R_{path}$ tolerance in production. The circuit also contains a power MOSFET Q1 pulling current pulses through the sensor R1-R1a-R1b, and precision reference resistor R3. The sensor signal is monitored by high-side current amplifier U1 that emulates a VR- or on-board current monitoring feature. The current amplifier output signal is fed to the peak hold circuit input represented by U2.2, D2 and C4. The reference signal used in calibration (voltage across R3) is fed to the peak hold circuit represented by U2.1, D1 and C3.

The criteria used for verification of the required minimum power level was not exceeding 0.5% pk-pk ripple in the power plane sense and reference dc signals ($V_{sense}$ and $V_{calib}$) to be used in $K_{ACT}$ computation. The criteria used for calibration accuracy verification was to check whether the computed plane (sensor) resistance can be within 1% of the value measured with high-power precision external equipment.

First, the power plane resistance values R1-R1a and R1b were measured with the precision electronic load in an active cooling environment to minimize the impact of temperature rise caused by self-heating. After that the resistance was computed in calibration mode. The input impedance of the MCU that is supposed to monitor peak hold circuit outputs was emulated with 510-kΩ resistors (not shown in Fig. 3). The experimental results are shown in the table below. As the results demonstrate, the computed sensor resistance is within 1% of the value measured with high-power precision external equipment.

Table. Experimental results obtained with the prototype of the copper-trace current-sensor calibration circuit.

| Power plane resistance configuration | Power plane resistance measured with precision E-load, mΩ | Power plane resistance computed in calibration mode, mΩ | Error, % |
|---|---|---|---|
| $R_1$ | 1.12 | 1.11 | 0.89 |
| $R_1$+Ra | 1.35 | 1.34 | 0.74 |
| $R_1$+Ra+Rb | 1.52 | 1.51 | 0.66 |

Furthermore, timing diagrams for $V_{calib}$ and $V_{CMN}$ (Fig. 4) prove that we have met the sensor accuracy at an average power level not exceeding 180 mW. To achieve the required ripple the current pulse duration was set at 30 μs including edges and repetition frequency $F_r$ = 52 Hz.

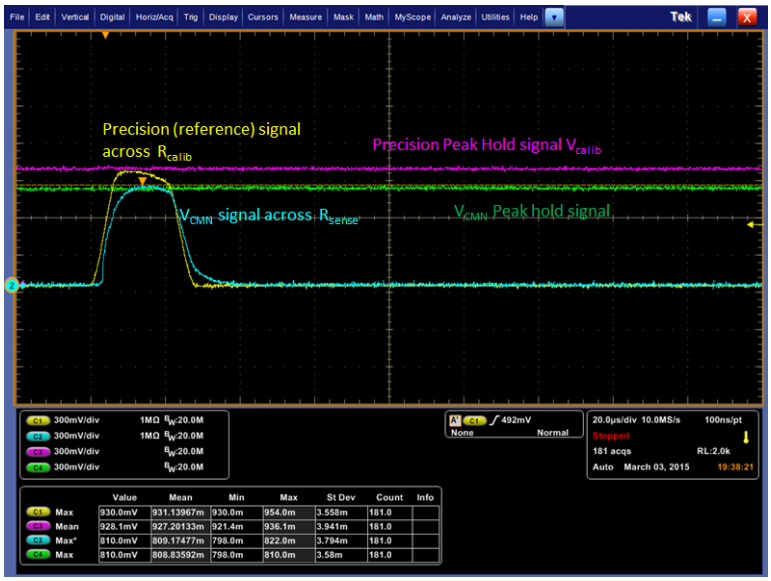


*Fig. 4 Experimental timing diagrams for the calibration circuit.*

The calibration current magnitude used in the experiment was calculated as $I_m = V_{calib}/R_3$. From the scope capture in Fig. 4, the calibration current magnitude was $I_m = 0.81/0.02 = 40.5$ A.

## *Conclusions And Future work*

Experimental results agreed well with the projected levels and prove that the proposed calibration method can provide current monitoring accuracy that is sufficient for practical applications. With this method, the current monitoring error caused by sensor resistance variations does not exceed 1.0%. The method can be deployed for real-time power monitoring, improving accuracy of the CPU IMON signal and enabling nonintrusive fast accurate power virus detection.

Calibrating network power measurements have proven that applying a calibration current at ultra-low duty cycle (0.1% or less) enables high calibration accuracy at an average power consumption below 200 mW. This power level can be considered sufficient for accommodating the circuit on a small PCB footprint and/or making it an integral part of the CPU VR or CPU package, or using it as a miniature pluggable calibration tool.

Next steps for further investigation may include application of the described method for accurate CPU current monitoring in dynamic operating mode and fast detection of power virus events.

**References**

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## About The Author

*Viktor Vogman currently works at Power Conversion Consulting as an analog design engineer, specializing in the design of various power test tools for ac and dc power delivery applications. Prior to this, he spent over 20 years at Intel, focused on hardware engineering and power delivery architectures. Viktor obtained an MS degree in Radio Communication, Television and Multimedia Technology and a PhD in Power Electronics from the Saint Petersburg University of Telecommunications, Russia. Vogman holds over 50 U.S. and foreign patents and has authored over 20 articles on various aspects of power delivery and analog design.*

*For more information on current sensing techniques, see How2Power's Design Guide, and do a keyword search on "current sensing." Also locate the Design Area category and select Test and Measurement.*