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The Engineer's Guide To EMI In DC-DC Converters (Part 6): Mitigation Techniques Using Discrete FET Designs

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Parts 1 through 5 of this article series offer practical guidelines and examples to mitigate conducted and radiated electromagnetic interference (EMI),[1-5] specifically for dc-dc converter solutions with monolithically integrated power MOSFETs.[5] As a sequel to those earlier parts, this article explores EMI abatement in dc-dc regulator circuits that employ a controller driving a discrete pair of high- and low-side power MOSFETs.

An implementation using a controller and external MOSFETs—such as the synchronous buck regulator circuit shown in Fig. 1—offers numerous advantages. These include increased current capability; better thermal performance; and a higher level of flexibility in terms of design choices, component selection and available features. From an EMI perspective, however, a controller solution with discrete FETs is considerably more challenging to design and implement vis-à-vis a converter with integrated FETs.

Two primary considerations apply here. First, the printed circuit board (PCB) layout of a power stage with MOSFETs and controller cannot be as compact as a power converter IC with optimized pinout and internal gate drivers.[5] Second, dead-time management is typically more precise in a converter where the MOSFET switching times are fully characterized. As a result, body-diode conduction times are shorter, leading to improved switching performance and lower noise related to reverse recovery.

This article provides guidelines for laying out a multilayer PCB of a half-bridge design with MOSFETs and controller to achieve excellent EMI performance. The imperative is to minimize critical loop parasitic inductances by careful power-stage component selection and PCB layout. A layout example demonstrates that it's possible to reduce the generation of conducted electromagnetic emissions without sacrificing efficiency or thermal performance metrics.

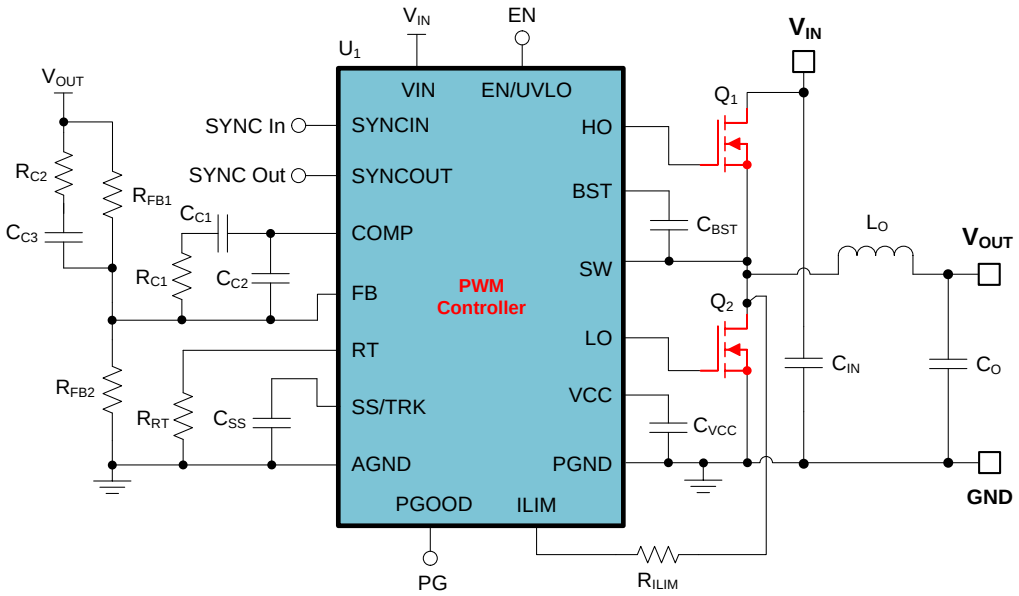


Fig. 1. Schematic of a synchronous buck controller driving power MOSFETs Q_1 and Q_2.

Appreciating The EMI Challenge

Three essential elements must exist for EMI to occur: an electrical noise source, a coupling path and a victim receptor. It's possible to achieve interference suppression and hence electromagnetic compatibility (EMC) by addressing any or all of these aspects. In practice, you can employ several techniques to disrupt coupling paths and/or harden potential victims, such as inserting an EMI filter to suppress the conducted interference and using shielding to mitigate the radiated interference.[4]

The low-frequency EMI spectral amplitude related to a buck regulator's discontinuous input current (or a boost's discontinuous output current) is relatively easy to deal with using a conventional filter stage. However, a greater concern relates to the harmonic content from the high dv/dt and di/dt associated with the sharp edges of voltage and current during switching commutation.

High-current gate drivers (typically integrated in the controller for voltages less than 100 V) can switch power MOSFETs at extremely high speeds. Slew rates greater than 10 V/ns and 1 A/ns are common with conventional silicon FETs, with much higher slew rates possible with gallium nitride (GaN)-based devices. I investigated relationships between the time-domain characteristics of trapezoidal switching waveforms and their spectral content in part 2, explaining that the steepest slope of the waveform determines the high-frequency spectrum asymptotical envelope, and methods to reduce dv/dt and di/dt are thus useful to diminish the EMI generation potential.[2]

In addition to the sharp voltage and current edges, also troublesome is the overshoot/undershoot and subsequent ringing associated with the switching waveforms. Fig. 2 shows the switch-node voltage waveform of a hard-switched synchronous buck regulator. The switch-node voltage ringing frequency ranges from 50 MHz to 250 MHz depending on the resonance of the parasitic power-loop inductance (L_{LOOP}) with the MOSFET output capacitance (C_{OSS}).

Such high-frequency content can propagate by near-field coupling[4] to the output bus, nearby components or the input supply lines, and is difficult to attenuate with conventional filtering. Synchronous MOSFET body-diode reverse recovery presents similar negative effects, exacerbating the ringing voltage as the diode recovery current flows in the parasitic loop inductance.

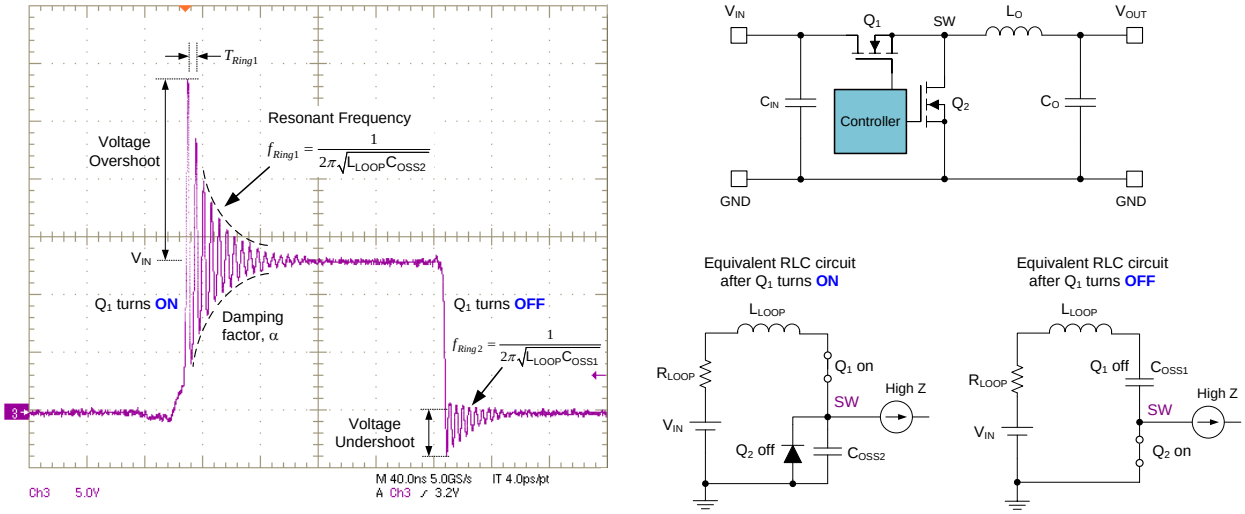


Fig. 2. Switch-node voltage waveform and equivalent circuits during MOSFET turn-on and turn-off transitions for a synchronous buck regulator.

The schematic of Fig. 3 identifies the critical high-frequency power loop of a buck regulator circuit[6] representing circuit elements with high slew-rate current. You can apply a similar examination to boost, inverting buck-boost, SEPIC and other topologies. Minimizing the area of the power loop is essential because of its proportionality to parasitic inductance and related H-field propagation.[3]

The main design goal is to push the resonant frequency of the parasitic LC tank as high as possible by curtailing the parasitic inductance. This decreases the total stored reactive energy and lowers the switch-node voltage peak overshoot and ringing. Also, the equivalent resistance to achieve a critical damping factor is effectively lower, so any ringing decays earlier—especially as the skin effect at high frequencies increases the parasitic resistance of the loop.

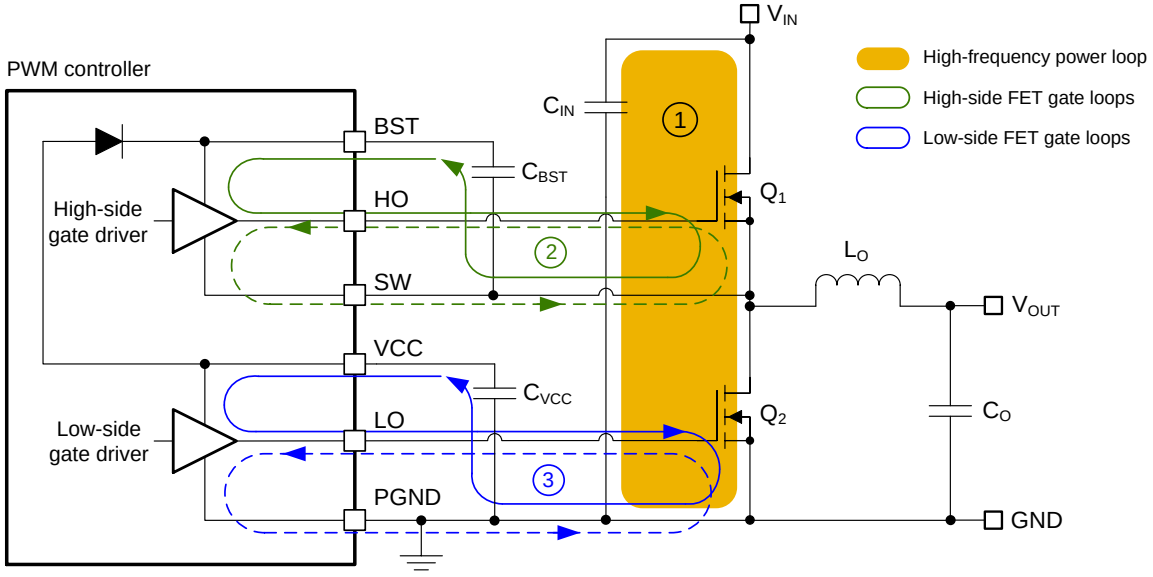


Fig. 3. The high-frequency current loops critical to EMI are identified for a synchronous buck regulator.

Fig. 3 also shows the gate-driver loops of the high- and low-side MOSFETs during turn-on and turn-off. Special considerations during layout of the power stage (discussed next) ensure that the power-loop, gate-loop and common-source parasitic inductances[3] are as low as possible.

PCB Layout Design For Low EMI

The following items summarize the essential guidelines for component placement and PCB layout to achieve the lowest noise and EMI signature in a dc-dc regulator. Some of these steps are similar to those provided in part 5 for a converter design using integrated MOSFETs.[5] Later, I'll provide a PCB layout case study for an EMI-optimized buck regulator.

1. Routing and component placement.
   - Route all power-stage components on the top side of the PCB. Avoid locating the switch-node copper and inductor on the bottom side, where it can radiate to the reference plane of the EMI test setup.
   - Place bypass capacitors for VCC or BIAS close to their respective pins. Ensure that the AGND pin "sees" the C_{VCC} and C_{BIAS} capacitors first before connecting it to GND.
   - Connect the bootstrap capacitor adjacent to the controller's BST and SW pins. Shield the C_{BST} capacitor and switch node with adjacent ground copper to reduce common-mode noise.

2. Ground plane design.
   - Position a layer-2 ground plane in the PCB layer stackup as close as possible to the power-stage components located on the top layer to provide H-field cancellation, parasitic inductance reduction and noise shielding.
   - Use low z-axis spacing between the top layer and second layer ground plane for optimal image plane effectiveness. Specify a 6-mil intralayer spacing in the PCB stackup specification.

3. Input and output capacitors.
   - Place C_{IN} for a buck regulator to minimize the loop area formed by C_{IN} connections to the power MOSFETs. A similar recommendation applies to C_{OUT} for boost and SEPIC regulators. The power loop is classified as lateral or vertical depending on the capacitor placement with respect to the MOSFETs.[6]
   - Ground return paths for both C_{IN} and C_{OUT} should consist of localized top-side planes. Connect dc current routes using multiple external or internal ground planes.
   - Use 0402- or 0603-case size ceramic capacitors with low equivalent series inductance (ESL) located close to the MOSFETs to minimize power-loop parasitic inductance.

4. Inductor and switch-node layout.
   - Place the inductor close to the MOSFETs. Minimize the switch-node copper polygon area to reduce capacitive coupling and common-mode current. The copper should occupy just the inductor pad and the minimum area required to connect to the MOSFETs' terminals.
   - Confine switch-node noise using adjacent ground guarding and via shielding.
   - Check the inductor's dot position to ensure that the end of the winding tied to the switch-node is on the bottom and inside of the winding geometry and shielded by the outer turns of the winding connected to VOUT (for a buck) or VIN (for a boost).
   - Select an inductor with terminations underneath the package. Avoid large vertical sidewall terminations that can act as a radiating antenna.
   - Use an e-field-shielded inductor if possible. Connect the shield terminals to the PCB ground plane.

5. Gate-drive trace layout.

Locate the controller as close as possible to the power MOSFETs while performing the following steps:
   - Route gate-drive traces for HO and SW differentially with minimal length and loop area directly to the high-side MOSFET gate and source terminals.
   - Route the gate-drive trace for LO directly to the low-side MOSFET gate above a ground plane with minimal dielectric spacing.
   - Minimize coupling from the power loop to the gate loops by orthogonal routing of the gate-drive traces.[6]

6. EMI management
   - Route the EMI filter components to avoid coupling from the electric field radiated by the inductor and switch node. Place the EMI filter on the opposite side of the board from the converter if it cannot be sufficiently separated from the power stage.
   - Place cutouts on all layers below the EMI filter to prevent parasitic coupling paths impacting the filter's attenuation characteristic.
   - Place a boot resistor (preferably less than 10 Ω) in series with C_{BOOT}, if needed, to limit the MOSFET turn-on speed, reducing the switch-node voltage slew rate, overshoot and ringing. The boot resistor changes the drive-current transient rate and thus reduces the switch-node voltage and current slew rates during MOSFET turn-on. For added flexibility, consider using a controller with dedicated source and sink pins for the gate driver(s).
   - Any required switch-node snubber circuit should occupy a minimum loop area based on its transient current spike at each switching transition. Connect the smallest footprint component to SW (usually the capacitor) to minimize its antenna effect.
   - Use a multilayer PCB with inner ground planes to achieve much improved performance relative to a two-layer design. Avoid disruption of the high-frequency current paths near the MOSFETs.
   - Consider using metal case shielding to optimize radiated EMI performance. The shield covers all power-stage components except the EMI filter and is connected to GND on the PCB, essentially forming a Faraday cage with the PCB ground plane.

Case Study Of A DC-DC Synchronous Buck Controller

Fig. 4 shows the schematic of a synchronous buck converter circuit[6] intended for automotive or noise-sensitive industrial applications. The controller IC incorporates several included features for improved EMI performance,

including constant switching frequency operation, external clock synchronization and switch-node shaping (slew-rate control) by controlled high-side MOSFET turn-on.[7]

To help translate to an optimized PCB layout, the schematic highlights the high-current traces (VIN, PGND, SW connections), noise-sensitive nets (FB, COMP, ILIM) and high dv/dt circuit nodes (SW, BST, HO, LO, SYNC). The high di/dt loops are similar to those identified in Fig. 3.

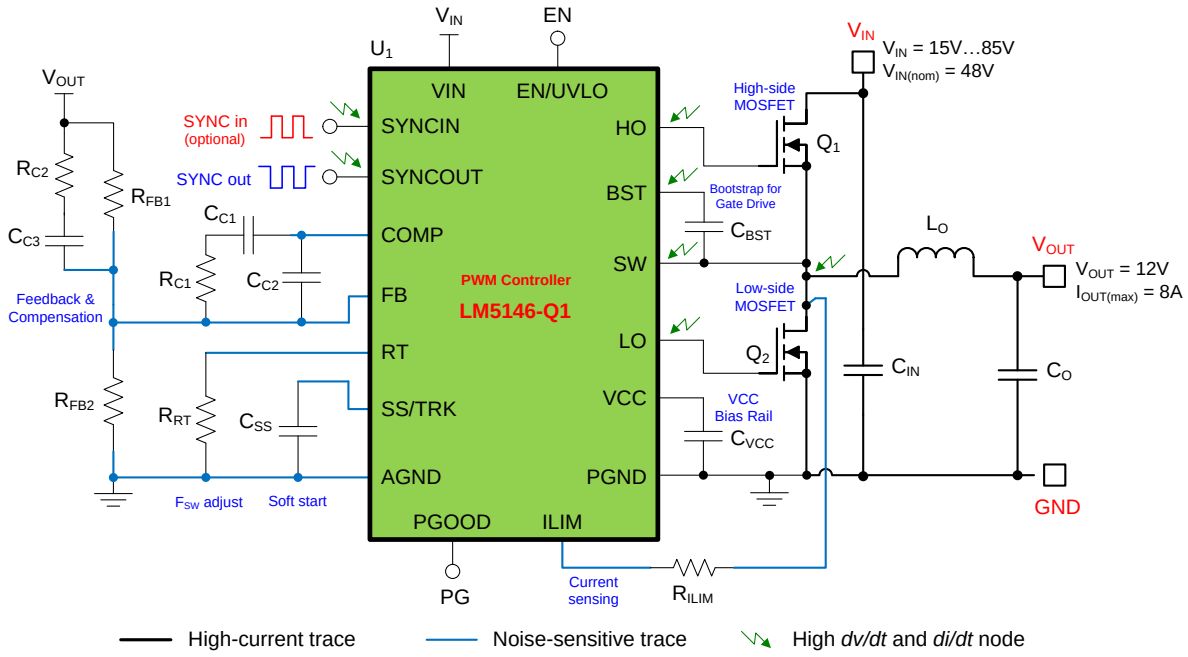
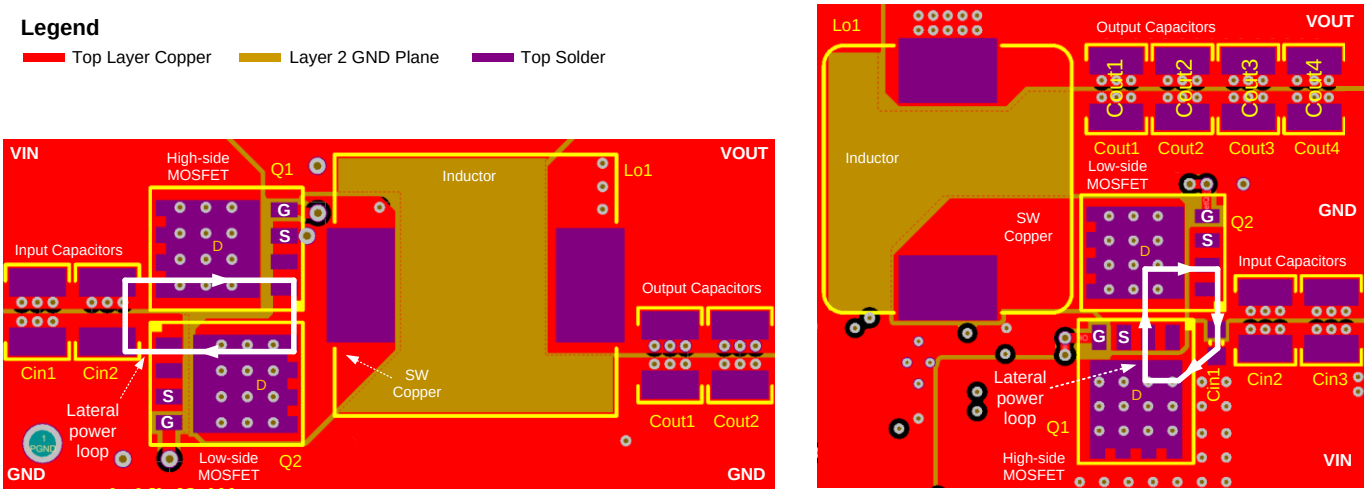


Fig. 4. Schematic of a buck regulator with important nodes and traces identified for PCB layout.

Fig. 5 shows two lateral loop arrangements of power MOSFETs and input capacitors. The power stage is on the top layer of the PCB with the controller placed on the bottom. The lateral loop design has a circulating current on the top layer (denoted by the white border in Fig. 5) that induces an image current on the layer-2 ground plane to achieve flux cancellation and thus lower parasitic loop inductance.

More specifically, the layout in Fig. 5b is modified so that the high-side FET (Q1) is rotated 90 degrees. This improves heat sinking of Q1 for better thermal management and allows convenient placement of a low-ESL capacitor (Cin1) in an 0603-case size near the MOSFETs for high-frequency decoupling. The U-shaped layout orientation of the power-stage components positions the output capacitors for a shorter return connection to the low-side MOSFET.



(a) (b)

Fig. 5. Two conventional lateral-loop layout designs.

Improved PCB Layout Design

Fig. 6 shows an improved layout with the benefit of a reduced power loop area and high efficiency for a multilayer structure. The design uses layer 2 of the PCB as a power-loop return path.[7,8,9] This return path is located directly underneath the top layer, creating a small physical loop size. The currents flowing in opposing directions in the vertical loop provide field self-cancellation, further reducing parasitic inductance. The side view depicted in Fig. 6 illustrates the concept of creating a low-profile self-canceling loop in a multilayer PCB structure.

Four 0603-input capacitors with small 0402 or 0603 case size and low ESL (C_{IN1} through C_{IN4}, located between bulk input decoupling capacitors C_{IN5} and C_{IN6} in Fig. 6) are placed as close as possible to the high-side MOSFET. The return connections of these capacitors are connected to the layer-2 ground plane with multiple 12-mil vias. The layer-2 ground plane provides a current return path directly underneath the MOSFETs to the source terminal of the low-side MOSFET.

In addition, the switch-node copper polygon includes just the pad of the inductor and the minimum area required to connect to the MOSFETs. Ground plane copper shields the polygon pour connecting the MOSFETs to the inductor terminal. The single-layer layout for SW and BST implies that vias with high dv/dt do not appear on the bottom side of the PCB. This avoids e-field coupling to the reference ground plane during the EMI test.

Finally, using two ceramic output caps, C_{OUT1} and C_{OUT2}, on each side of the inductor optimizes the output current loops. Having two parallel return paths from the output splits the return current in two, helping mitigate the "ground bounce" effect.

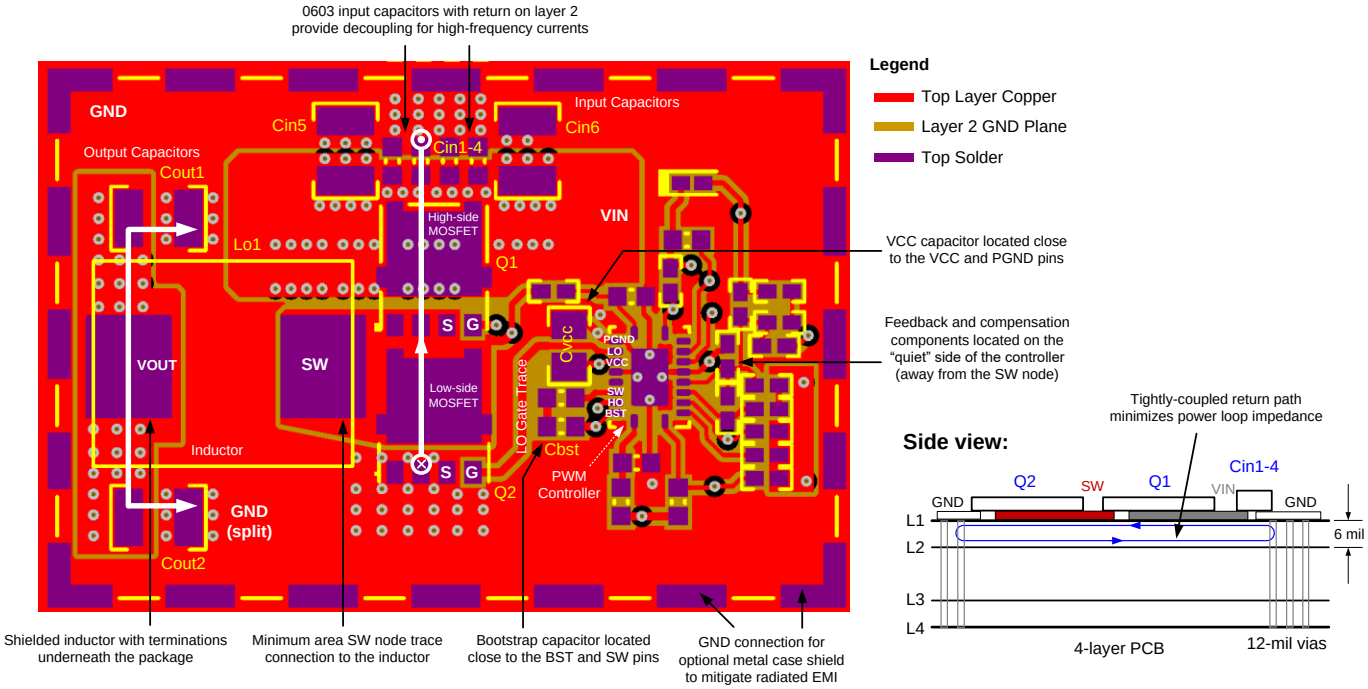


Fig. 6. Layout of power stage and controller with an optimized vertical power-loop design.

Fig. 7a shows the switch-node voltage waveform measured with a wide-bandwidth probe for the regulator in Fig. 4 using the optimized layout of Fig. 6. Ringing is not evident, just a low-amplitude overshoot and negligible undershoot, which bodes well for EMI performance above 50 MHz. For comparison, Fig. 7b shows a similar measurement using the lateral loop layout of Fig. 5b. The peak overshoot of the optimized layout is lower by approximately 4 V.

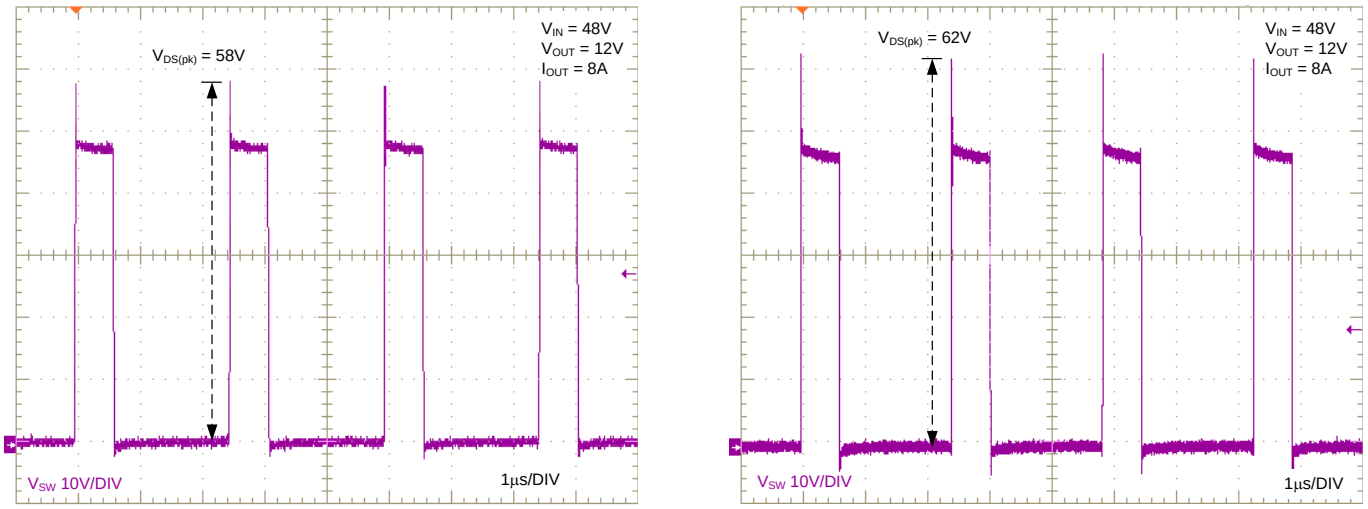


Fig. 7. Switch-node voltage waveforms at V_{IN} = 48 V and I_{OUT} = 8 A, optimized layout (a); lateral loop layout (b).

Fig. 8 shows the conducted emissions measured from 150 kHz to 108 MHz for the regulator in Fig. 6. Using a Rohde & Schwarz spectrum analyzer, peak and average detector scans are denoted in yellow and blue,

respectively. The results are in compliance with CISPR 25 Class 5 requirements. The limit lines in red are the Class 5 peak and average limits (peak limits are generally 20 dB higher than the average limits).

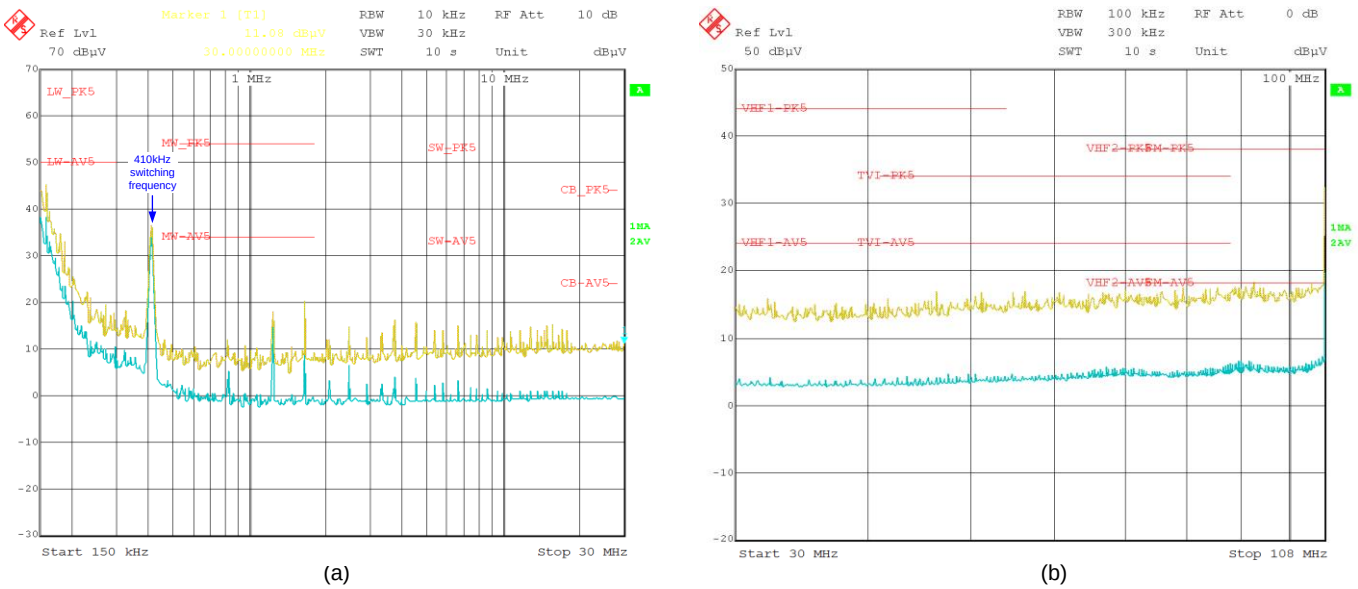


Fig. 8. CISPR 25 conducted emission results, 150 kHz to 30 MHz (a) and 30 MHz to 108 MHz (b).

Summary

The switching transients of power semiconductor devices are the chief sources of both conducted and radiated EMI. This article highlights PCB layout for lower EMI in dc-dc regulator circuits that use a controller with external MOSFETs.

The essential layout recommendations are to minimize the current "hot loop" area in the layout; avoid disruption of the current path; use a multilayer PCB with inner ground planes for shielding (yielding much better performance than a two-layer PCB); route short, direct gate-drive traces as differential pairs; and use a minimal switch-node copper area to reduce e-field radiated coupling.

An optimized PCB layout can help improve a regulator's EMI signature (without the sacrifice of efficiency or thermal performance associated with other "fixes" commonly used to reduce EMI). While this discussion centers around an EMI-aware synchronous buck power stage, you can generally extend the concepts to any dc-dc regulator as long you identify the critical loops and implement the recommended layout techniques.

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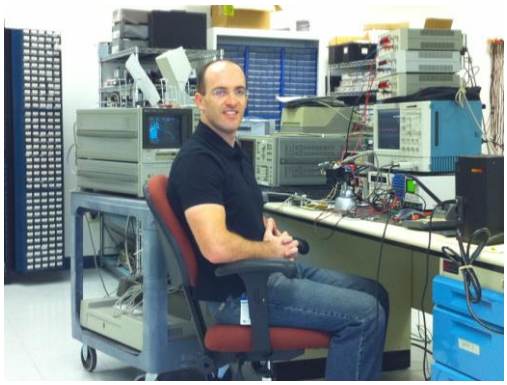
About The Author



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For more information on EMI, see How2Power's Power Supply EMI Anthology. Also see the How2Power's Design Guide, locate the Design Area category and select "EMI and EMC".