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Options For Optimizing PFC Efficiency Over Wide Load And Line Ranges

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Environmental concerns lead to new efficiency requirements when designing modern power supplies. For instance, the 80 PLUS initiative and moreover its Bronze, Silver or Gold derivatives[1] force desktops and servers manufacturers to work on innovative solutions. An important focus is on the power factor correction (PFC) stage together with the EMI filter can consume 5% to 8% of the output power at low line, full load.

In general, relevant devices do not permanently operate at the maximum power they are designed for—they only operate at such levels for short periods of time. Hence, for effective power savings, "green requirements" do not only target the full-load efficiency. Instead, they tend to cope with the actual operating conditions by specifying minimum levels for either the averaged efficiency or for the efficiency ratios at different loading scenarios such as 20%, 50% and 100% of the full power.

As a result, full- but also medium- and light-load efficiency ratios have become critical points to address in designing PFC stages. After a basic overview of the power factor correction topic, this article will first discuss the efficiency "nibblers"—the factors that degrade efficiency. The impact on efficiency of these nibblers, relative to one another, is not the same at low, medium and full load and also varies with line voltage. Hence, it will be seen that the PFC stage cannot be operated the same way over all operating conditions when high-efficiency ratios are sought over wide line and load ranges.

Instead, as discussed in the second section of this article, the controller algorithm needs to adapt the operating mode of the PFC stage to the line and load conditions. This is a multimode approach. In the third and final section, architectural aspects of PFC stages will be considered with a focus on the bridgeless and interleaved approaches. Respective merits of these solutions will be compared in a 300-W, wide-input-voltage application.

A Review Of PFC Basics

The line utility provides a sinusoidal voltage but the shape and phase of the line current depend on the load. If the load is resistive, the line current is proportional to the input voltage. Therefore, it is sinusoidal and in phase with the line voltage. In this case, we can easily compute the active power (also named average or real power) by integrating the instantaneous power over the line period and see that it equals the apparent power that is, the line rms voltage multiplied by the line rms current:

$$P_{in,avg} = P_{apparent} = V_{line,rms} \cdot I_{line,rms} \quad (1)$$

Now, if the load further consists of a storage element (a capacitor and/or an inductor), the line current will remain sinusoidal but a phase shift will occur as illustrated by Fig. 1a. As result, the active power is lower than the apparent power by a factor which is the cosine of the phase angle:

$$P_{in,avg} = V_{line,rms} \cdot I_{line,rms} \cdot \cos(\phi) \quad (2)$$

where $\cos(\phi)$ is the displacement factor.

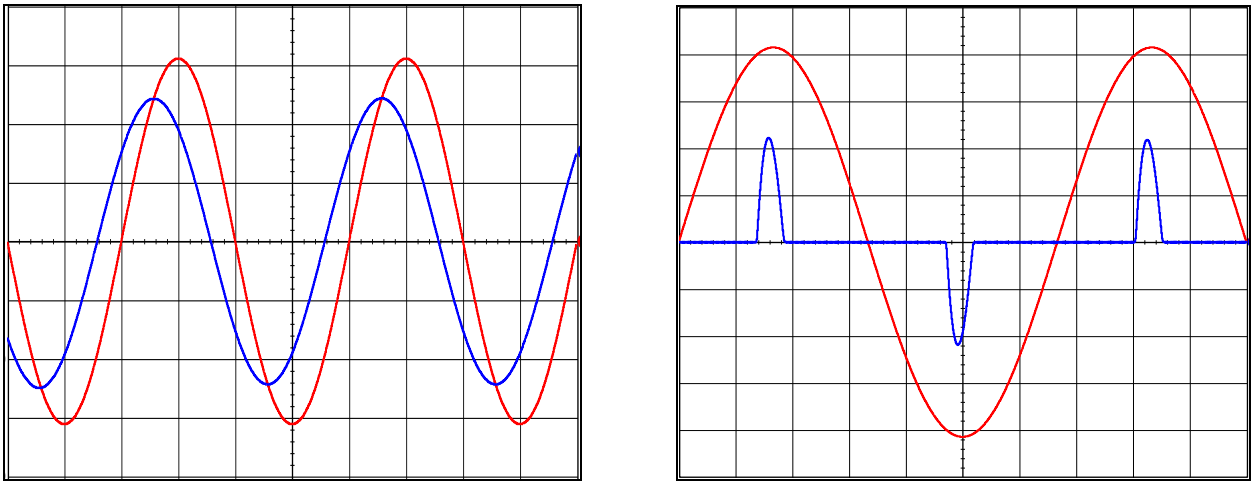


Fig. 1. Line voltage (blue) and line current (red) in the case of a reactive load (left) and of a non-linear load (right).

Let us further assume a non-linear load, typically, as illustrated in Fig. 2, a diode bridge followed by a large bulk capacitor to provide a rough dc voltage. In this case, the current is not sinusoidal anymore but consists of inrush current spikes near the line sinusoid peak (see Fig. 1b). The current being nonlinear, the power computation can be made by using its breakdown into Fourier series.

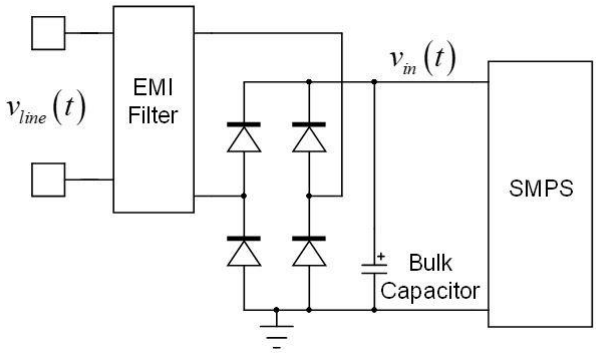


Fig. 2. The shape and phase of the line current depend on the load.

Now, averaging the product of two sinusoids gives zero except if the two signals have the same frequency. In other words, only the fundamental component provides real power. Other harmonic currents circulate needlessly and just contribute to an increased circulating current. As a result, assuming that the fundamental is not phase shifted, the active power is affected by a coefficient cos(θ), which is the distortion factor:

$$P_{in,avg} = V_{line,rms} \cdot I_{line,rms} \cdot \cos(\theta) \quad (3)$$

As a result, if the line current is both phase-shifted and distorted, the real power suffers from both the distortion and the displacement factors:

$$P_{in,avg} = V_{line,rms} \cdot I_{line,rms} \cdot \cos(\phi) \cdot \cos(\theta) \quad (4)$$

The power factor is the product of the displacement factor (less than 1 if the line current and voltage are not in phase) by the distortion factor (less than 1 if the line current is not sinusoidal).

$$PF = \cos(\phi) \cdot \cos(\theta) \tag{5}$$

Thus PF connects the apparent power to the real power as follows:

$$P_{in,avg} = V_{line,rms} \cdot I_{line,rms} \cdot PF \tag{6}$$

If the line voltage is assumed to be the well-controlled sinusoidal voltage generally provided by the electricity utility, you can immediately see that the line current will be inversely proportional to the PF for a given power demand:

$$I_{line,rms} = \frac{P_{in,avg}}{V_{line,rms} \cdot PF} \tag{7}$$

Low power factor ratios are thus indicative of useless reactive currents flowing in the distribution network. As highlighted by equation (7), this causes the line rms current and hence, the conduction losses to be increased. This also limits the power which can be absorbed from an outlet. For instance, if PF = 0.5, the line rms current is doubled compared to its value when PF is 1, thus limiting by 2 the power one can draw from a 16-A electric socket!

We can further note that the distortion factor is linked to the total harmonic distortion (THD):

$$\cos(\theta) = \frac{1}{\sqrt{1+THD^2}} \tag{8}$$

Commonly expressed as a percentage, the THD is an important method in determining the harmonic quality of the current absorbed from the ac mains or ac grid. Practically, it is computed as the square root ratio of the sum of the squares of all other harmonics to the square of the fundamental component. In other words, it gives the relative weight of the unwanted harmonic content with respect to the fundamental:

$$THD(\%) = 100 \cdot \sqrt{\sum_{p=2}^{\infty} \frac{I_p^{\,2}}{I_1^{\,2}}} \tag{9}$$

If there is no phase shift (which is generally true for switch-mode power supplies as long as the EMI filter reactance is ignored), the relationship between the power factor and THD is fairly straightforward:

$$PF = \cos(\theta) \cdot \cos(\phi) = \cos(\theta) = \sqrt{\frac{1}{1+THD^2}} \tag{10}$$

The EN 61000-3-2 specification, usually referred to as the power factor correction (PFC) standard, has been issued with the goal of minimizing the THD of the current that is drawn from the grid. In practice, the legislation specifies a maximum harmonic magnitude from the second harmonic up to the 40th order. Please note that in

addition to the EN 61000-3-2 norm, PF is also specified in other specifications like Energy Star, which contributes greatly to the widespread use of power factor correction. Other standards exist for applications with input currents >16 A (e.g., EN 61000-3-12) and for specific applications like aircraft.

Active solutions are the most effective means to meet these legislative requirements. As illustrated in Fig. 3, a PFC pre-regulator is inserted between the input bridge and the bulk capacitor. This intermediate stage is designed to deliver a constant voltage while drawing a sinusoidal current from the line. In practice, the stepup (or boost) configuration is adopted, because this type of converter is robust and easy to implement. Obviously this topology requires the output to be higher than the input voltage. That is why the output regulation level is generally set to around 400 V for universal input (85 to 264 Vac).

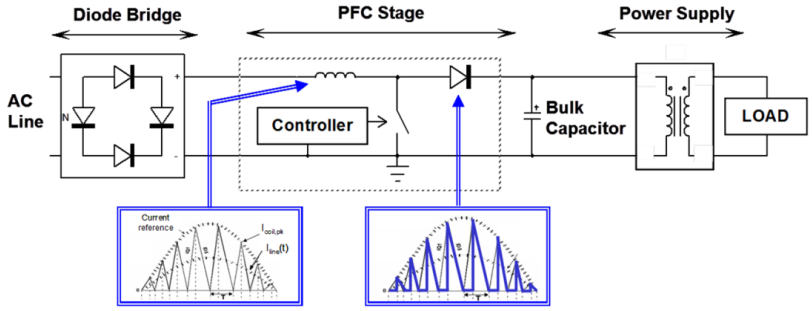


Fig. 3. Power factor corrected power converter.

This additional stage simplifies the design of the main downstream converter by providing it with a narrow input voltage. Also, the high-voltage dc-link (bulk) capacitor helps meeting hold-up time requirements while the non-pulsating input current of a boost converter eases EMI filtering. However, as aforementioned, efficiency is a major requirement for modern power supplies. A PFC pre-converter is the seat of some losses which must be mitigated to meet today specifications.

Fig. 4 reports the efficiency performance of a 300-W, wide-input PFC stage driven by the NCP1654 power factor controller from ON Semiconductor.[2] The efficiency of a PFC boost converter is generally worse at low line. Reference [3] instructs that an efficiency chart generally shapes as a bell curve peaking at an intermediate load level. From this peak, the efficiency decays when the load rises because of the conduction losses while on the light-load side, it diminishes due to the constant and switching losses.[4]

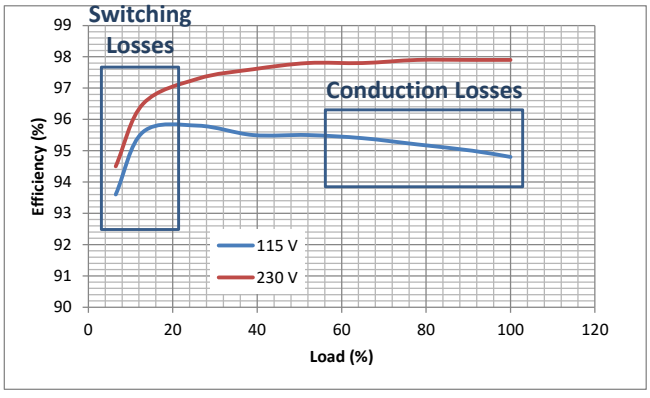


Fig. 4. Efficiency over the load range of the NCP1654 PF controller evaluation board.

We can identify two types of losses—conduction and switching losses. The conduction losses increase as the load rises. Some of them are approximately proportional to the input power. Typically, these are those caused by diode forward voltage like in the input bridge as discussed later. Since they are a nearly constant portion of the input power, their impact on the efficiency is constant over the load range.

Others are proportional to the square of the input current and hence at a given line level, to the square of the power. They consist of the dissipation of all the resistances present in the current path including the EMI filter parasitic resistances and the boost inductor ac resistance, the MOSFET on-time resistance, the current-sensing resistance and the bulk capacitor equivalent series resistance. Being proportional to the input power square, the negative impact of these losses on efficiency dramatically increases as the load rises. They typically cause the low-line, heavy-load efficiency drop shown in Fig. 4. If we omit those incurred by the EMI filter, these losses are highly dependent on the inductor current ripple.

Then, we have the switching losses, which have multiple components. One type is the energy lost when the current transitions from the power switch to the boost diode and vice versa. These losses are proportional to the current which is switched and to the switching frequency. They also depend on transition delays which result from non-idealities of components (parasitic capacitances and current charge necessary to force the recovery of a diode—Q_{rr}). These losses are proportional to the current and have a generally constant impact of the efficiency over the load if the frequency is fixed. The impact dramatically worsens in CrM since the switching frequency rises under light-load conditions.

Another form of switching losses stems from the energy necessary to manage the switching-mode power transfer, with mainly the commutation of the switching cell. These losses, which are designated as constant losses in reference [4], are independent of the current which is driven. For instance, the power necessary to drive the power switch can be expressed for a MOSFET as

$$P_{drive} = V_{CC} \cdot Q_g \cdot f_{sw}$$

where V_{CC} is the voltage applied to the MOSFET gate, Q_g is the total gate charge necessary to charge the gate to V_{CC} and f_{sw} is the switching frequency.

Also, the losses produced at turn-on by the discharge of the MOSFET output capacitance are independent of the processed current unless a specific control law is in play. As such, they can be considered independent of the load and as a result, their impact on efficiency is generally minor at full load while considerably increased at light load. The degradation is even worse if the switching frequency increases at light load as with critical conduction mode circuits since the losses are no longer constant but rising in the low-power range.

Yet another form of switching losses are the magnetic core losses, which to some extent, could be included in the preceding category of losses independent of the current which is driven in continuous (CCM) and critical (CrM) conduction modes since the Steinmetz's equation

$$\left(P_c = k \cdot {f_{sw}}^{\alpha} \cdot (\Delta B)^{\beta}\right)$$

shows a dependence on only the magnetic field swing and switching frequency, which are both constant in CCM and the variations of which tend to cancel in CrM.

To these losses, we can add the permanent power consumed by the PFC controller (V_{CC} consumption) and the dissipation caused by the different biasing currents like those of the high-voltage sensing networks. These losses can be a problem if high efficiency ratios are required at very low power.

The full-load losses of a PFC boost converter should be mainly considered at the lowest line level where the efficiency is worse. The thermal management and power component selection will largely depend on them. Thus, based on the above rapid overview of efficiency nibblers, it appears that switching losses must be controlled at light load while the conduction losses are to be contained at full load, low line.

We will see in the next sections how PFC control schemes and architectures can help optimize the operation to reach this goal.

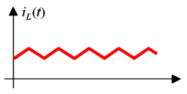
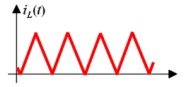
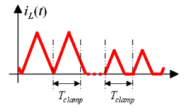
One-Channel PFC Typical Operation Modes

Table 1 summarizes the basic control schemes in play in a PFC stage. First, the continuous conduction mode (CCM) consists of limiting the inductor current ripple at the cost of losses during the power switch turn-on. Traditionally operated at a fixed switching frequency, CCM is generally used for applications of 300 W or more.

Critical conduction mode (CrM) consists of starting a new switching cycle when the inductor current has reached zero. As a result, CrM saves the need for a fast-recovery diode to contain turn-on losses. On the other hand, the switching frequency is essentially variable and the current ripple is large. CrM is very popular for lighting and other lower-power applications. CrM controllers are simple and inexpensive.

However, a variation on CrM known as frequency-clamped critical conduction mode (FCCrM) is an approach introduced years ago by ON Semiconductor to limit the switching frequency spread of CrM circuits. A maximum frequency clamp forces a change to discontinuous conduction mode (DCM) when the converter operates in light-load and/or near the line zero crossing. Without this circuitry, the CrM switching frequency would exceed the upper clamp threshold, naturally increasing switching losses. With FCCrM, a circuit is added to compensate the DCM-induced deadtimes so that the line current continues to have the desired shape.

Table 1. Operating mode overview.

	Operating Mode	Main Features
	Continuous Conduction Mode (CCM)	Always hard-switching Inductor value is largest Minimized rms current
	Critical conduction Mode (CrM)	Large rms current Switching frequency is not fixed
	Frequency Clamped Critical conduction Mode (FCCrM)	Large rms current Frequency is limited Reduced coil inductance

Further details on these modes of operation can be found in reference [5]. The best usage of these modes with respect to efficiency will be discussed in the next sections. But in general, CrM is very popular up to 300 W. The availability of inexpensive and low-$R_{DS(on)}$ power switches tends to extend its power range. In the discussions which follow, we will use CrM as the default operating mode.

Basics Of The Critical Conduction Mode

Fig. 5 sketches an inductor current cycle of a CrM PFC. The inductor current ramps to twice the desired average value, ramps down to zero, then immediately ramps positive again.

The PFC stage adjusts the amplitude of the obtained current triangles so that the inductor averaged current is the wished haversine. The EMI filter performs the filtering function.

The inductor peak current is:

$$I_{L,pk} = i_{L,pk}(t) = \frac{v_{in}(t) \cdot t_{on}}{L} \qquad (11)$$

The line instantaneous current is the average value of the triangle peaking to $I_{L,pk}$. Hence:

$$i_{line}(t) = \left\langle i_L(t) \right\rangle_{T_{sw}} = \frac{i_{L,pk}(t)}{2} = \frac{v_{in}(t) \cdot t_{on}}{2 \cdot L} \qquad (12)$$

One can deduce from equation (12) the two traditional ways to control the triangle's magnitude and shape the current:

- Generating a sinusoidal reference and forcing the inductor peak current to follow this sinusoidal envelope. This is the current-mode approach.
- Dictating a constant on-time. This is the voltage-mode approach.

As detailed in reference [6], in both cases, the regulation loop bandwidth is set low so that its output is a slow-varying signal which can be considered as a constant within a half-line cycle. It can then be used to control the on-time or generate the sinusoidal reference by multiplying it with a portion of the input voltage.

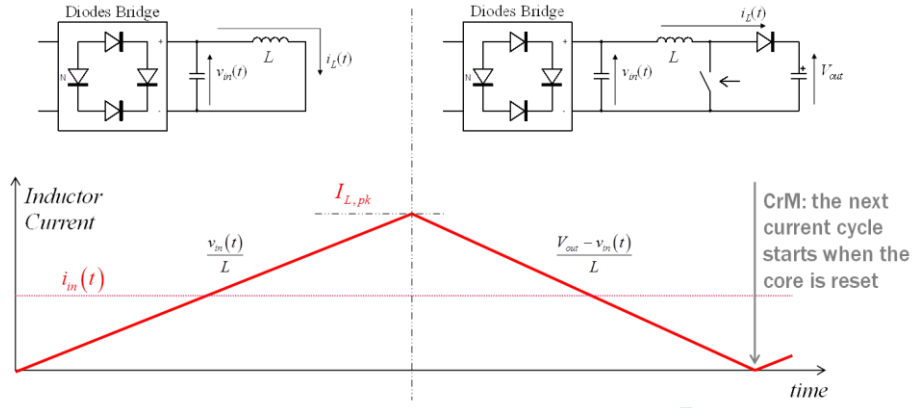


Fig. 5. Switching sequences of a CrM PFC stage.

Besides its simplicity and ruggedness, one major merit of CrM is its minimized turn-on losses. First, the boost diode naturally opens as its current vanishes. Hence, there is no reverse-recovery charge (Q_{rr}) to worry about. In addition, the power switch is not turned on immediately when the inductor current reaches zero. Instead, as detailed in reference [7], the closing is delayed for a time t_d of typically a few hundreds of nanoseconds.

During this delay, the oscillating network consisting of the inductor and of the switching-node lumped capacitance makes the power switch voltage swing around the input voltage. As shown in Fig. 6, the power switch closes at the end of t_d when the valley is reached. The turn-on losses are thus minimized since the valley voltage is as low as ($2V_{in}(t) - V_{out}$) when the instantaneous input voltage is higher than ($V_{out}/2$). If ($v_{in}(t) < V_{out}/2$), zero-voltage-switching is even obtained.

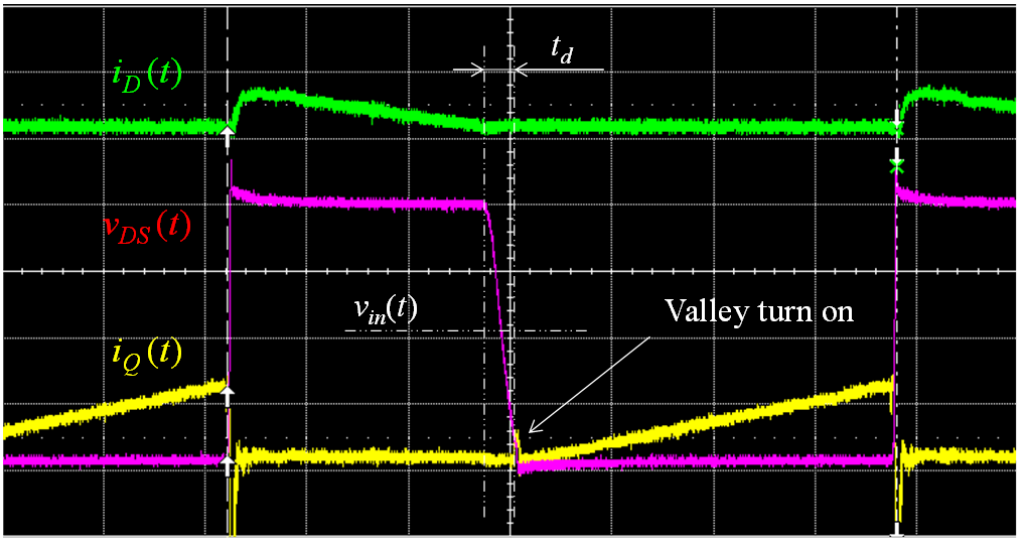


Fig. 6. Valley turn-on of the MOSFET (measured on the NCP1612 PF controller evaluation board).

On the other hand, CrM has two major inconveniences. For one, the inductor current ripple is large, thus leading to bulky input/output current filters. The ripple also implies, high rms currents within the boost converter and large copper/core losses within the inductor. This limits the cost-effectiveness and practical use of the solution for high-power applications.

The switching frequency is variable and can reach high values, particularly under light-load conditions, thus, altering the efficiency in this mode. The following equation provides a simplified expression (in which the delay to reach the valley is neglected) of the switching frequency as a function of the line voltage and of the input power:

$$f_{sw}(t) = \frac{V_{in,rms}^{\ 2}}{2 \cdot L \cdot P_{in,avg}} \cdot \left(1 - \frac{v_{in}(t)}{V_{out}}\right) \qquad (13)$$

As will be seen in the next section, the rise of the switching frequency dramatically pulls efficiency down in light-load conditions. Unfortunately, the degradation can only be mitigated by the use of large inductors.

DCM Operation: a Good Idea?

Reference [7] explains that clamping the switching frequency of a CrM PFC stage causes a dramatic line current distortion unless additional circuitry is added. ON Semiconductor has released several controllers like the NCP1612 or the NCP1632 which purposely embed such proprietary circuitry.

In practice, these controllers sense the deadtime generated in the preceding switching cycles and based on this input, increase the on-time so that the averaged value of the current over one switching period remains what it would be in CrM. As Fig. 7 illustrates, to maintain the same line current, we need a CrM peak current of $(I_{L,pk})_{CrM}$ while a higher one ($(I_{L,pk})_{DCM}$) is necessary in DCM and:

$$i_{line}(t) = \frac{\left(I_{L,pk}\right)_{CrM}}{2} = \frac{\left(I_{L,pk}\right)_{DCM}}{2} \cdot \frac{t_{on,DCM} + t_{demag,DCM}}{T_{SW,DCM}} \qquad (14)$$

where $t_{on,DCM}$ is the on-time of the considered DCM cycle, $t_{demag,DCM}$ is the demagnetization phase corresponding to $t_{on,DCM}$ and $t_{SW,DCM}$ is the DCM switching period.

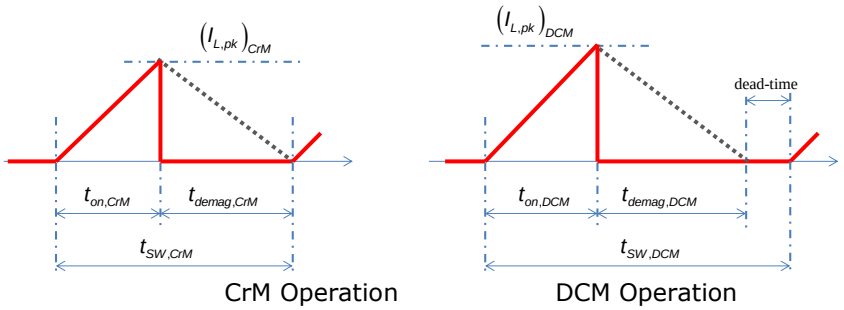


Fig. 7. Power switch current in CrM (left) and DCM (right) for a PFC stage employing FCCrM.

Note that the system is auto-adaptive in the sense that within a half-line cycle, the system can transition between CrM (typically at the top of the sinusoid) and DCM (typically near the line zero crossing) with no discontinuity in operation and no PF degradation. Simply, the on-time will be higher in DCM cycles and recovers its CrM duration when there are no deadtimes. This ON proprietary scheme is named frequency-clamped critical conduction mode (FCCrM). This control scheme can further support forms of frequency foldback like the gradual decrease of the switching frequency as a function of the load (NCP1631), the current-controlled frequency foldback (NCP1611/2) or the valley-switching frequency foldback (NCP1602/22).

The current shapes in Fig. 8 suggest that the DCM mode causes higher conduction losses. Reference [8] shows that clamping the switching frequency at too low a level can be counterproductive. In practice, the optimal frequency reduction, expressed as a percentage of the CrM switching frequency, is the ratio of the switching losses to the conduction losses when the converter operates in CrM. This means that if α is the ($f_{SW,CrM}$ over $f_{SW,DCM}$) ratio, where $f_{SW,DCM}$ is the DCM switching frequency and that $f_{SW,CrM}$ is the switching frequency if CrM operation was maintained, the optimal value for α is:

$$\alpha_{opt} = \frac{(P_{SW})_{CrM}}{(P_{cond})_{CrM}} \qquad (15)$$

where $(P_{SW})_{CrM}$ and $(P_{COND})_{CrM}$ are respectively the switching and conduction losses of the PFC stage when operated in CrM. Because switching losses are difficult to predict, it is therefore difficult to theoretically and accurately find α_{opt}. Anyway, this means that since conduction losses are produced by the input current, the input current is a convenient parameter to use to control the frequency foldback.

Following these efficiency considerations, ON Semiconductor has released several parts (NCP1611/2/5/6) to drive PFC boost stages using the so-called Current Controlled Frequency Foldback (CCFF). In this mode, the PFC stage operates in traditional critical conduction mode when the line current exceeds a programmable value. Conversely, when the current is below this preset level, the switching frequency decays down towards about 20 kHz as the line current reduces to zero.

Fig. 8 shows how CCFF can reduce the switching frequency. These plots were obtained using the NCP1612 evaluation board.[9] The circuit lengthens the deadtime when the line current becomes smaller as it gets closer to the line zero crossing. Finally, a CCFF boost stage is intended to operate in CrM under heavy line current conditions and as the line current reduces, the controller enters DCM operation. By the way, even in DCM, the MOSFET turn-on is stretched until its drain-source voltage is at its valley for an optimal power saving.

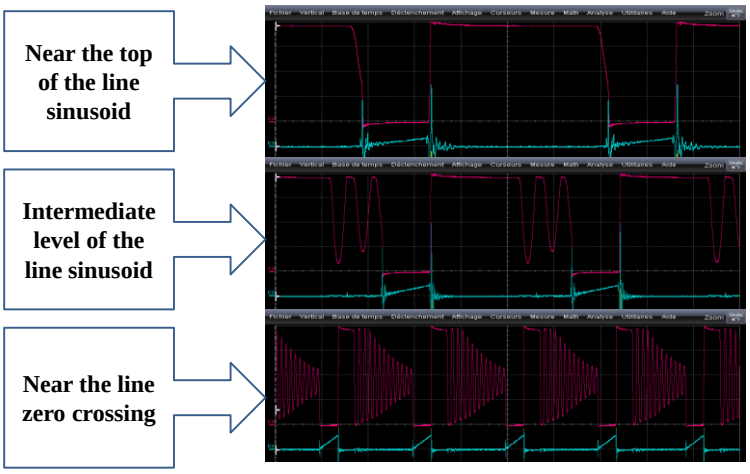


Fig. 8. Operation at 230 V, 160 W near the line zero crossing of the NCP1612 evaluation board. The MOSFET drain-source voltage is in red, while the blue trace shows the MOSFET current.

Fig. 9 reports data detailed in reference [9] obtained using the NCP1612 evaluation board. The CCFF efficiency is compared to that of a pure CrM circuit on the same board (by inhibiting the NCP1612 CCFF function). In addition, the NCP1612 can skip cycles near the line zero crossing where the current is very small (green trace).

The efficiency ratios were measured at low and high line over a large power range (from 5% to 100% of full load). The right-hand side of the CCFF efficiency curves resembles that of a traditional CrM PFC stage. On the left-hand side, the efficiency normally drops because of the switching losses until an inflection point where it rises up again as a result of the CCFF operation.

As previously detailed, CCFF makes the switching frequency decay linearly as a function of the instantaneous line current when it goes below a preset level. The CCFF threshold was set to about 20% of the line maximum current at low line and to nearly 45% at high line as confirmed by the aforementioned inflection points observed in Fig. 9. Thus, CCFF significantly improves efficiency below 20% of the load at low line while some benefit starts to become visible starting below 50% of the load at 230-V input.

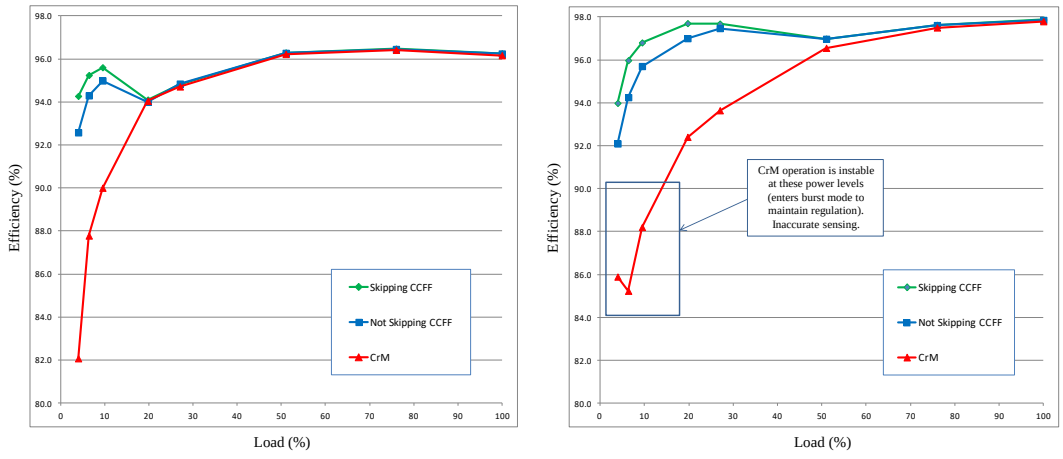


Fig. 9. Efficiency over the load range at low- and high-line conditions.

Hence, frequency foldback is a very effective means of improving the light-load efficiency. Note that the control of the switching frequency brings two other major benefits.

Because of the propagation delays in the power switch control chain and the high switching frequency, CrM PFC stages generally cannot maintain continuous operation below 20% of the load when operating at the highest line levels. Instead, they enter a burst-mode of operation. It can cause audible noise and the board may fail to pass THD specifications. Fig. 9 illustrates that reducing the switching frequency solves this limitation. Thus, it should be noted that CrM PFC circuits with frequency foldback (like the CCFF circuit in Fig. 9) feature stable operation down to extremely low power levels.

In the absence of frequency clamp or frequency foldback, the only way to improve the light- and even medium-load efficiency is to increase the inductor value to lower the CrM switching frequency (since as indicated by equation (13), the switching frequency is inversely proportional to *L*).

In practice, experience shows that pure CrM PFC stages require an inductor in the range of 45 mH.W (i.e., 300 µH for a 150-W, wide-ac input application) while less than 30 mH.W (i.e. 200 µH or less for the same 150-W, wide-ac input application) is sufficient if the frequency is clamped. As an example, the NCP1631 wide ac input, 300-W evaluation board runs with PQ26/20, 150-µH inductors.[10]

Reducing Conduction Losses

We have seen that at low line, full load, conduction losses represent the main problem. The best solution consists of limiting the resistance and/or voltage drop of the components seen by the current. Now, to mitigate the heavy-load, low-line efficiency drop shown in Fig. 4, it will mainly be necessary to reduce the resistive losses which rise as a function of the square of the input power. Thus, as an example, it makes sense to try to reduce the series resistance of the EMI choke or use a lower $R_{DS(on)}$ MOSFET.

Above a given power level, such a solution becomes impractical and costly, causing continuous conduction mode to be preferred. As a rule of thumb, this power level is often said to be 300 W but this value may have increased due to use of newer components. However the merit of CCM is to reduce the inductor current ripple which lowers the rms current circulating within the boost converter, as shown in Fig. 10. The lower ripple offers several other advantages such as easier EMI filtering and less stress and lower heating of the bulk PFC output capacitor.

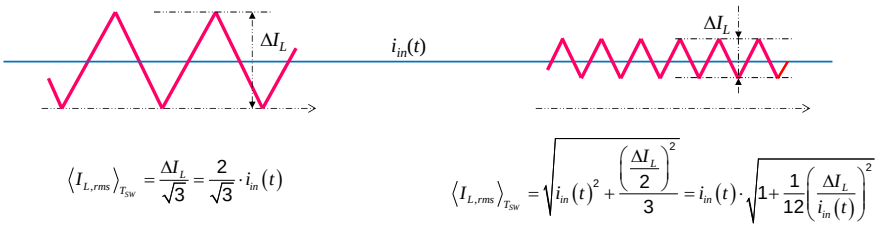


Fig. 10. Reducing the current ripple to lower its rms value.

Now, turn-on losses are minimized in CrM since as aforementioned, the power switch closes at the valley and zero voltage switching can even be obtained if ($v_{in}(t) < V_{out}/2$). This is not the case with CCM, which adds significant turn-on losses, particularly if slow-recovery boost diodes are used.

Low-t_{rr} diodes are hence preferred to minimize the turn-on losses which according to reference [11], can be computed as follows:

Recovery boost diode losses:

$$p_D = \left(\frac{V_F \cdot I_L \cdot t_1}{2} + \frac{V_F \cdot I_{RRM} \cdot t_A}{2} + \frac{V_{OUT} \cdot I_{RRM} \cdot t_B}{6} \right) \cdot f_{SW} \qquad (16)$$

Power switch turn-on losses:

$$p_{Q,on} = V_{OUT} \cdot \left(\frac{I_L \cdot (t_1 + 2 \cdot t_A + t_B)}{2} + \frac{I_{RRM} \cdot (3 \cdot t_A + 2 \cdot t_B)}{6} \right) \cdot f_{SW} \quad (17)$$

where I_{RRM} is the diode reverse-recovery current, t_A is the time between the diode zero crossing of the current and the peak reverse current, t_B is the time between the peak reverse current and diode actual opening and the sum of t_A and t_B is the reverse-recovery time, t_{RR} (where $t_{RR} = t_A + t_B$). These parameters are highlighted in Fig. 11.

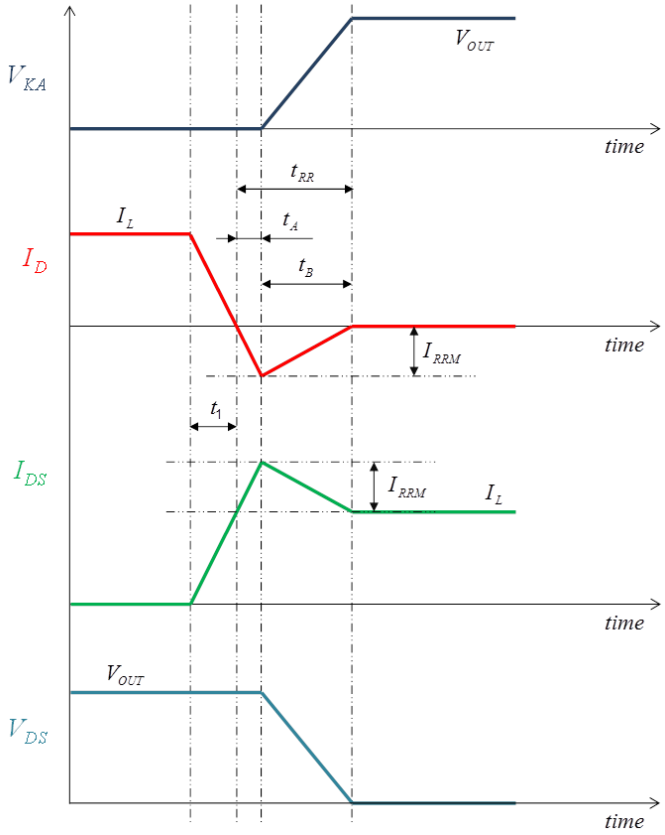


Fig. 11. CCM power switch turn-on sequence.

Finally, critical conduction mode has been considered as the default operating mode because of the good tradeoff it offers between conduction and switching losses. However, if one targets a high efficiency in light-load conditions, the PFC stage must enter discontinuous conduction mode when the line current gets low. Such a dual-mode operation offered by controllers like the NCP1612[9] maintains an optimal balance between the switching and conduction losses.

When the power exceeds 300 or 400 W, it may become uneconomical to continue operating in CrM and despite the significant increase in MOSFET turn-on losses, CCM is generally preferred. A multimode solution which tries to combine the merits of each conduction mode, seems necessary to achieve high-performance and cost-effective operation over a large load/line range:

- DCM in light load
- CCM in heavy load, low line where the input current is high and the inductor current ripple, ΔI_L, would be too large if the PFC was operated in CrM

- CrM otherwise.

Interleaving Channels

A two-channel interleaved PFC converter consists of two paralleled PFC stages operated out-of-phase. Each individual stage can be referred to in a number of ways, either as a phase, a channel, a leg or a branch.

Fig. 12 provides a simplified representation of an interleaved PFC driven by the NCP1632 controller from ON Semiconductor.[12] One merit of this approach is that two small PFC stages are to be designed instead of a larger one, allowing a modular approach. The interleaving solution requires more components but they are smaller and often more standard. These characteristics make the solution ideal for flat panels where the height of the components is critical as in LCD TVs.

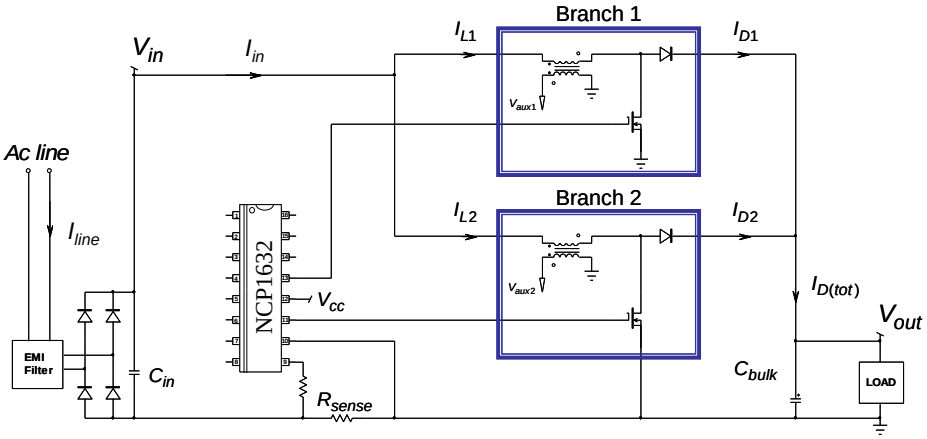


Fig. 12. A two-channel interleaved PFC stage.

Also, if the two channels are properly operated out-of-phase, a large portion of the switching-frequency ripple currents generated by each individual branch cancel when they add within the EMI filter and the bulk capacitors. As a result, EMI filtering is significantly eased and the bulk capacitor rms current is drastically reduced. Interleaving therefore extends the CrM power range by sharing the task between the two phases. This allows a reduced input current ripple and a minimized bulk capacitor rms current.[13]

As an example, Fig. 13 sketches the input current absorbed by each channel (red trace for channel 1 and green trace for channel 2) by a two-channel CrM interleaved PFC. Starting from zero, they ramp up until a peak value is reached and then linearly return to zero. So individually their ripple is large, leading to a high rms value, which limits the power range of the CrM approach.

Now since these two currents are out-of-phase, the total current absorbed from the input rail has a very small ripple and actually resembles the current absorbed by a CCM-operated circuit. Fig. 14 shows that if the line peak voltage is below 50% of the output voltage, the input current looks like the input current of a hysteretic CCM PFC. A similar benefit can be observed on the output side.

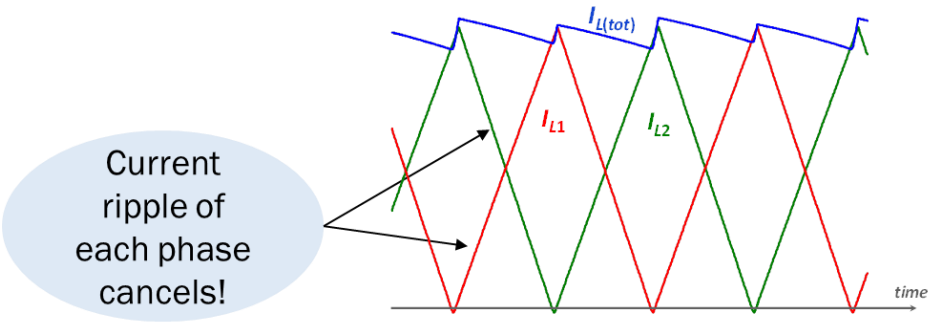


Fig. 13. With interleaving of two CRM-operated channels, a large part of the input ripple cancels.

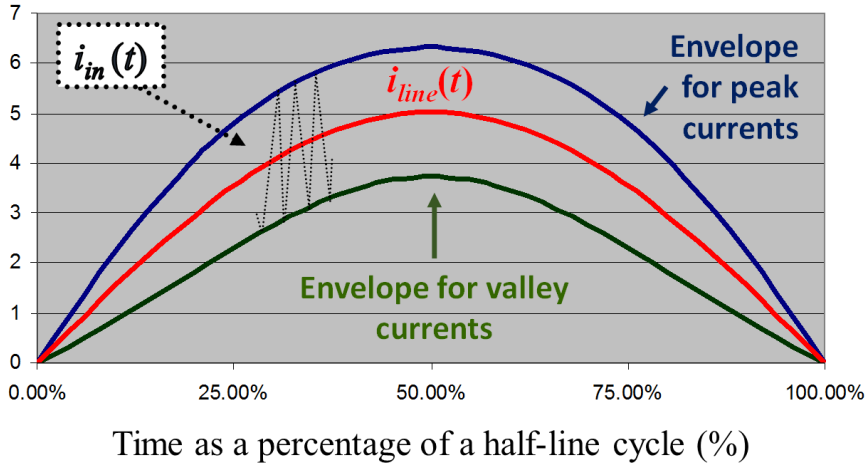


Fig. 14. Low-line ($V_{in,pk}$ < V_{out}/2), peak, valley and input current of a CrM interleaved PFC.

Table 2 illustrates the benefits of interleaving on the output refueling current in a 300-W, wide-ac input application. The output rms currents are reduced, thus minimizing the bulk capacitor heating and improving the application reliability.

Table 2. Comparison of the bulk capacitor rms current in a 300-W application.

	Single-phase CCM PFC	Single-phase CrM / FCCrM* PFC	Interleaved CrM / FCCrM* PFC
Diode(s) rms current ($I_{D,\mathrm{rms}}$)	$I_1 = \sqrt{\frac{8\sqrt{2}\cdot\left(\frac{P_{out}}{\eta}\right)^2}{3\pi\cdot V_{in,rms}\cdot V_{out}}}$	$\frac{2}{\sqrt{3}}\cdot I_1$	$\sqrt{\frac{2}{3}}\cdot I_1$
C_{BULK} rms current ($I_{C,\mathrm{rms}}$)	$\sqrt{(I_1)^2-(I_{out})^2}$	$\sqrt{\frac{4\cdot(I_1)^2}{3}-(I_{out})^2}$	$\sqrt{\frac{2\cdot(I_1)^2}{3}-(I_{out})^2}$
300-W, V_{out} = 390 V $V_{in,rms}$ = 90 V	$I_{D,\mathrm{rms}} = 1.9$ A $I_{C,\mathrm{rms}} = 1.7$ A	$I_{D,\mathrm{rms}} = 2.2$ A $I_{C,\mathrm{rms}} = 2.1$ A	$I_{D,\mathrm{rms(tot)}} = 1.5$ A $I_{C,\mathrm{rms}} = 1.3$ A

Furthermore, if the input current is well balanced, each channel processes half the total power. Thus the size and cost of each individual branch is accordingly minimized and losses are split between the two channels. Hence, hot spots are less likely to be encountered.

As an example, interleaving PFC stages requires two boost diodes but each of them will only have to dissipate half the losses of the single boost diode of a one-channel PFC. In addition, this load sharing may help save cost. Applications exist where two inexpensive axial diodes can do the job while a one-channel PFC may need a more costly TO-220 rectifier.

Conduction losses and current ripple can be further reduced by adding more branches. For instance, the FAN9673 CCM controller[14] is designed to drive a three-channel interleaved PFC with a 120-degree phase shift between branches. That's why this approach, which at first glance, may appear more complex and costly than the traditional one-channel solution, can actually be extremely cost-effective and efficient for power levels above 300 W. For example, interleaved PFC can be a very good choice for applications like LCD and plasma TV applications where the need for smaller components, although more numerous, helps meet the required low-profile form-factors.

By the way, if one admits that a CrM PFC stage is very efficient up to 300 W with wide ac input, an interleaved PFC stage is very efficient up to at least 600 W, wide ac input. Continuous improvement of components tends to increase this power threshold. While the benefits of interleaving merits have been illustrated here with CrM-based solutions, similar benefits are also obtained when CCM channels are interleaved.

The Bridgeless Option

Fig. 15 portrays the diode bridge that is usually inserted between the EMI filter and the PFC stage. This bridge rectifies the line voltage to feed the PFC stage with a rectified sinusoidal input voltage.

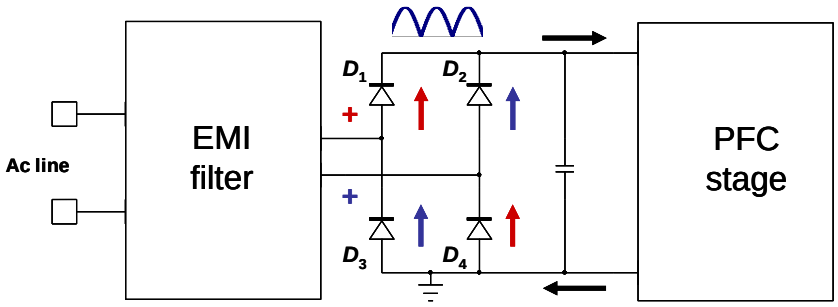


Fig. 15. In a conventional PFC stage, the input current always flows through two diodes.

As a result of this structure, the input current must flow through two diodes before being processed by the PFC boost (D_1 and D_4 during a first half-line cycle—see red arrows of Fig. 15, D_2 and D_3 for the other half-line cycle—blue arrows of Fig. 15). As a matter of fact, two diodes of the bridge are permanently inserted in the current path. Unfortunately, these components exhibit a forward voltage that leads to conduction losses.

The mean value of the current seen by the bridge is the average line current. Based on this, reference [15] gives the following expression of the diode bridge losses:

$$P_{bridge} = 2 \cdot V_f \cdot \left\langle I_{bridge} \right\rangle_{T_{line}} \cong 2 \cdot V_f \cdot \frac{2\sqrt{2} \cdot P_{out}}{\eta \cdot \pi \cdot V_{in,rms}} \qquad (18)$$

where P_{out} is the output power, η is the efficiency and $V_{in,rms}$ is the rms line voltage.

Finally, if we assume an 850-mV forward voltage per diode and assume a 90-V lowest line rms level ($(V_{in,rms})_{LL}$ = 90 V), this power loss becomes:

$$P_{bridge} \cong 2 \cdot 0.85 \cdot \frac{2\sqrt{2} \cdot P_{out}}{\eta \cdot \pi \cdot 90} \cdot \frac{(V_{in,rms})_{LL}}{V_{in,rms}} \quad (19)$$

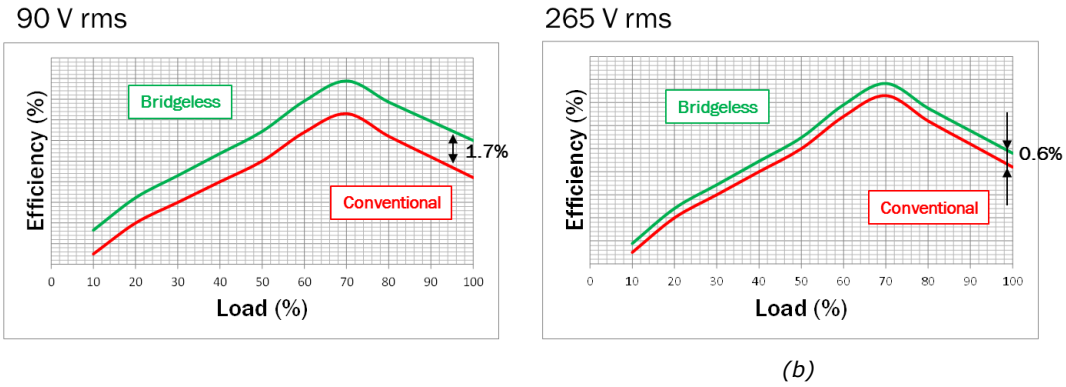
or

$$P_{bridge} \cong 1.7\% \cdot \frac{P_{out}}{\eta} \cdot \frac{(V_{in,rms})_{LL}}{V_{in,rms}} \quad (20)$$

where $(V_{in,rms})_{LL}$ is 90 V, that is, the lowest level of the line rms voltage we have selected.

In other words, equation (20) teaches us that the input bridge dissipation is inversely proportional to the line magnitude and hence, that it reduces at high line. For instance, the input bridge consumes about 1.7% of the input power at 90 Vrms and about 0.6% at 265 Vrms.

Now, as shown by Fig. 16, this percentage remains substantially the same over the load range assuming that the diode V_F voltage is not too heavily affected by the conducted current. The diode bridge conduction losses thus cause a significant efficiency drop over the whole load range and also create a major hot spot affecting the application reliability. Eliminating the diode bridge or at least one diode from the current path is thus highly desirable. So these are the motivations behind the bridgeless approach.



(b)

Fig. 16. Typical bridgeless efficiency gain over the load range at 90-V (a) and 265-V (b) line voltages.

Two-Boost Approach

As detailed in reference [16], several possible solutions are available. We focus here on the two-boost solution for its ease of implementation. Fig. 17 portrays this bridgeless solution first proposed in reference [17].

In this approach, two PFC stages operate in parallel, one fed by one line terminal, the other by the other line terminal. This option eliminates the full-wave rectifier but the line negative terminal remains linked to the application ground by either diode D_1 or D_2 depending on the half-line cycle. Hence, the solution could be viewed as a two-boost PFC where the two branches operate in parallel, as described below.

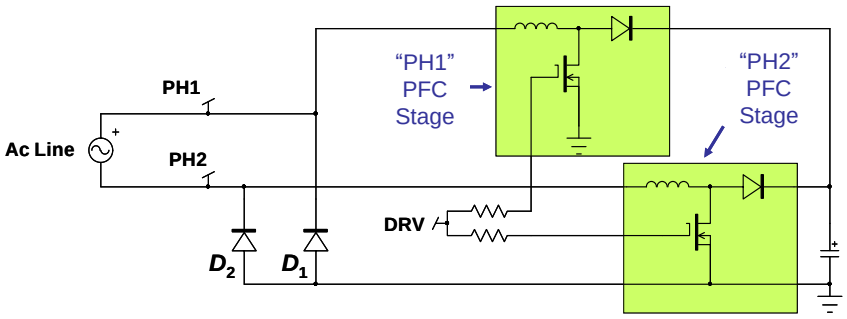


Fig. 17. The two-boost bridgeless PFC architecture.

For the half-wave when the terminal "PH_1" of the line is high, diode D_1 is off and D_2 connects the PFC ground to the negative line terminal ("PH_2"). Thus, D_2 grounds the input of the "PH2 PFC stage" branch which hence, is inactive and the "PH_1 PFC stage" processes the full power.

For the second half-line cycle (when "PH_2" is high), the "PH_2 PFC stage" branch is operating and the "PH_1 PFC stage" that has no input voltage, is inactive.

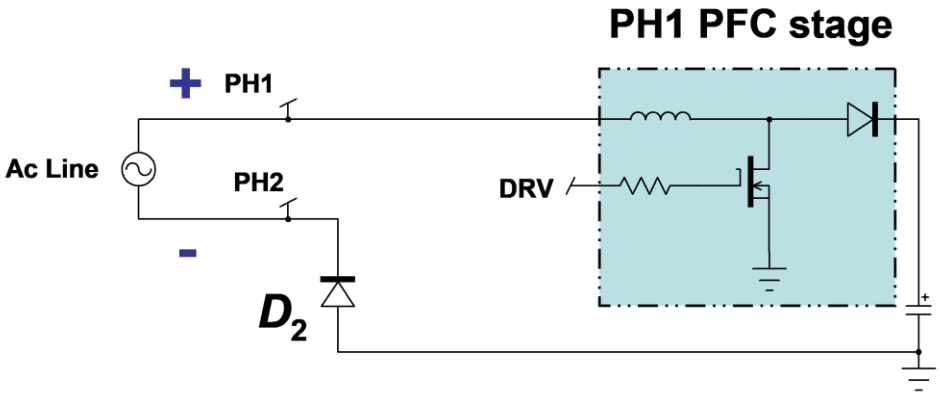
Fig. 18 gives an equivalent schematic for the two half-waves. This bridgeless structure saves one diode in the current path and hence improves the efficiency. One other interesting characteristic of this structure is that the active PFC stage behaves as a conventional PFC boost would do:

When the "PH1" terminal is positive (see Fig. 18a), diode D_1 opens and D_2 offers the return path. The input voltage for the "PH1" PFC stage is a rectified sinusoid referenced to ground.

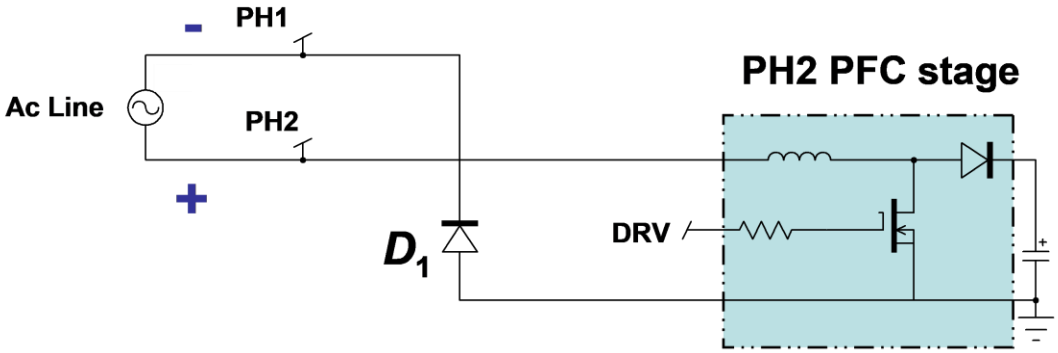
For the other half-wave (see Fig. 18b), when "PH1" is the positive terminal, D_1 offers the return path. Diode D_2 is off and sees a rectified sinusoid that inputs the "PH2" PFC stage. Again, we have a conventional PFC where the input voltage and the boost stage are traditionally referenced to ground.

It is also worth noting that the two-boost structure does not require any specific controller. The MOSFETs of the two branches are referenced to ground and they can be driven even during the idle phase. Put another way, it does not matter whether the MOSFET of the inactive channel is driven or not. So, in the two-boost bridgeless structure the MOSFETs of the two channels can be driven by the same drive pin, whatever the line polarity is.

It is worth noting that the body diode of the inactive MOSFET provides the current with another return path. Because the inductance exhibits a low impedance at the line frequency, we have two diodes in parallel and the current is shared between them. That is why current sensing generally requires special attention like the use of current sense transformers.[15]



(a)



(b)

Fig. 18. Equivalent schematic for the two half-waves. In (a) terminal PH1 is the high one while in (b) terminal PH2 is the high one.

Interleaved Vs. Bridgeless PFC

In Fig. 19, prototypes of two wide-ac input, 300-W PFC stages shown are compared. The two boards are controlled by an FCCrM driver (the NCP1605 for bridgeless, the NCP1631 for interleaved).

The inductors in these PFC stages are to be designed to operate in CrM under the most stressful conditions while DCM limits the switching frequency at light load and near the line zero crossing. Note that since the frequency is clamped, there is no need to oversize the inductor to avoid excessively high frequencies at medium load.

The two boards use the same input bridge, the same MOSFETs (one 250-mΩ or one 99-mΩ $R_{DS(on)}$ MOSFET per branch), the same boost diodes (the axial ultrafast MUR550) and an identical 2.9-°C/W heatsink. The two boards also share similar components for the EMI filter even if the reduced ripple of the input current significantly eases the differential-mode filtering in the interleaved PFC. The NCP1605 and the NCP1631 controllers are both powered by an external 15-V power source.

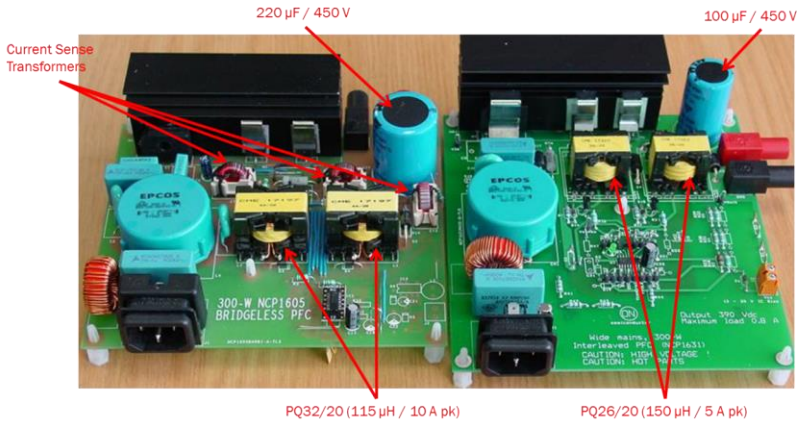


Fig. 19. The two test boards—interleaved PFC (left) and two-boost bridgeless PFC (right).

The two-boost bridgeless solution generates the same rms current in the bulk capacitor as a single-channel CrM PFC while one of the interleaved PFC's merits is to reduce it (1.3 A instead of 2.1 A). In order to have the same stress in both applications, the two-boost bridgeless stage embeds a 220-µF, 450-V capacitor while a 100 µF, 450 V is mounted on the interleaved board.

Another significant difference is in the inductor selection. Each inductor of the two-boost bridgeless drives the total power for one half-line cycle over two while each inductor of the interleaved PFC continuously processes half of the power. The current stress is hence higher in the bridgeless case.

The frequency clamp is set to 130 kHz for each branch of both solutions. To do so, PQ26/20, 150-µH inductors are employed in the interleaved PFC while the two-boost bridgeless application incorporates the bigger PQ32/20, 115-µH chokes.

For the sake of consistency, the standby management featured by the two controllers (soft-skip mode for the NCP1605 and frequency fold-back for the NCP1631) is disabled for a fair comparison of the intrinsic efficiency performance of each concept over the power range.

An exhaustive loss analysis of the two systems is difficult to perform. However reference [18] explains that the two options, when designed to operate in the same frequency range, exhibit similar switching losses. Reference [18] also highlights that each system brings one major benefit regarding the conduction losses. In the case of the two-boost bridgeless PFC, as above discussed, this approach saves the losses of one diode in the current path.

With the interleaved PFC, the input current is equally divided between the two branches of the interleaved PFC while in the bridgeless case, only one branch is active at a time and it sees the total input current. The rms current in each of the interleaved PFC MOSFETs is half the rms current in the active MOSFET of the two-boost bridgeless PFC. As a consequence, the conduction losses in each interleaved PFC MOSFET are one fourth the two-boost bridgeless active MOSFET.

Now, as there are two MOSFETs working in parallel in the interleaved application, the global conduction losses in the interleaved case are halved compared to the two-boost bridgeless one. Here is a clear advantage for the interleaved PFC: if the same MOSFETs are used, conduction losses are two times lower in the interleaved solution:

$$\left(P_{cond}\right)_{Interleaved} = 2 \cdot \left(\frac{4 \cdot r_{DS(on)}}{3} \cdot \frac{\left(\frac{P_{out}}{2 \cdot \eta}\right)^2}{V_{in,rms}^{\ 2}} \cdot \left(1 - \frac{8\sqrt{2} \cdot V_{in,rms}}{3\pi \cdot V_{out}}\right) \right) \quad (21)$$

which leads to

$$(P_{cond})_{Interleaved} = \frac{(P_{cond})_{Bridgeless}}{2} \quad (22)$$

We could easily check that the boost diodes dissipate a similar power in both approaches.

Finally, if we assume the same losses for both applications in the inductors, the bulk capacitor and the EMI filter, we can note that each approach brings an efficiency advantage.

Simply, the two-boost bridgeless approach saves an identical portion of the output power and leads to approximately the same efficiency improvement at full or light load. Close to 0.85% at low line (90 V rms), the savings drop to about 0.3% at high line (270 V rms).

The power savings of the interleaved PFC are proportional to the square of (P_{out} over $V_{in,rms}$). Thus, they are maximum under the most stressful conditions (full load, low line) and rapidly decay as the load decreases or the line magnitude becomes higher.

These most stressful conditions must be considered when dimensioning the components and the board cooling system. We can compute a MOSFET on-time resistance ($R_{DS(on)}$) for which both the bridgeless and interleaved options provide the same savings. In our 300-W application, 410 mΩ is the resistance which is not far from the on-time resistance of our 250-mΩ MOSFET at 110°C (250-mΩ is the $R_{DS(on)}$ at 25°C and this resistance is roughly multiplied by 1.8 at high temperature). This is confirmed by Fig. 20 which shows no bridgeless benefit at full load with the 250-mΩ MOSFET.

In other words, high $R_{DS(on)}$ MOSFETs cancel the bridgeless advantage with respect to the interleaved solution while with low $R_{DS(on)}$ MOSFETs which reduce the contribution of the MOSFET conduction losses, it is possible to obtain the full efficiency benefit obtained by saving half the power consumed by the input diode bridge of a traditional PFC stage.

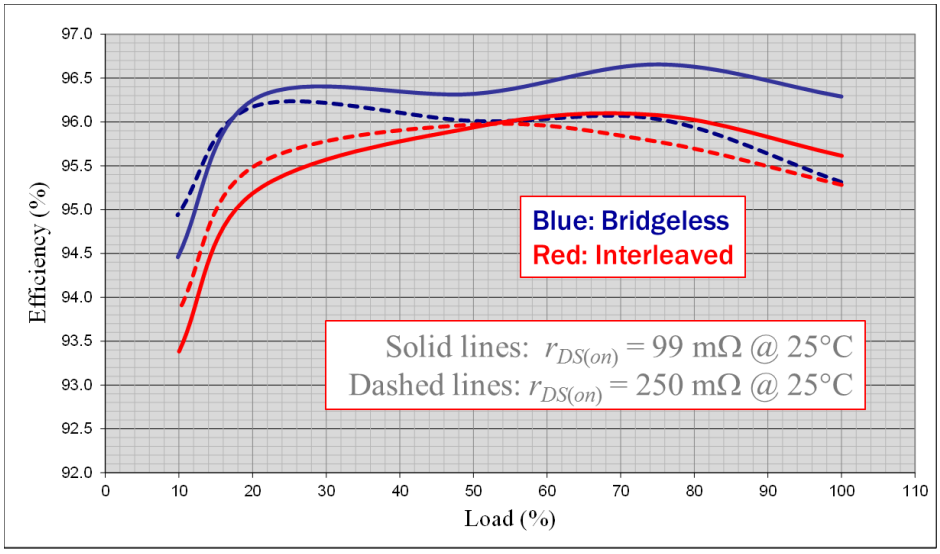


Fig. 20. Efficiency comparison of two-boost bridgeless PFC vs. interleaved PFC at 90-Vrms input.

The portion of the load power saved by the bridgeless PFC is inversely proportional to the line magnitude. At 230 V rms, the gain is therefore limited but not necessarily negligible (about 0.25%). As for the interleaved PFC, savings are proportional to the square of the ratio (power over line voltage magnitude). Hence, its savings are very low at full load to null at light load.

Fig. 21 illustrates the differences between bridgeless and interleaved PFC at high line voltage. On the left, experiments were performed with the most resistive MOSFET (250-mΩ $R_{DS(on)}$), while, on the right, we used the lowest $R_{DS(on)}$ MOSFET (99 mΩ). We see that the bridgeless option is more efficient in both cases and the gap is more significant at light load. The interleaved PFC performance is worse with the lowest $R_{DS(on)}$ MOSFET particularly at light load. This can be explained by the capacitive turn-on losses, which were neglected until now.

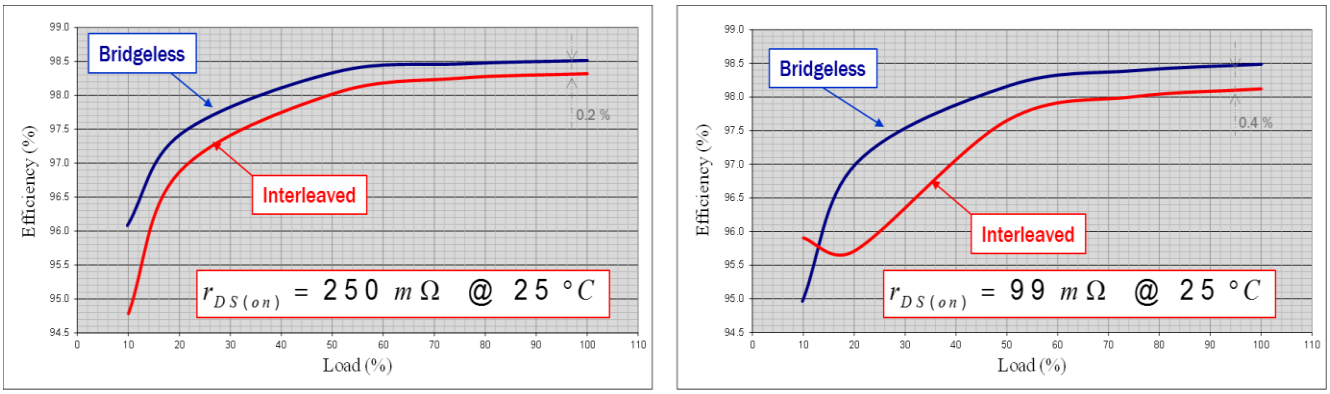


Fig. 21. Efficiency comparison of two-boost bridgeless PFC vs. interleaved PFC at 230 Vrms with 250-mΩ MOSFETs (left) or 99-mΩ MOSFETs (right).

When the MOSFET turns on, it dissipates the energy stored by the lumped capacitance associated with the drain, which includes the MOSFET and boost diode parasitic capacitances, a possible external snubber capacitor, etc. The lowest $R_{DS(on)}$ MOSFET exhibits a higher output capacitance (130 pF vs 63 pF). Note that the interleaved PFC has two branches switching in parallel versus the two-boost bridgeless in which only one channel operates at a time. The influence of the lumped capacitance is then more significant in the interleaved PFC.

As a conclusion, the two-boost bridgeless structure appears to be the most efficient at low line. This is particularly true if low $R_{DS(on)}$ MOSFETs are used. In this case, it brings the full efficiency advantage obtained by saving half the power consumed by the input diodes bridge of a traditional PFC stage. If not, the gain is moderate compared to an interleaved PFC.

Note that that as the line increases, bridgeless benefits reduce. Practically, bridgeless should be preferably envisaged in applications where the line magnitude can be low. As already pointed-out, the bridgeless gain is line-dependent but the efficiency percentage point increase remains substantially the same over the load range. Hence, light-load performance is also improved.

Clearly, the bridgeless approach is more complex and expensive and hence seems to be reserved for applications with efficiency targets impossible to meet with traditional solutions. A bit less efficient, interleaved PFC is a more compact and cost-effective solution.

Conclusion

CrM is a popular and efficient operating mode for low power, offering valley- and even zero-voltage-switching when the instantaneous line voltage is below 50% of the output voltage. However, its major drawback lies in its wide switching frequency variation, which affects efficiency particularly at light load (high switching losses). Frequency clamp and frequency reduction techniques are therefore necessary if high efficiency is targeted at low power.

In addition, frequency clamping helps optimize the inductor size and cost since the inductance does not need to be increased dramatically to limit the switching frequency at medium- and light-load and maintain high-efficiency ratios.

CCM becomes necessary at power levels causing too high an input current ripple which would be uneconomically addressed in CrM, unless an interleaved multi-channel approach was used.

In both CrM and CCM, interleaving offers a modular approach with more but smaller components and easier thermal management. This option increases the CrM power range or improves a CCM solution mainly by dramatically reducing the current ripple.

Bridgeless solutions cost more but they further improve the efficiency particularly at low line. It is worth noting that the efficiency gain remains approximately the same over the whole power range. If you cannot meet your efficiency specification, this looks like the ultimate solution to consider.

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About The Author

Joel Turchi is a member of the Technical Staff at ON Semiconductor in Toulouse, France, where he defines and supports the development of new off-line PWM controllers with a particular focus on power factor correction. With 25 years of power supply industry experience, he often publishes papers and application notes and regularly gives presentations for internal training or customer seminars.

Joel holds more than 20 issued U.S. patents pertinent to control techniques and has originated several innovative control schemes and numerous integrated circuits including the NCP1612 power factor controller with current-controlled frequency foldback and the NCL3018x family of LED-drivers. Prior to joining ON Semiconductor in 1999, Joel was an application engineer at Motorola Semiconductor. He holds an engineering degree in power electronics from the ENSEEIHT School, which is part of the National Polytechnic Institute of Toulouse (France).

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