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The Engineer's Guide To EMI In DC-DC Converters (Part 7): Common-Mode Noise Of A Flyback

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Parts 5 and 6 of this article series[1-6] offered practical guidelines and examples to mitigate conducted and radiated electromagnetic interference (EMI) for nonisolated dc-dc regulator circuits. Of course, no treatment of EMI for dc-dc power supplies would be complete without considering galvanically isolated designs, as the power transformer in these circuits plays a significant role in terms of its contribution to overall EMI performance.

In particular, it's crucial to understand the impact of transformer interwinding capacitance on common-mode (CM) emissions. CM noise is mainly caused by displacement currents within the transformer interwinding parasitic capacitance and the parasitic capacitance between the power switch and chassis/earth ground. This article specifically analyzes CM noise for the dc-dc flyback converter, since it is so widely used as an isolated power supply. At the end of this analysis, a simple, two-capacitor CM noise model of the flyback transformer is developed to model and characterize CM EMI performance.

Flyback Topology

Spanning industrial and automotive market segments, dc-dc flyback circuits[7,8] are a good fit for low-cost isolated bias rails, especially given their easy configuration for single or multiple outputs. Applications requiring isolation include high-voltage MOSFET gate drivers for single- and three-phase motor drives, as well as loop-powered sensors and programmable logic controllers used in factory automation and process control.

A flyback implementation, as shown in the schematic of Fig. 1, offers a robust solution with a simple structure and low component count. If a primary-side regulation (PSR) technique is available, an optocoupler and its associated circuits are not required for feedback regulation,[7] further reducing component count and simplifying transformer design. A transformer with functional-grade isolation provides a straightforward separation of circuit grounds, while reinforced isolation is useful for high-voltage safety-critical applications.

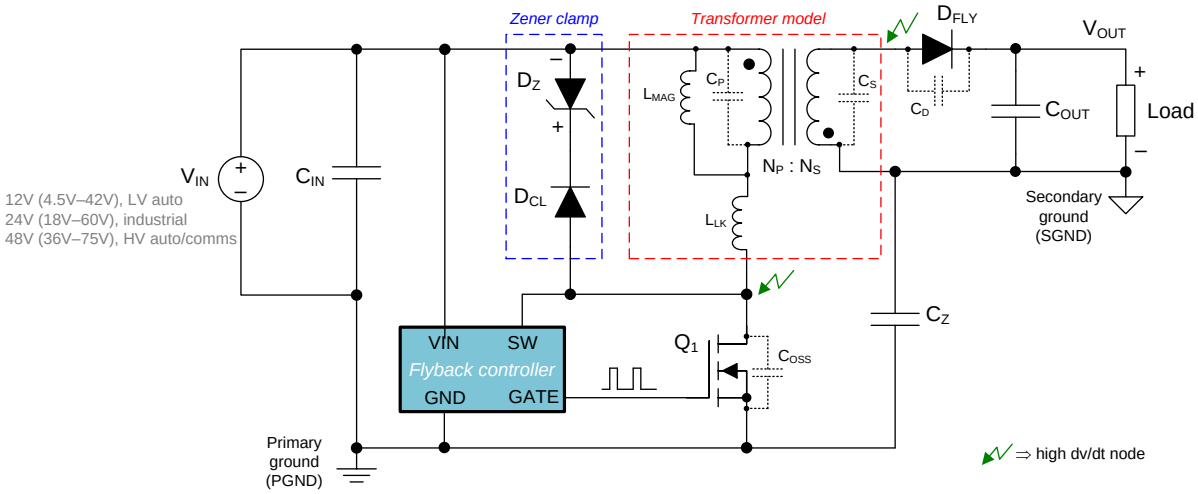


Fig. 1. A dc-dc flyback regulator with a classic 24-V supply or 12-V/48-V input for industrial or automotive battery applications, respectively. The flyback transformer magnetizing and leakage inductances and the circuit parasitic capacitances are denoted explicitly.

Flyback Switching Waveform Behavior

Fig. 2 shows the primary MOSFET and secondary rectifying diode voltage waveforms for a flyback power stage—such as that shown in Fig. 1—operating in discontinuous (DCM) and boundary (BCM) conduction

modes.[7] Fig. 2a highlights the switching waveforms in DCM where the primary MOSFET turns on near the valley of the switch-node resonant voltage swing. Fig. 2b shows the waveforms for BCM switching, with quasi-resonant MOSFET turn-on after an approximate one-half resonant period delay from when the secondary winding current decays to zero. The primary MOSFET turns on at zero current in both DCM and BCM.

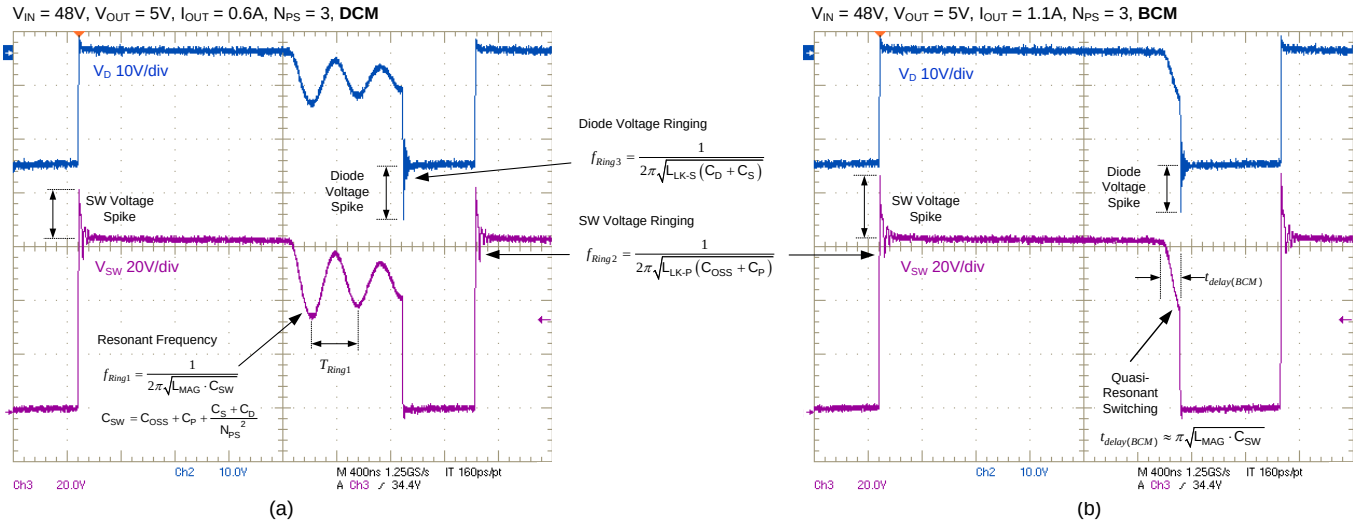


Fig. 2. Primary MOSFET and secondary diode voltage waveforms of a flyback converter operating in DCM (a) and BCM (b). A zener diode circuit across the primary winding clamps the voltage spike caused by the leakage inductance resonating with MOSFET and transformer parasitic capacitances.

Along with the sharp voltage and current edges during switching, particularly troublesome as a source of EMI is the voltage spike overshoot and subsequent ringing behavior. Each commutation excites damped voltage and current oscillations between switch and diode parasitic capacitances and transformer leakage inductance.

Fig. 2 shows the switch-node voltage leading-edge spike and high-frequency ringing at MOSFET turn-off. The ringing behavior depends on the primary-side leakage inductance (L_{LK-P}) resonating with the MOSFET output capacitance (C_{OSS}) plus the transformer primary intrawinding capacitance (C_P).

Similarly, the diode voltage ringing relates to the secondary-side leakage inductance (L_{LK-SEC}) resonating with the diode junction capacitance (C_D) and secondary intrawinding capacitance (C_S). The overshoot and ringing have high transient voltages (dv/dt), so any capacitive couplings to earth ground lead to induced displacement currents and CM noise.

When operating in continuous conduction mode (CCM), reverse recovery of the flyback diode when the primary switch turns on presents additional negative effects. Reverse recovery of D_{FLY} exacerbates the ringing voltage and creates a leading-edge current spike that flows in the primary MOSFET as the recovery current gets reflected to the primary side.

Note that the flyback magnetic component behaves mostly as a coupled inductor, as currents typically do not flow in primary and secondary windings at the same time. The switching transitions are the only intervals where true transformer action exists,[9] with currents flowing simultaneously in the primary and secondary windings (currents ramping in the leakage inductances).

CM EMI In An Isolated DC-DC Flyback

Fig. 3 shows a flyback schematic with a line impedance stabilization network (LISN) connected for EMI measurement. Red dashed lines indicate the dominant CM noise current-propagation paths through the parasitic capacitances to earth ground and back to the LISN. A capacitor designated C_Z connected from primary

ground (PGND) to secondary ground (SGND) shunts CM currents on the secondary side back to the primary, advantageously diverting CM current away from C_{SE} that returns via the LISN.

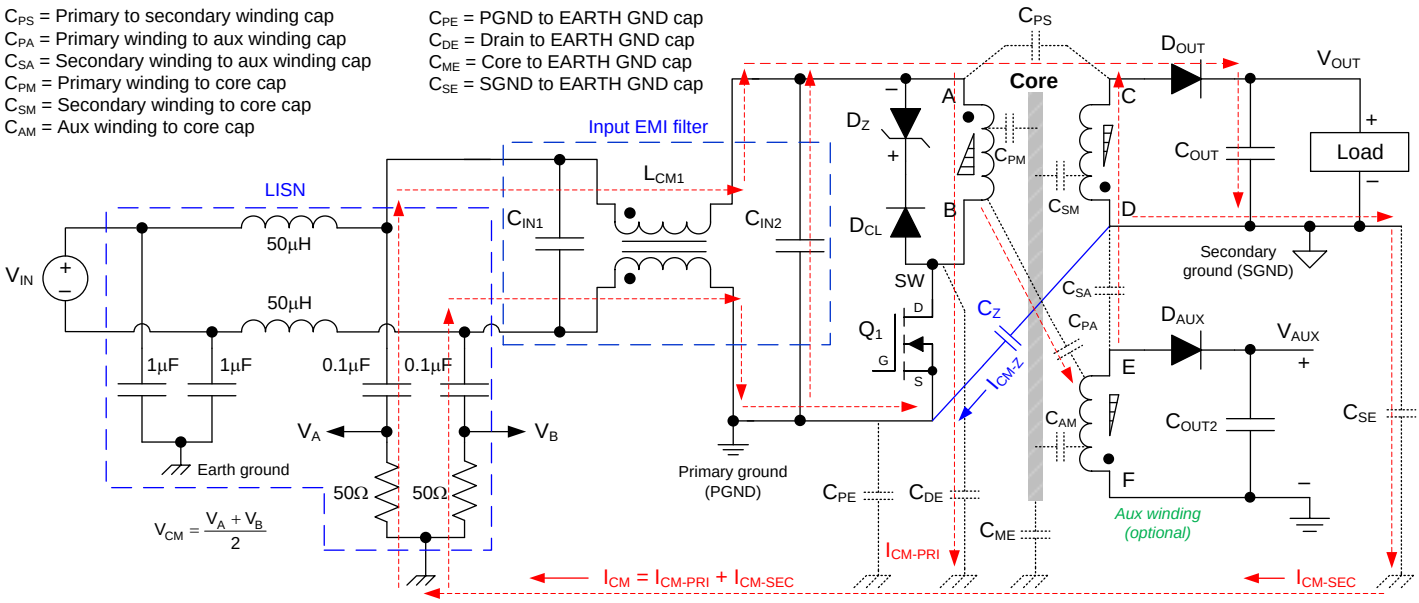


Fig. 3. CM noise current-propagation paths of a two-wire dc-dc flyback regulator with a LISN connected at the input. Also shown is a primary-referenced auxiliary output.

While the high slew-rate voltage of the primary MOSFET drain terminal is the main source of CM noise, the transformer and its parasitic capacitances are the coupling channels through which conducted EMI can propagate from primary to secondary and through the impedance from output circuit to earth ground. The dominant CM current path (denoted by $I_{CM\text{-}SEC}$ in Fig. 3) is from primary to secondary across the transformer and through the impedance from the output circuit to earth ground. Similar to a nonisolated converter, using a small switch-node copper area, connecting the MOSFET heat sink (if needed) to PGND, and avoiding switch-node full vias to the bottom side of the board[6] are three techniques that diminish the coupling from the MOSFET drain to earth ground (denoted by $I_{CM\text{-}PRI}$ in Fig. 3).

Three main considerations related to the transformer apply here. First, tightly coupling the transformer windings minimizes the leakage inductance in order to achieve high efficiency, reduced switch voltage stress and high reliability. Interleaving is a common technique to reduce the leakage inductance and winding ac resistance; consequently, the interwinding capacitance becomes relatively large.

Furthermore, planar transformers with printed circuit board (PCB) embedded windings have even higher interwinding capacitance than conventional wirewound designs due to their closely stacked layers and intrinsically large layer surface areas. In any case, applying a pulsating noise voltage source to such distributed parasitic capacitances generates a relatively high displacement current. It flows from primary to secondary windings and returns to earth ground, resulting in high levels of CM noise.[10]

Second, leakage inductance resonating with parasitic interwinding capacitance may result in severe high-frequency CM noise peaks in the measured EMI spectrum. Third, the stray near-electric field generated by the high dv/dt nodes may easily couple through the transformer magnetic core, as the core material has a high electric permittivity and presents low impedance to electric fields. However, parasitic capacitance (C_{ME}) from magnetic core to earth is small if the core is wrapped in a copper foil connected to PGND.

In general, optimizing flyback transformer design is not only critical in terms of solution size, profile, efficiency and thermal performance, but also has an outsized impact on CM noise performance.

CM Noise Analytical Model

Fig. 4a shows a two-winding transformer with primary and secondary terminals designated (A, B) and (C, D), respectively. Terminal A equivalently connects to PGND based on the input bus capacitor appearing as an effective short at the applicable frequencies for CM noise analysis. Fig. 4b illustrates the conventional electrostatic model of the transformer. From an energy conservation standpoint, the parasitic capacitance of a two-winding transformer can be modeled with six capacitances, including four interwinding capacitances (C_1, C_2, C_3, C_4) and two intrawinding capacitances (C_P, C_S).

Other than affecting the dv/dt of the pulsating switch-voltage waveform, the intrawinding capacitances do not impact the displacement currents from the primary to secondary. The six-capacitor model unnecessarily increases the complexity and makes it difficult to calculate the transformer equivalent capacitances.

However, when substituting the nonlinear switching devices with equivalent noise voltage sources (based on the substitution theory for CM noise analysis[11]), an independent or dependent noise voltage source is in parallel with the transformer windings and the two intrawinding capacitors can be removed. The winding capacitance model then reduces to four lumped capacitors as shown in Fig. 4c, where v_{SW} and v_{SW}/N_{PS} are the switching voltage sources on the primary and secondary windings, respectively. Assuming a low leakage inductance, the winding voltages scale by the transformer turns ratio, N_{PS}, as expected.

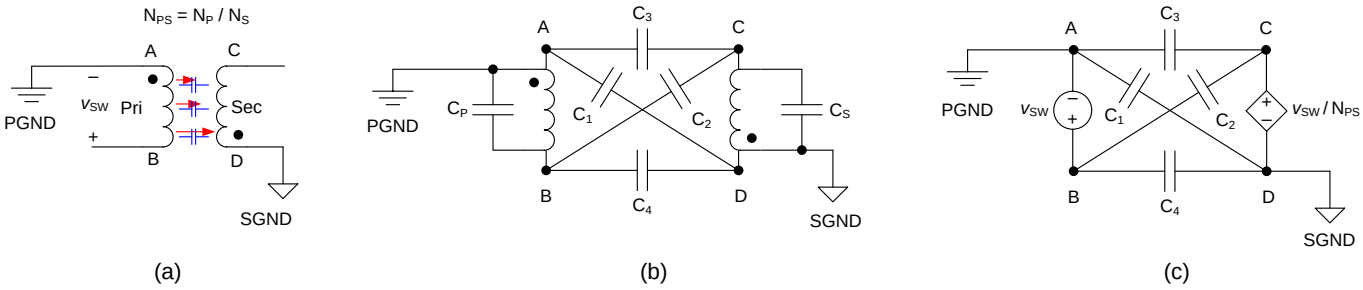


Fig. 4. Two-winding transformer for CM noise analysis (a), six-capacitor CM model (b) and four-capacitor CM model (c).

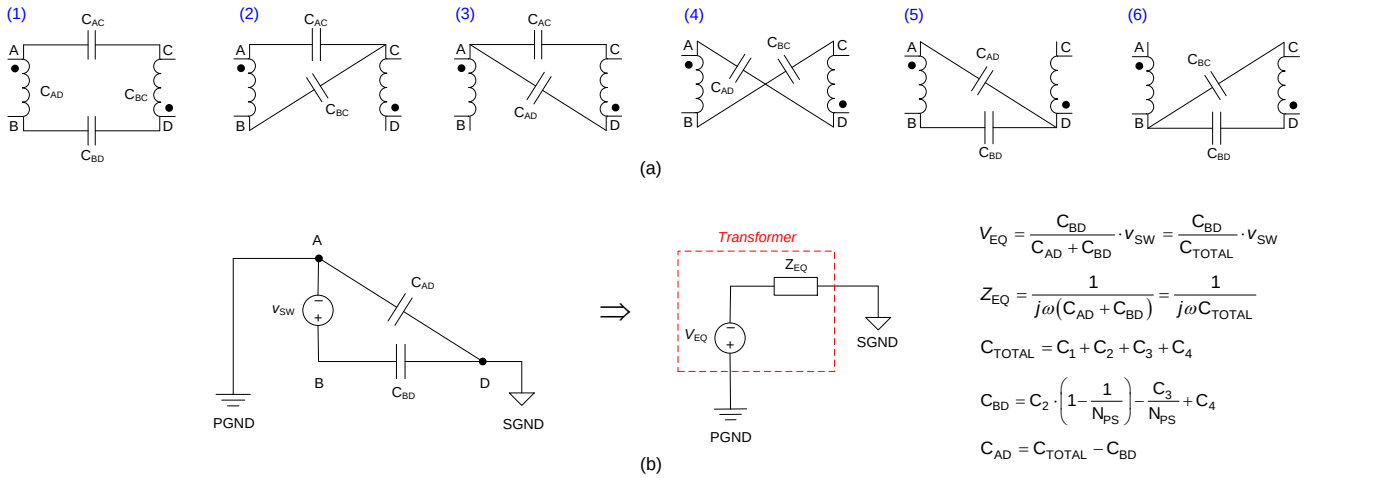
Finally, when one of the transformer windings equivalently connects to an independent voltage source (to substitute for a nonlinear switch), two lumped capacitors are then sufficient to characterize the interwinding parasitic capacitances of a two-winding transformer. The derivation of the two-capacitor model is consistent with displacement current conservation.[11, 12]

As shown in Fig. 5a, there are a total of six possible two-capacitor winding capacitance models. Fig. 5b shows one possible implementation of a two-capacitor CM model (using capacitors C_{AD} and C_{BD}) and its corresponding Thevenin-equivalent circuit.

The two-capacitor CM noise model is flexible, accommodating different isolated regulator topologies, and it facilitates extraction of the transformer lumped capacitance model by experimental measurements.[13] C_{TOTAL} is the structural interwinding capacitance of the transformer measured with an impedance analyzer by shorting the primary and secondary terminals and then treating the transformer as a one-port network. Equation 1 derives C_{BD} by applying a switching frequency sinusoidal excitation signal with 50-Ω source impedance to primary winding terminals (A, B) and measuring the ratio of voltages V_{AD} and V_{AB}:

$$C_{BD} = \left(V_{AD}/V_{AB}\right) \times C_{TOTAL} \qquad (1)$$

Clearly, the advantage of the model is that the parasitic capacitances are easily extracted by simple experimental measurement without knowledge of the transformer structure or the electric potential distributions along the windings.[12]



$$V_{EQ} = \frac{C_{BD}}{C_{AD}+C_{BD}} \cdot v_{SW} = \frac{C_{BD}}{C_{TOTAL}} \cdot v_{SW}$$

$$Z_{EQ} = \frac{1}{j\omega(C_{AD}+C_{BD})} = \frac{1}{j\omega C_{TOTAL}}$$

$$C_{TOTAL} = C_1 + C_2 + C_3 + C_4$$

$$C_{BD} = C_2 \cdot \left(1 - \frac{1}{N_{PS}}\right) - \frac{C_3}{N_{PS}} + C_4$$

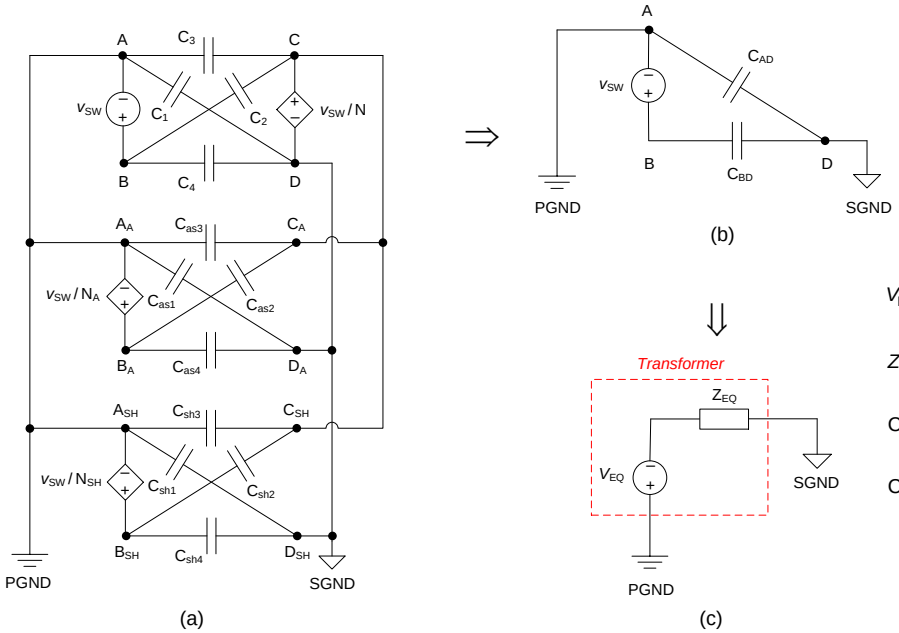
$$C_{AD} = C_{TOTAL} - C_{BD}$$

Fig. 5. Six possible two-capacitor CM models (a) and a two-capacitor CM model with its Thevenin-equivalent circuit (b).

Flyback Regulator CM Noise Model

Fig. 6 shows the CM model for a flyback transformer with primary, secondary, auxiliary and shield windings (similar to Fig. 3 but with an included primary-grounded shield winding). N_A and N_{SH} are the primary-to-auxiliary winding and primary-to-shield winding turns ratios, respectively.

The couplings from primary to auxiliary and primary to shield windings are not considered, as the currents flow solely on the primary side and not back to the LISN, thus not contributing to measured CM noise. As a result, three four-capacitor circuits are sufficient to model primary-to-secondary, auxiliary-to-secondary and shield-to-secondary couplings. Based on the input capacitor acting as low impedance for CM noise, terminal A of the primary winding shorts to PGND.



$$V_{EQ} = \frac{C_{BD}}{C_{AD}+C_{BD}} \cdot v_{SW} = \frac{C_{BD}}{C_{TOTAL}} \cdot v_{SW}$$

$$Z_{EQ} = \frac{1}{j\omega(C_{AD}+C_{BD})} = \frac{1}{j\omega C_{TOTAL}}$$

$$C_{AD} = C_{TOTAL} - C_{BD}$$

$$C_{BD} = C_2 \cdot \left(1 - \frac{1}{N_{PS}}\right) - \frac{C_3}{N_{PS}} + C_4 + C_{as2} \cdot \left(\frac{1}{N_A} - \frac{1}{N_{PS}}\right) - \frac{C_{as3}}{N_{PS}} + \frac{C_{as4}}{N_A} + C_{sh2} \cdot \left(\frac{1}{N_{SH}} - \frac{1}{N_{PS}}\right) - \frac{C_{sh3}}{N_{PS}} + \frac{C_{sh4}}{N_{SH}}$$

Fig. 6. Lumped CM parasitic capacitance model for a multiwinding flyback transformer (a), two-capacitor CM model (b) and Thevenin equivalent circuit (c).

From the previous discussion, only two independent capacitances and a voltage source are required to describe the CM behavior, the expressions for which are included in Fig. 6. As before, C_{TOTAL} is the measured capacitance between the shorted primary-referenced windings and shorted secondary winding.

To develop a CM noise model for the flyback regulator in Fig. 3, the block in Fig. 7 represents the transformer (including primary, secondary, and auxiliary and shield windings) that can be subsequently exchanged for the appropriate two-capacitor CM transformer model. Based on the substitution theorem, all voltages and currents in a circuit will not change when replacing the nonlinear switching devices in the circuit with voltage or current sources that have the exact same time-domain voltage or current waveforms as the original components.

Thus, a voltage source (V_{SW}), which has the same voltage waveform as the drain-to-source voltage of the MOSFET, replaces the MOSFET. Similarly, current sources (I_{DOUT} and I_{DCL}), which have the same current waveforms as the diode currents, replace the two diodes. The voltages and currents in the circuit after substitution are kept unchanged.

Meanwhile, the input and output capacitors have very small impedances to CM noise, so their impedances are neglected. The CM choke series impedance is designated $Z_{CM\text{-}CHOKE}$, and a 25-Ω measuring resistor characterizes the LISN. Finally, the parasitic capacitances that do not significantly contribute to CM noise flowing through the LISN are removed. Fig. 7a represents the CM noise model of the flyback regulator after applying the substitution theorem.[13]

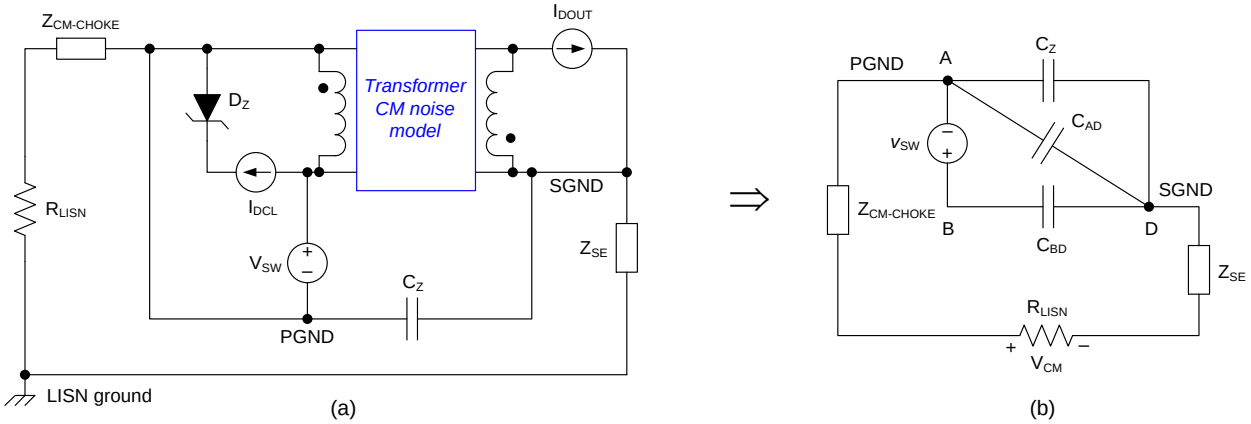


Fig. 7. Flyback circuit model based on the substitution theorem (a) and final CM model of the flyback regulator after applying the superposition theorem (b).

Components in parallel with voltage sources or in series with current sources can be removed, since they do not contribute to the voltages or currents of the network. Superposition theory facilitates analysis of the effects of I_{DCL}, I_{DOUT} and V_{SW} separately. Clearly, I_{DCL} and I_{DOUT} do not generate CM noise, as they are shorted. Fig. 7b shows the final CM model, and Equation 2 provides the CM noise voltage measured at the LISN:

$$V_{LISN} = \frac{R_{LISN}}{j\omega\left(C_{TOTAL}+C_Z\right)+R_{LISN}+Z_{CM\text{-}CHOKE}+Z_{SE}} \cdot \frac{C_{BD}}{C_{TOTAL}+C_Z} \cdot V_{SW} \qquad (2)$$

Circuit simulation incorporating the measured V_{SW} waveform is then conveniently applied to analyze CM noise and the impact of various components. The model is accurate, assuming that the impedance of the leakage inductance is much lower than that of the total parasitic winding capacitance, C_{TOTAL}. Clearly, decreasing C_{BD} as well as increasing $Z_{CM\text{-}CHOKE}$ or C_Z results in lower noise voltage. Note that if the measured V_{AD} based on Equation 1 is zero, C_{BD} is effectively zero, essentially eliminating the CM noise through the transformer. This is a convenient test to check if a transformer is well-balanced.

The general derivation of the CM noise model based on the two-capacitor transformer model follows six steps:

1. Substitute nonlinear semiconductor devices with either equivalent voltage sources or current sources using the substitution theorem. The rule of substitution is to acquire a CM noise circuit that is easy to analyze, while avoiding voltage loops and current nodes. The voltage and current sources shall have equivalent time-domain waveforms as the originals. Treat the input and output capacitors as short circuits because they have very small impedance to CM noise.

2. If paralleling one transformer winding with a voltage source, replace all other windings with controlled voltage sources, because the winding voltages depend on the transformer turn ratios.

3. Simplify the model by removing all components in parallel with voltage sources or in series with current sources.

4. Use one of the two-capacitor models in Fig. 5a that most simplifies the CM noise analysis to replace the original transformer.

5. Analyze the CM noise generated by all voltage sources and current sources based on the superposition theorem.

6. Remove the parasitic capacitances that do not contribute to CM noise flowing through the LISN by analyzing the circuit developed using steps 1 to 5. Inspect the CM noise currents based on the resultant CM noise model.

Summary

From an EMI perspective, a conventional hard-switched isolated converter is considerably more challenging vis-à-vis its nonisolated counterpart. The performance requirements of high-frequency transformers for isolated dc-dc regulators have recently become more stringent, particularly in terms of EMI. The dynamic interwinding capacitance of the transformer represents a critical coupling path for CM noise.

The presented transformer two-capacitor model is broadly applicable and easy to use, as its lumped capacitances are easily quantifiable through a simple measurement method. The next part of this EMI article series applies the model to design and characterize EMI mitigation techniques for isolated converters, including noise balance and cancellation.

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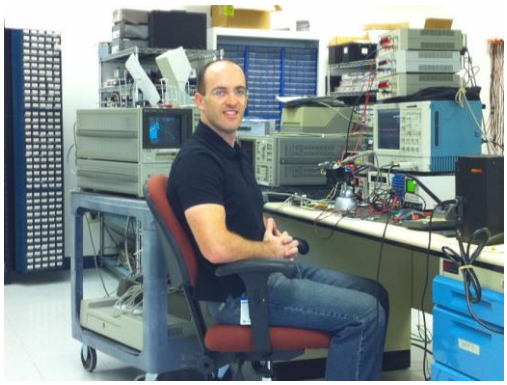
About The Author



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Tim's current focus is on enabling technologies for high-frequency, low-EMI, isolated and nonisolated regulators with wide input voltage range, targeting industrial, communications and automotive applications in particular. He is a senior member of the IEEE and a member of the IEEE Power Electronics, Industrial Applications and EMC Societies.

For more information on EMI, see How2Power's Power Supply EMI Anthology. Also see the How2Power's Design Guide, locate the Design Area category and select "EMI and EMC".