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The Engineer's Guide To EMI In DC-DC Converters (Part 8): Common-Mode Noise Mitigation In Isolated Designs

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The performance requirements of high-frequency transformers for isolated dc-dc regulators have recently become more stringent, particularly in terms of electromagnetic interference (EMI). Part 7 of this article series[1-7] detailed the major sources and propagation paths of common-mode (CM) noise within an isolated flyback regulator.

While the high-voltage (dv/dt) switching nodes are the main sources of CM noise, the distributed interwinding capacitance of the transformer represents a critical coupling path for CM noise. Using a simple and convenient two-capacitor model of the transformer in part 7, an equivalent circuit for CM noise modeled the displacement currents that flow in the transformer capacitances. Only a signal generator and an oscilloscope are needed to extract the parasitic capacitances and characterize the transformer's CM noise performance, obviating the need for in-circuit testing.

Part 8 now reviews CM noise mitigation for isolated dc-dc converter circuits. Converters operating at a high input voltage—such as the phase-shifted full-bridge[8] and LLC series resonant converter[9] in applications such as electric vehicle onboard charging, data center power systems and RF power amplifier supplies—can generate large CM currents. The effect is more pronounced when applying gallium-nitride (GaN) switching devices, as they switch at higher dv/dt than their silicon counterparts.

A wide variety of techniques exist for mitigating CM noise in isolated designs, including symmetrical circuit arrangements, connecting a capacitor between primary and secondary grounds, shielding, adding balance capacitors, optimizing transformer winding design and using an adjustable CM cancellation auxiliary winding. This article reviews these techniques, focusing mostly on flyback circuits.

Symmetrical Circuit Designs

In a symmetrical topology, the switching nodes that have complementary electric potentials with respect to ground are presented in pairs. If the associated parasitic capacitances are the same, the generated CM displacement currents will approximately cancel each other.

Fig. 1a shows the schematic of a two-switch forward converter based on the LM5015, a monolithic two-switch forward dc-dc regulator IC from Texas Instruments.[10,11] Fig. 1b presents a flyback converter configured with split primary and secondary windings. Both converters have symmetrical primary-side circuits with out-of-phase voltage switching waveforms, designated as SW1 and SW2, that create opposite-polarity CM currents and thus lower total CM noise.

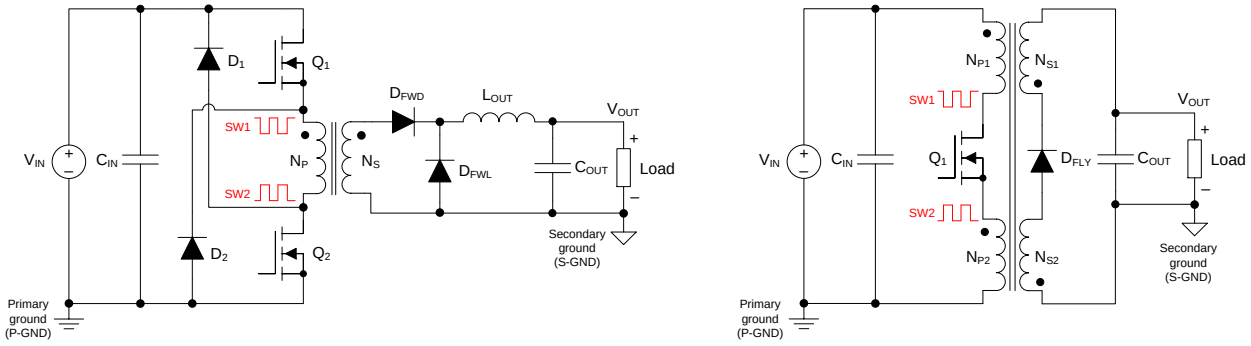


Fig. 1. Balanced-winding topologies with symmetrical primary-side circuits and equal-magnitude, out-of-phase dv/dt switching waveforms for a lower CM noise signature: two-switch forward converter (a); flyback converter with split primary and secondary windings (b).

The two-switch forward converter in Fig. 1a is a well-known topology, but perhaps its favorable CM noise signature is underappreciated. The balanced-winding flyback converter in Fig. 1b also has symmetrical secondary windings. A split winding is usually available if the windings are wound interleaved (to achieve lower leakage inductance). The main drawback of this circuit is that it requires a floating gate driver referenced to SW2.

Similar balanced-winding symmetrical implementations are possible for single-switch forward and LLC resonant converter topologies, as depicted in Fig. 2. The modified symmetrical circuits require additional components, such as a floating gate driver in the forward converter and an additional switch in the LLC resonant circuit, and are only effective for CM attenuation if the transformer's physical winding structure yields symmetrical parasitic capacitances. As a result, other techniques are generally necessary to mitigate CM noise and use conventional isolated topology circuits.

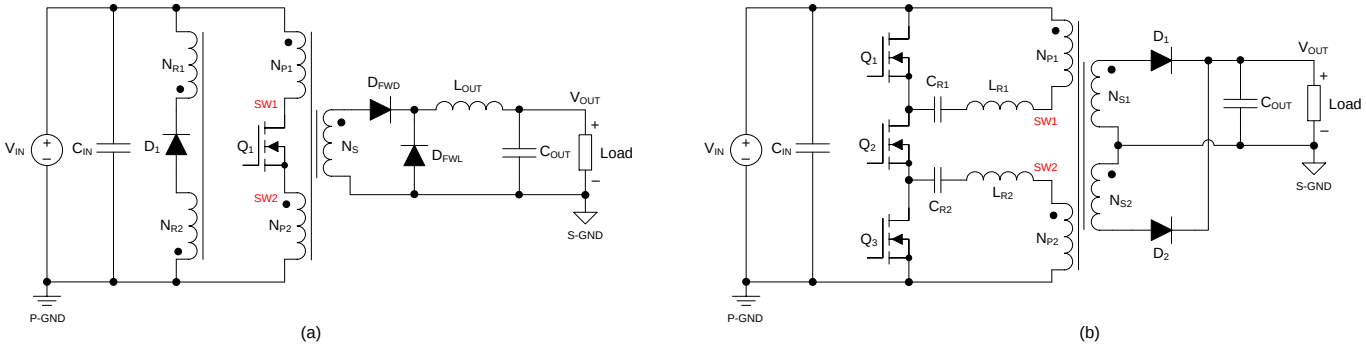


Fig. 2. Symmetrical primary winding design applied to the single-switch forward converter (a) and LLC resonant converter (b).

Connecting A Capacitor Between Primary And Secondary Grounds

Y-capacitors connected from both line and neutral to chassis ground are common in EMI input filters to attenuate CM noise in three-wire ac-dc applications. In a two-wire dc-dc system, however, there is no chassis ground connection point; therefore, it's not possible to connect Y-capacitors. In such systems, connecting a substituting capacitor between primary ground (P-GND) and secondary ground (S-GND) can shunt the CM currents that propagate to the secondary back to their primary-side source.

See the capacitor designated C_Z in Fig. 1 of part 7.[7] This component is a safety-rated capacitor selected with a voltage rating of 1 kV or higher, well above the required isolation voltage specification. However, galvanic isolation is compromised if this capacitor becomes shorted during a fault condition. Also, the capacitor can conduct excessive current if the S-GND connection has a high CM voltage swing relative to the primary, for example in high-side gate-driver bias-supply applications. And if the dc-dc stage follows an ac-dc front-end rectifier, the capacitor can conduct line-frequency leakage currents that may be unacceptable in the application or limited by regulation.[12-15]

CM Balance And Cancellation Techniques

Balance techniques can reduce the CM noise related to transformer winding capacitances based on internal and external transformer balancing. Internal balancing techniques include applying shielding layers,[16-18] optimizing the winding design or using cancellation windings. The most common external balance technique is to add a balance capacitor between selected primary and secondary winding terminals.[12]

Shielding

Shielding techniques aim to block the near-field electric coupling between a transformer's primary and secondary windings by inserting wire or foil shielding layers, thus reducing the displacement current flowing through the interwinding capacitances.

As an example, Fig. 3a shows a flyback converter with a traditional one-turn foil shield winding placed between the primary and secondary layers. Fig. 3b depicts an RM-style core shape with a gapped center leg and vertically oriented windings. The winding half window illustrates two series-connected primary layers (2 x 12T), one secondary layer (1 x 8T) and a single shield layer. The noninterleaved winding arrangement is configured as layers designated P1, P2, SH1 and S1. The figure also depicts the intralayer parasitic winding capacitances.

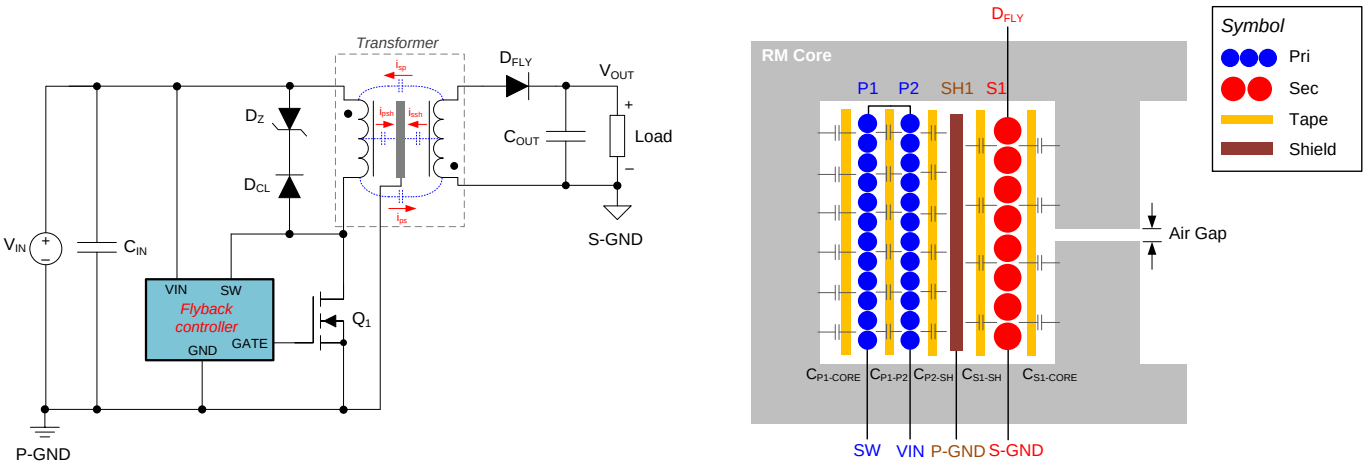


Fig. 3. Flyback converter with a conventional electrostatic foil shield winding placed between primary and secondary layers and connected to P-GND (a) and a winding layer structure of one transformer winding window (b).

A single shielding layer, SH1, is inserted between primary layer P2 and secondary layer S1. The shield normally connects back to a static electric potential in the primary circuit, such as the local P-GND as shown in Fig. 3 or the input capacitor's positive terminal, also a quiet ac node. As a result, the electric coupling between P2 and S1 is blocked, and the displacement current between P2 and S1 is eliminated.

With the shield in place, i_{psh} will flow into the shield and back to P-GND instead of flowing to the output and from there back to chassis ground. However, capacitance still exists between the shield and the adjacent secondary winding. Since the voltage induced in the one-turn shield is not the same as in the secondary winding (the exception being a one-turn secondary), some CM current inevitably flows between the shield and the secondary winding. Driving the shield instead by a tap on an auxiliary winding, such that the average voltage on the shield matches the average voltage on the secondary, can achieve CM balance.[18]

Note that there is coupling between the P1 and S1 layers in Fig. 3 through the high-permittivity core material. Therefore, while a single shield layer helps attenuate CM noise, it may not eliminate it entirely. Also, a disadvantage is that more shield layers are required as the number of primary-secondary boundaries increases. Importantly, a shield layer increases the space between windings and therefore leads to increased leakage inductance.

In general, a copper foil shield should be as thin as possible in order to reduce eddy current losses due to the proximity effect. The losses in the shield can become excessive at high switching frequencies, and the shield also increases the total parasitic capacitance reflected to the switch node.

Balancing Capacitor Value And Position

Fig. 4a shows the schematic of a flyback converter with primary, secondary and auxiliary transformer windings. N_{PS} and N_{AUX} are the primary-to-secondary and the primary-to-auxiliary winding turns ratios, respectively. The couplings from primary to auxiliary are not considered, as the currents flow solely on the primary side, thus not contributing to measured CM noise. Based on the discussion in part 7, two four-capacitor circuits are sufficient to model the primary-to-secondary and auxiliary-to-secondary couplings, as shown in Fig. 4b.

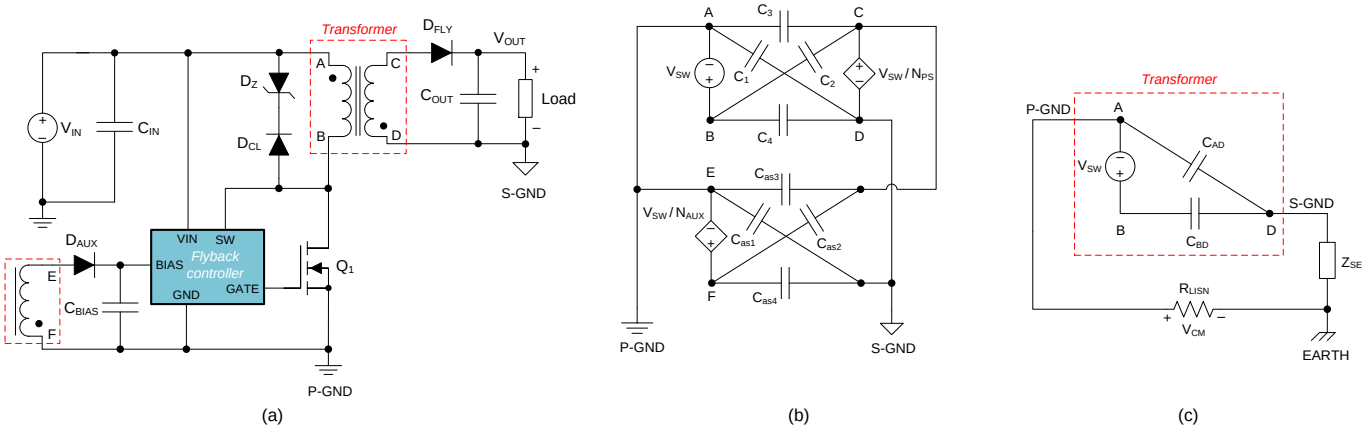


Fig. 4. Flyback converter with auxiliary winding (a), lumped CM parasitic capacitance model for a three-winding flyback transformer (b) and CM noise-equivalent circuit using a two-capacitor transformer model (c).

If the input capacitor acts as low impedance for CM noise, terminal A of the primary winding shorts to P-GND. Then, using the simplified two-capacitor model of the transformer, with Z_{SE} modeling the capacitive coupling from S-GND to earth, Fig. 4c gives the final equivalent circuit model for CM noise (see part 7 for additional context and description).

Equation 1 provides the CM noise voltage measured at the line impedance stabilization network (LISN). Clearly, a decrease of the capacitance C_{BD} results in a lower noise voltage.

$$V_{LISN} = \frac{R_{LISN}}{j\omega\, C_{TOTAL} + R_{LISN} + Z_{SE}} \cdot \frac{C_{BD}}{C_{TOTAL}} \cdot V_{SW} \qquad (1)$$

Equation 2 gives the theoretical expression for C_{BD}, and is measured using the technique described in part 7 based on Equation 3:

$$C_{BD} = C_2 \cdot \left(1 - \frac{1}{N_{PS}}\right) - \frac{C_3}{N_{PS}} + C_4 + C_{as2} \cdot \left(\frac{1}{N_{AUX}} - \frac{1}{N_{PS}}\right) - \frac{C_{as3}}{N_{PS}} + \frac{C_{as4}}{N_{AUX}} \qquad (2)$$

$$C_{BD} = \left(V_{AD}/V_{AB}\right) \cdot C_{TOTAL} \qquad (3)$$

It is possible to balance C_{BD} to zero[13] by increasing the negative terms in equation 2. The easiest way is to parallel a capacitor with C3 across transformer terminals A and C between the primary and secondary sides. The value of this external balance capacitor is $C_{EXT} = N_{PS} * C_{BD}$.

Similarly, if C_{BD} is negative (when the V_{AD} and V_{AB} measured voltages are out of phase), connecting a balance capacitor equal to the absolute value of C_{BD} in parallel with C4 across terminals B and D can achieve balance. Note that if the measured V_{AD} from Equation 3 is zero, C_{BD} is effectively zero, essentially eliminating CM noise through the transformer. This is a very convenient test to determine whether a transformer is well balanced.

Winding Design

As an alternative to balancing capacitors, it is possible to arrange the transformer winding layer positions to improve CM balance. According to the concept of paired layers,[12-15] there are layers on the primary and

secondary sides that have similar dv/dt; therefore, their overlapping does not generate CM noise. The average voltages at both ends of the interwinding capacitances are arranged to have similar amplitude and polarity, thus minimizing or nulling the CM current through the capacitances.

The basic principle is to ensure that the adjacent primary and secondary winding layers have similar voltage distributions. Assuming that the interwinding parasitic capacitances are evenly distributed between the two paired winding layers, zero dv/dt can be maintained over these capacitances such that no CM current is generated.

As an example, consider the flyback converter of Fig. 4a and an interleaved three-winding (primary, secondary, auxiliary) transformer. Even though it increases the interwinding capacitance, interleaving is often mandatory to reduce leakage inductance and proximity effect losses. Fig. 5a illustrates the winding half-window of a flyback transformer with three series-connected primary layers (3 x 12T), two paralleled secondary layers (2 x 9T) and one auxiliary/bias winding layer (1 x 15T).

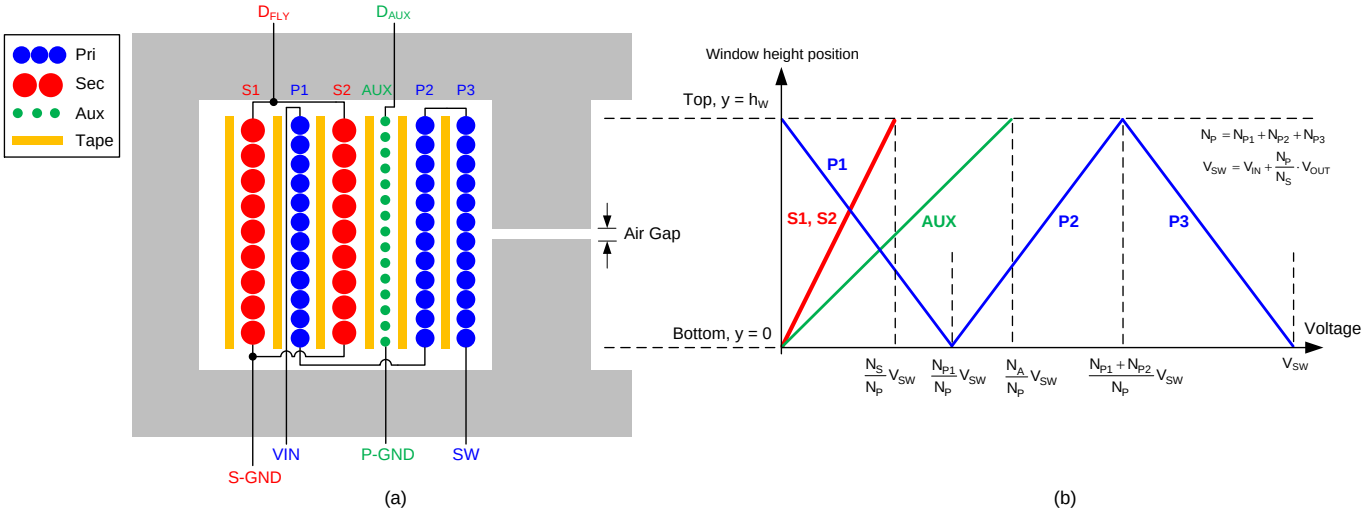


Fig. 5. Flyback transformer with a sandwiched winding layer structure (a) and voltage distributions of layers across the winding window (b).

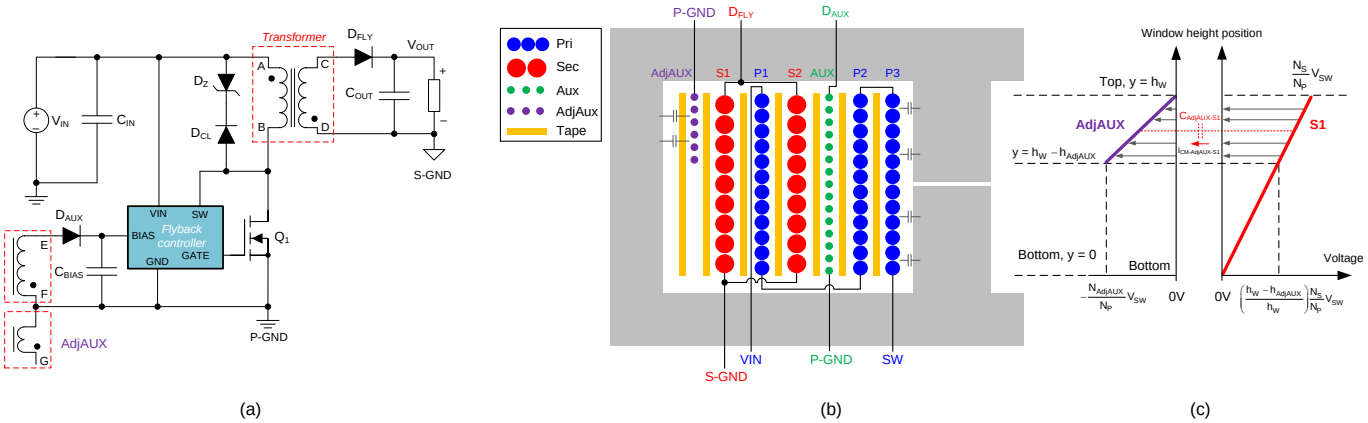
If the voltage is linearly distributed along the winding, Fig. 5b illustrates the voltage distribution of the windings. To achieve the lowest CM noise, the adjacent layers between the primary and secondary winding layers should have the lowest average voltage difference. As a result, the interleaved layers of Fig. 5a are purposely arranged as S1-P1-S2-AUX-P2-P3.

The average voltage difference between P1 and S1 or S2 is lowest with the terminal connections shown in Fig. 5a. P1 starts at VIN (a quiet node) and is positioned adjacent to the two paralleled secondary layers S1 and S2, as depicted in Fig. 5a. Similarly, the AUX winding is adjacent to layer S2, because the voltage difference between AUX and S2 is less than that between S2 and P2 or P3.

The voltage difference between AUX and P2 does not generate CM noise, as both windings reside on the primary side. The displacement currents between them are thus confined within the primary side of the converter and not measured as EMI by the LISN. Conversely, when using a full interleaving winding structure of P1-S1-P2-S2-AUX-P3, the CM noise will significantly increase because of the larger average voltage differences between layer pairs S1 and P2, and P2 and S2.

Adjustable Auxiliary Cancellation Winding

An auxiliary winding layer may be used for adjustable cancellation of CM noise. This type of winding, which is labeled AdjAUX in Fig. 6, is wound outside secondary layer S1 to balance the CM noise that is not fully canceled within the winding layers.[13,14] One terminal of AdjAUX connects to P-GND and the other terminal is floating.



(a) (b) (c)

Fig. 6. Adding an adjustable auxiliary winding on the outer layer to cancel CM noise: schematic (a), winding arrangement (b) and voltage and current distributions (c).

As the voltage difference between AdjAUX and S1 is negative, there is a displacement CM current flowing from S1 to the AdjAUX winding and then back to the primary side. This helps cancel the displacement CM current flowing from P1 to S1 and S2 as well as from AUX to S2, due to the positive voltage difference between P1 and S1, between P1 and S2, and between the AUX and S2 layers (P1 and AUX have a higher number of turns on each layer than S1 and S2 in this example). As depicted in Fig. 6b, the position of the AdjAUX winding is located at the outer layer of transformer windings, so it is convenient to adjust the number of turns to achieve effective noise cancellation.

As shown in Fig. 6c, when the AdjAUX winding starts from the top of the winding window, the voltage difference between AdjAUX and S1 layers is largest. Fewer turns achieve the required cancellation effect, whereas more turns are needed if the AdjAUX winding is located at the bottom of the window.

There is no eddy current power loss, since the AdjAUX winding is not near the air gap and incurs zero H-field. As a result, the transformer ac winding loss is lower than that with conventional shielding layers. And because there are no shielding layers between winding layers, the mutual coupling between windings is higher, resulting in lower leakage inductance.[18] Finally, when combined with the transformer balance examination technique discussed in part 7, the AdjAUX winding layer can be conveniently designed without any in-circuit tests.

Summary

CM noise is one of the major concerns in the design of high-frequency isolated dc-dc converters. As the switching frequency increases to improve power density, a high dv/dt at the primary switching node and associated CM interference through the transformer interwinding capacitance become detrimental to the system. CM noise reduction techniques include using symmetrical topology designs, shielding and balance capacitors.

Also, the winding design method reduces noise by properly arranging the transformer layers and choosing optimal connections between the winding layer terminals and the circuit nodes. Finally, an auxiliary cancellation winding wound on the outside of the transformer achieves CM noise balance. These methods can be adopted individually for some topologies or combined to achieve better noise reduction for meeting specification requirements and solving complex CM noise issues.

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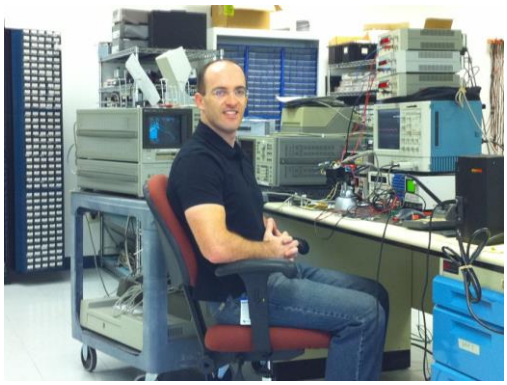
About The Author



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