






New Packages Offer Smaller Size, Greater Reliability For Rectifiers—With Some Tradeoffs







by Jos van Loo, Taiwan Semiconductor Europe, Zorneding, Germany and Kevin Parmenter, Taiwan Semiconductor America, Chandler, Ariz.

Since the introduction of the SMA, SMB and SMC rectifiers in 1990 and 1991 (earlier for TVS), customers have complained about their height. Lower-profile packages are desirable. The SMA/B/C packages were initially transient voltage suppressor (TVS) packages and nobody ever claimed that their thermal design was very good. The rectifier industry just started using them because they were available at the time and customers wanted to replace MELFs (metal electrode leadless face packages) because of the problems linked to soldering MELF diodes.

The SMA/B/C packages reflected the technology available 30 years ago. However, there is room for improvement and recently a number of new packages have been introduced by Taiwan Semiconductor (TSC) and other vendors to address the shortcomings of the SMA/B/C packages (see Table 1). In addition, process improvements were made. As a result, rectifiers can now be produced with zero defects.

Table 1. Taiwan Semiconductor SMD packages.

Package					
	Micro SMA	SOD-123FL	SOD-123W	Sub SMA	SOD-123HE
Outline dimension (L*W*H mm)	2.70*1.35*0.73	3.90*1.70*1.15	3.80*1.90*1.02	3.80*1.90*1.43	3.90*1.95*0.85
Footprint size (mm ²)	3.65	6.63	7.22	7.22	7.61

Package						
	SOD-128	Thin SMA	DO-214AC (SMA)	DO-214AA (SMB)	TO-277A (SMPC)	DO-214AB (SMC)
Outline dimension (L*W*H mm)	5.00*2.70*1.10	5.35*2.70*1.00	5.33*2.83*2.50	5.60*3.95*2.65	6.65*4.65*1.20	8.13*6.22*2.62
Footprint size (mm ²)	13.50	14.45	15.08	22.12	30.92	50.57

In other power management markets, like MOSFETs, power management ICs and other power discrete components, improvements have been made to reduce the die size-to-package ratio.

Older packages, such as the SMA, have a poor die size-to-PCB footprint ratio. The maximum possible die size in the SMA package is 70 mil or 1.75 mm (square die). However most products sold in an SMA package have a 50-mil or 1.25-mm square die. In this case the die/package size ratio is just over 10%. A picture of the package visualizes the wasted space in the package and the longer distance the heat has to travel to reach the solder joint and PCB (Fig. 1).

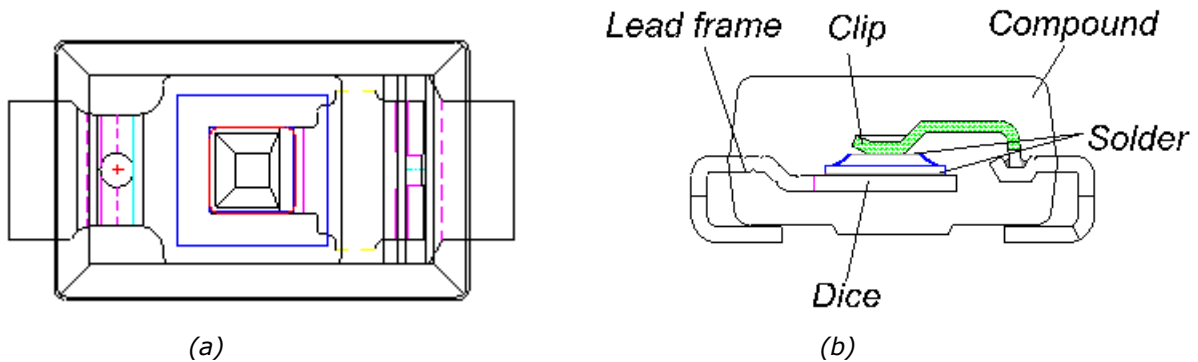


Fig. 1. SMD series internal structure for SMA. Top view (a) and side view (b) are shown here.

Newer packages with flat leads and exposed solder pads transport the heat more efficiently and waste less space on a PCB. The same 50-mil die from an SMA can also be manufactured in an SOD123W package (Fig. 2).

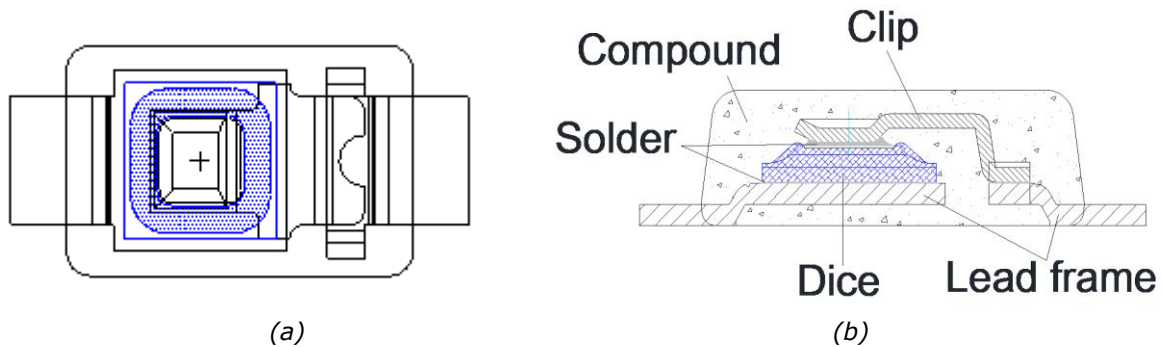












Fig. 2. SMD series internal structure for SOD-123W. Top view (a) and side view (b) are shown here.

With the SOD123W, the package no longer wastes space and the die-to-package footprint ratio is now >20%. The heat is directly transferred out of the package. An added benefit is the height reduction of 2.5 mm for the SMA to 1.02 mm for the SOD123W.

So existing die and new die, currently used in SMA, SMB and SMC packages, can now be placed in smaller packages. A lot of combinations are possible, depending on the product and the application but in general the SMC package can be replaced by the TO277A and SMPC package, the SMB package can be replaced by the SOD128 package and the Thin SMA, and the SMA package by the SOD123W and the SOD123HE (Table 2).

Sometimes downsizing to these newer packages will be easy and straightforward, but not always. This article will discuss how smaller packages will influence designs and applications. The four key areas in rectifier/TVS product development are transient thermal impedance, package height, thermal resistance and process improvements leading to zero defects. This article discusses the impact that moving to the smaller packages will have on each of these areas, identifying the relevant design tradeoffs that device users must be aware of. But first, we'll review the key electrical specifications that govern rectifier selection and the factors that determine their maximum ratings.

Table 2. Smaller solutions by Taiwan Semiconductor for selected surface-mount packages.

SOD-123HE 3,90x1,95x0,85 mm	SMA 5,33x2,83x2,50 mm		SMB 5,60x3,95x2,65 mm	SMC 8,13x6,22x2,62 mm	D-PAK 10,40x6,73x2,38 mm
					
↓	↓	↓	↓	↓	↓
SPACE SAVINGS					
48 %	45 %	45 %	45 %	64 %	45 %
					
MICRO SMA 2,70x1,35x0,73 mm	SOD-123W 3,80x1,90x1,02 mm	SOD-123HE 3,90x1,95x0,85 mm	SOD-128 5,0x2,70x1,10 mm THIN SMA 5,35x2,70x1,0mm	TO-277A (SMPC) 6,65x4,65x1,20 mm	

Absolute Maximum Ratings Of Rectifiers

$T_J = T_A + P_D * R_{\theta J-A}$ is the most important equation when designing with rectifiers. The absolute maximum ratings of a rectifier are the T_J junction temperature, the I_{FSM} surge current and the maximum breakdown voltage. The current rating and power dissipation (as well as current derating curves) are determined by marketing and designers who choose the size of the solder pads and PCB materials (thermal resistance).

The junction temperature is linked to the power dissipation (P_D) and the thermal resistance $R_{\theta J-A}$. So both package design and die technology contribute. The I_{FSM} surge current is mainly linked to the die size and the transient thermal impedance. The breakdown voltage is determined by the die. In a TVS, the maximum peak power dissipation is linked to the die and the transient thermal impedance.

Transient Thermal Impedance

The transient thermal impedance of a rectifier or a TVS diode is rarely discussed. Lightning strikes, 8/20- μ s pulses or capacitive inrush surge currents (in ac-dc conversion designs) are single pulse events, not repetitive. The product either survives or fails.

The capability of a product to handle these surges is mainly dependent on the die size and the quality of the solder joint. For surges of 1 ms or less, it is possible to reduce the package size without any degradation of the electrical performance if you keep the die size the same.

TVS Packages And Roadmap

TVS diodes don't really follow the $T_J = T_A + P_D * R_{\theta J-A}$ formula if we assume that the application is a single pulse event. They have a peak power rating of, for example, 400 W linked to a certain pulse—in most cases a 10-/1000- μ s exponential waveform.

The T_J max may be briefly exceeded during this test—the product has to survive the test without damage. The product capability is determined by the die size. The new packages introduced have a better die size-to-footprint ratio so product miniaturization is straightforward if you keep the die size the same. Fig. 3 demonstrates this.

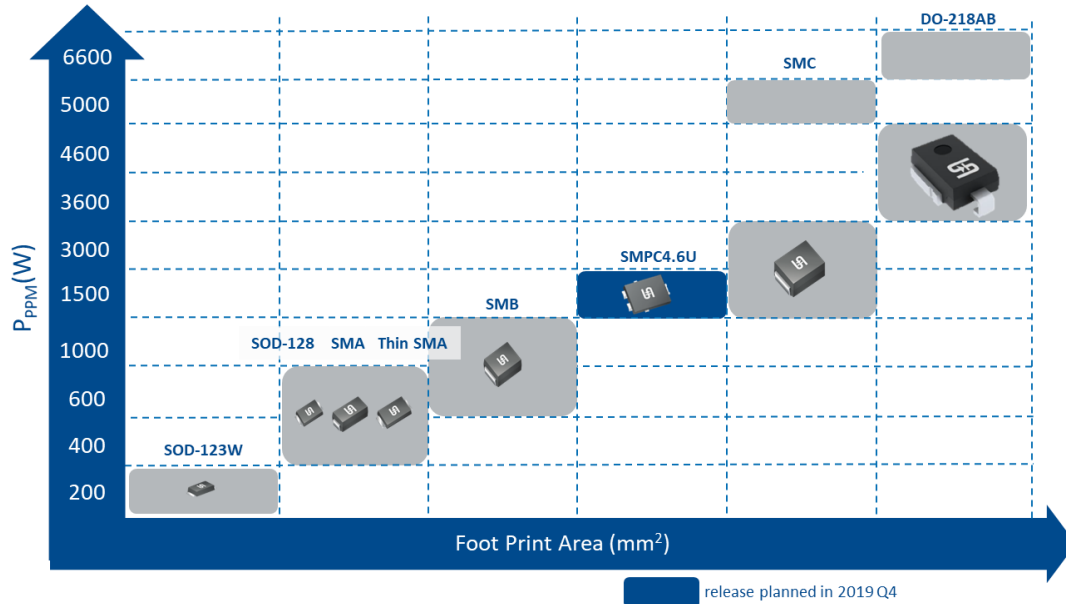


Fig. 3. Taiwan Semiconductor TVS Portfolio—SMD packages. The newer packages have a better (higher) die size-to-package ratio.

Exceptions are TVS products used as clamps in a snubber circuit (MOSFET protection), load dump protection and Zener diodes used for higher power dissipation. In these applications thermal resistance, package design and PCB design are important and miniaturization is difficult.

The automotive industry uses very well defined standards to protect against voltage spikes. The ISO7637 norm defines a number of pulses (1, 2a, 2b, 3a and 3b) that simulate the most common voltage transients that can occur in 12-V and 24-V cars. These transients are mainly low power, and short, and smaller packages can also protect against these pulses as demonstrated in Table 3. Consequently, the switch in the automotive industry to smaller TVS packages has started.

Table 3. TVS Diodes—compliance of different package styles with ISO-7637 and ISO-16750 norms.

	SOD123W	Thin SMA	SOD-128	SMA	SMB	SMC	DO-218
ISO-7637 ISO-16750							
1	●	●	●	●	●	●	●
2a	●	●	●	●	●	●	●
2b	●	●	●	●	●	●	●
3a	●	●	●	●	●	●	●
3b	●	●	●	●	●	●	●
A							●
B						●	●

The limitations on miniaturization of semiconductor packages can be easily seen in the ISO16750-2 Load Dump protection norm (A is primary protection, B is secondary protection). The A version requires the DO218

package, a very large package with a lot of copper and a big die. These load dump pulses are up to 400-ms long and have a lot of energy. The transient thermal impedance of the package has to help the die to handle the energy. Therefore no miniaturization is possible.

Standard Rectifiers

The 1N4007 series and S1 series of rectifiers are among of the most commonly used products in low power ac-dc conversion. Billions of these rectifiers are manufactured every year by multiple vendors. If we take as an example a flyback converter with <20-W output, the power dissipation in these rectifiers when used as an input bridge rectifier is quite small. Currents are less than 100 mA. Their limiting factor is the IFSM surge rating, which determines whether a rectifier can withstand the inrush current during start up when an empty capacitor needs to be charged.

Table 4 compares a number of products, all with a 30-A (8.3-ms) surge rating. It becomes clear immediately that the S1 in an SMA package is not needed because smaller packages with the same die are available that can also perform the input rectification function.

Table 4. Comparing electrical characteristics of standard rectifiers with a 30-A (8.3-ms) surge rating in different packages.

Part number	Package	V_{RRM} (V)	$I_{F(AV)}$ (A)	V_F (V)	I_{FSM} (A)
LL4007G	MELF (Plastic)	1000	1	1.1	30
S1M	DO-214AC (SMA)	1000	1	1.1	30
S1MB	DO-214AA (SMB)	1000	1	1.1	30
S1MF	SMAF	1000	1	1.1	30
S1MFS	SOD-128	1000	1	1.1	30
S1ML	Sub SMA	1000	1	1.1	30
S1MFL	SOD-123FL	1000	1	1.1	30
S1MLW	SOD-123W	1000	1	1.1	30

For ac-dc applications, the S1 can be routed on both sides of the PCB. On the bottom side of the PCB, the lower height of the smaller packages may be beneficial. On the top side of the board, you can use the smaller solder pads to save space because the power dissipation is minimal.

Package Height

In a lot of ac-dc applications, and others, a surprising number of rectifiers are routed on the bottom of the PCB, on the wave-soldering side. This is in many cases a good way to save space (in terms of the overall pc-board size) and it offers more space for solder pads, so larger pads may be used. In designs like these the height becomes crucial. The traditional SMA/B packages with their height over 2 mm are in many cases the highest components. But now a number of lower-profile solutions are becoming available.

For example, an SOD128 package can fit on both the SMA and SMB footprints (Fig. 4). This allows the designer to reduce the component height to 1 mm without changing the PCB layout, which could be an immediate advantage. If existing solder pads are maintained the designer should not see any increase in junction temperature.

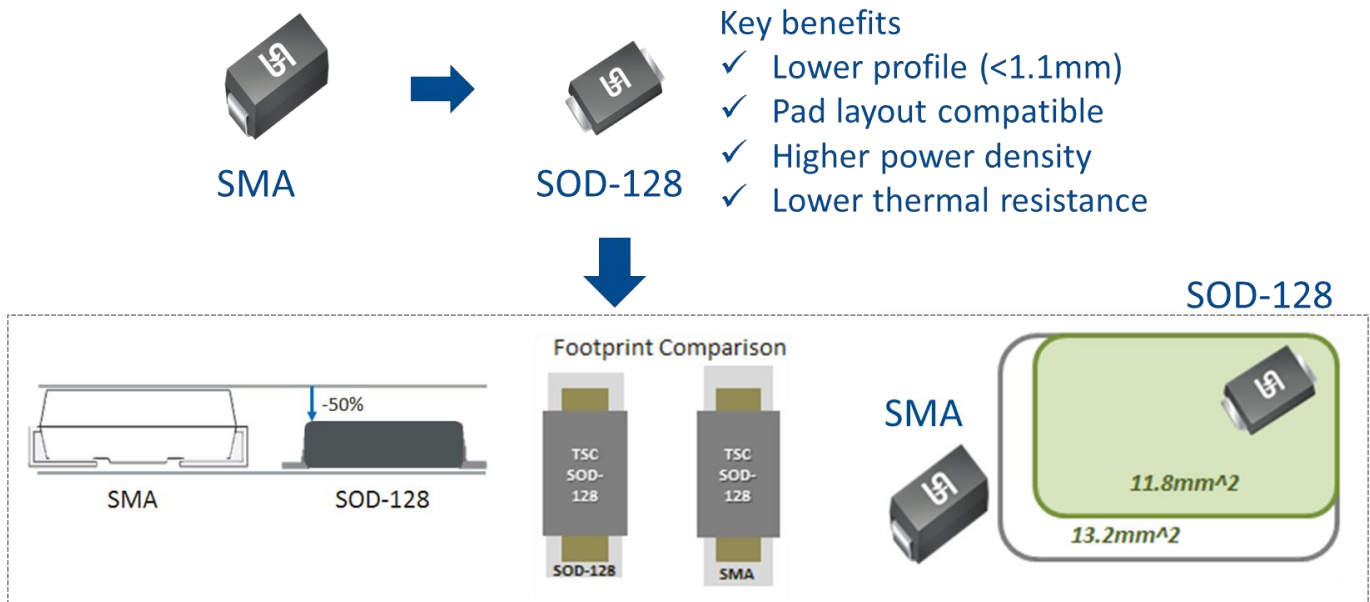


Fig. 4. Comparing heights and footprints of the SMA and SOD-128.

Thermal Resistance

Returning to the key formula, $T_J = T_A + P_d \cdot R_{\theta J-A}$, we observe that the thermal resistance junction-to-ambient ($R_{\theta J-A}$) consists of two parts: a package-related part and the contribution made by the solder pads—which is determined by the designer. To demonstrate this we chose measurements on the SOD123F. This package has very short leads. Packages like the SMA have very long leads which makes the definition of the lead temperature less accurate.

Tests on the S1MFL in the SOD123F package, which was mounted on 5-mm x 5-mm solder pads at room temperature on single-sided FR 4 with 35- μ m thick copper, gave the following results (Table 5).

Table 5. Thermal resistance measurements for an S1MFL in the SOD123F package.

I_F	2.06 A
T_j	148.95°C
T_l	121.4°C
T_A	22.4°C
$R_{\theta J-A}$ (junction-to-ambient)	68.3 K/W
$R_{\theta J-L}$ (junction-to-lead)	14.9 K/W

In this case we can safely split the thermal resistance in a package-related contribution $R_{\theta J-L}$ of 14.9 K/W and a contribution determined by the size of the solder pads of 43.4 K/W. The total thermal resistance is the sum of

both—68.3 K/W. In most designs on a single layer FR-4 PCB, the solder pads make, by far, the largest contribution to the total thermal resistance.

The T_J formula immediately tells us that smaller solder pads increasing $R_{\theta J-A}$ could be a potential issue. Very few designers use 5-mm x 5-mm solder pad areas, which are typically used by the device vendors to determine the thermal resistance.

Instead, designers tend to use the vendors' suggested solder pads for soldering, which are smaller (in some cases just 10% to 20% of the 5-mm x 5-mm solder pads used to measure the thermal resistance). As a result, the real thermal resistance $R_{\theta J-A}$ on single-layer PCBs when using the recommended solder pads may be higher than the value published in the datasheet. Expect an increase of 10 to 15 K/W.

On single-layer FR-4 style PCBs the size of the solder pads is the major contributor to the overall thermal resistance. Two-layer and four-layer PCBs reduce the thermal resistance. Using thermal vias is another good option. In higher-power designs, the more expensive IMS substrates are sometimes found. In all these designs, the overall thermal resistance is less dependent on very large size solder pads, and miniaturization is an option as well as increased power dissipation.

TSC also has introduced two new packages—the SMPC4.0 and the TO277A—with exposed pads. These packages offer second sources to similar packages from Diodes and Vishay. Exposed pads can help significantly in reducing board space in relation to the power dissipated. They also reduce the T_J by reducing $R_{\theta J-L}$, improving reliability. Also a smaller package called the SOD123HE package has exposed pads.

Current ratings of Schottky diodes, in particular, have been increasing in small packages. This does not mean that designers can use these packages at higher currents—but that designers can increase the efficiency by 10% to 20% due to the bigger die and the lower V_F . In the formula $T_J = T_A + P_d * R_{\theta J-A}$ it becomes immediately clear that you cannot increase power dissipation without reducing thermal resistance (for a given package). Increasing the T_J would reduce your reliability.

Trench Schottky technology is a major contributor to the package size reduction and increased efficiency. When comparing the performance of a planar and a Trench Schottky—at a given die size and breakdown voltage and barrier material—the Trench Schottky die will have a better V_F and lower leakage current. Its capacity may be higher. When making designs smaller, the risk of thermal runaway increases, and again Trench Schottky technology brings benefits.

Basically a snubber is one of these applications where axial rectifiers/TVSs are still used—as well as SMAs and SMBs. They tend to be routed on the top side of the PCB. This is a typical example where miniaturization will not work because of the higher power dissipation.

Estimating the impact that miniaturization will have on a specific design using a datasheet is not so easy. Thermal resistance is not an exact science. Manufacturers use software to simulate temperatures and to optimize designs.

In the everyday design world, thermal cameras are used to measure the temperatures on a PCB. Many designers know the rectifiers are usually among the hottest components on the board. When measuring, try to establish the temperature of the lead as close as possible to the package.

The potential to miniaturize will depend on the type of PCB used and the power dissipated.

Process Improvements On Rectifiers And TVS Diodes—Zero Defects

Rectifiers are still mainly produced using glass passivated pellet (GPP) processes and in four-inch fabs. Even though their processes lack the sophistication of MOSFET and other discrete processes, huge steps forward have been made in reliably producing rectifiers. TSC now manages a defect level less than 10 ppb on its rectifier products.

PAT Testing And AEC-Q101

Rectifiers are older components. For example, the 1N4007 was introduced in 1965. Another part, the S1, is more than 30 years old. Their datasheets still reflect this—the best example being a leakage current specification of 5 μ A. This does not reflect the natural distribution of the process.

A very important contribution to a zero defects strategy is part average testing (PAT). The test specifications on the main parameters are set to 4 or 6 sigma values by software. Especially on the leakage currents, datasheet values do not reflect the natural distribution. Even if I_R testing is reduced to 1 μ A instead of the 5- μ A datasheet value, a lot of products with potential mechanical damage, passivation problems and contamination issues can be shipped to customers. These products have a reduced reliability and may produce early HTRB or Intermittent Op Life failures. PAT testing eliminates these by setting the test limits to the normal distribution on I_R (Fig. 5).

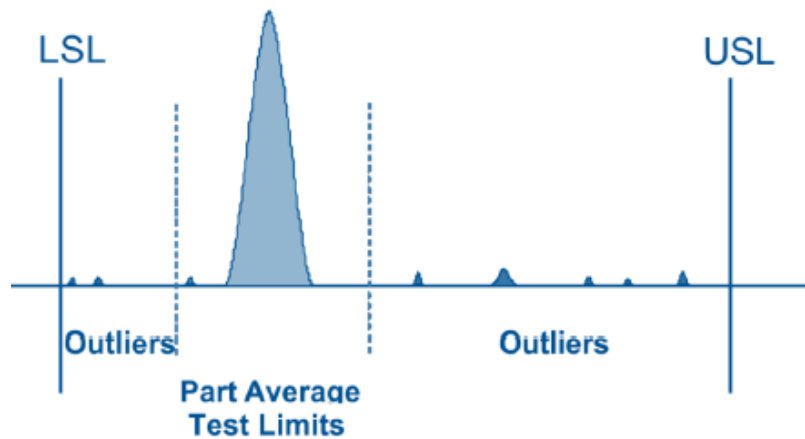


Fig. 5. Part average testing.

Commercial practices had a negative impact on rectifier reliability in the past. In many cases rectifiers use only one die for several different part names. In standard rectifiers, the 1000-V product (also called the prime bin) usually has the same die as the 50-V and 100-V product. Some suppliers sell products that failed the 1000-V tests as lower voltages, and offer significant discounts on lower voltage products like 100-V parts. This has a negative impact on product quality and FIT (failure in time) data. To some degree, these practices persist.

Automation And Reduction Of Solder Voids

In ac-dc conversion applications, no 100% outgoing quality control (OQC) test is possible to monitor I_{FSM} —the surge rating—of a rectifier. A delta V_F test (measuring the V_F before and after a short current pulse) monitors the thermal resistance and eliminates the worst soldered devices.

When SMA devices were first introduced they were manufactured using belt furnaces for soldering. These processes had inherent issues with solder voids and fluctuations in I_{FSM} surge capability. New backend soldering improvements with matrix lines and vacuum soldering eliminate these risks. In addition, the SMD packages discussed are now manufactured using fully automated equipment in a cleanroom environment. Moving production to a cleanroom environment has been a major contributor to achieving zero defects, along with other improvements discussed in this section.

Reducing solder voids improves the temperature cycling performance. Coffin Manson models may be a better predicting factor for some automotive applications than Arrhenius models.

Conclusion

Despite the fact that rectifiers use less advanced processes than MOSFETs or other discrete components, improvements have been made in recent years. Smaller packages have been introduced, reliability standards have increased and product innovation continues. These advancements may not be as spectacular as the progress made by other semiconductor technologies, but the fact that TSC and some other vendors can now supply rectifiers with zero defects is a major step forward for the power management industry.

About The Authors



Jos van Loo is a technical expert on power semiconductors with more than 30 years' experience. In his role as technical support engineer at Taiwan Semiconductor Europe, Jos consults with customers on rectifiers, MOSFETs and power management ICs.



Kevin Parmenter is an IEEE Senior Member and has over 20 years of experience in the electronics and semiconductor industry. Kevin is currently director of Field Applications Engineering North America for Taiwan Semiconductor. Previously he was vice president of applications engineering in the U.S.A. for Excelsys, an Advanced Energy company; director of Advanced Technical Marketing for Digital Power Products at Exar; and led global product applications engineering and new product definition for Freescale Semiconductors AMPD - Analog, Mixed Signal and Power Division. Prior to that, Kevin worked for Fairchild Semiconductor in the Americas as senior director of field applications engineering and held various technical and management positions with increasing responsibility at ON Semiconductor and in the Motorola Semiconductor Products Sector. He holds a BSEE and BS in Business Administration.

For further reading on power semiconductor packaging, see the How2Power [Design Guide](#), and locate the Design Area category and select "Packaging and Interconnects." For more on diodes and rectifiers, see the How2Power [Design Guide](#), and locate the Component category and select "Diodes and Rectifiers."