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Versatile SiC JFETs Benefit Power Switching And Circuit Protection Applications

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After more than two decades of promise, SiC switch technology has finally emerged as a contender for various power electronics applications, driven largely by adoption in automotive and industrial charging sectors, energy storage, PV inverters and even EV drivetrain inverters.[1] Continued advancement in cost-performance metrics of SiC switches have even yielded inroads in growing volume applications such as telecom rectifier and server power supply applications, where silicon superjunction FETs have reigned supreme.

Although most of the major players in the power semiconductor world have focused their attention on SiC MOSFETs, the case can be made that the SiC JFET is the highest performance and most versatile switch technology available. In this article, we examine some of the unique attributes of SiC JFETs that are so attractive across a variety of potential applications.

After reviewing the key characteristics of SiC JFETs, we describe their performance advantages when applied in cascode configurations and used with particular power supply topologies and switching schemes. An extension of the single-JFET cascode, the "supercascode" combines a low-voltage silicon MOSFET with multiple series-connected SiC JFETs. The supercascode devices offer higher performance alternatives to silicon IGBTs and thyristors in medium voltage (6.5 kV to 10 kV+) and high voltage (tens of kilovolts and higher) power switching applications. Finally, we discuss how the low on-resistance and robustness of SiC JFETs provide performance advantages in power switching and circuit protection applications.

SiC JFET Structure

The SiC JFET, as depicted in Fig. 1 is a vertical device, fabricated with high cell density, thin drift layers (5 to 15 µm, for voltage ratings from 650 V to 1.7 kV) and without dielectric interfaces where high electric fields are present. As such, the good bulk electron mobility (~750 cm^2/V-s) combined with high doping concentrations and thin layers allowed by SiC's high critical electric field give the SiC JFET the lowest specific on-resistance of any commercially available technology for voltage ratings between 650 V and 1.7 kV. The UnitedSiC 650-V, vertical JFET technology features an exceptional R_{DS} x A figure of merit as low as 0.75mΩ-cm^2.[2]

At first glance, the normally-on characteristic of the SiC JFET depicted in Fig. 1 might appear as a shortcoming in the world of power semiconductors. However, this attribute along with its architecture, gives the SiC JFET a great deal of versatility, wherein the same device platform can offer very low on-resistance, fast, normally off switches when configured in cascode with low-voltage MOSFETs, voltage scalability (650 V to tens of kilovolts) and a robust, tunable current limiting operation.

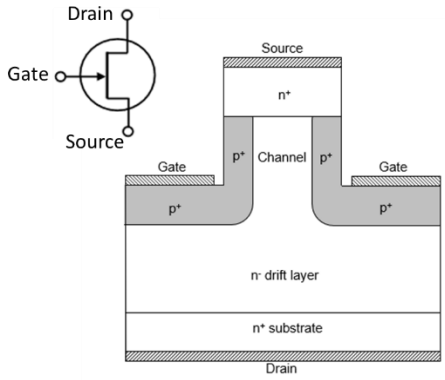

Fig. 1. Schematic depiction of vertical SiC JFET.

SiC JFET Cascode In High-Frequency Applications From 650 V And Above

When configured in a cascode with the correct low-voltage Si MOSFETs (as shown in Fig. 2), the SiC JFET becomes a superior switch in the 650-V to 1.7-kV class. The device's normally-off operation is achieved using the extremely cost-effective and high-performance low-voltage Si MOSFET, capable of being operated with V_{GS} = ±25 V but only requiring 0 V to 12 V for most switching applications. The high threshold voltage V_T = 5 V gives good noise immunity while the wide allowable V_{GS} range allows users to use standard gate drives, compatible with Si or SiC switches already being used.

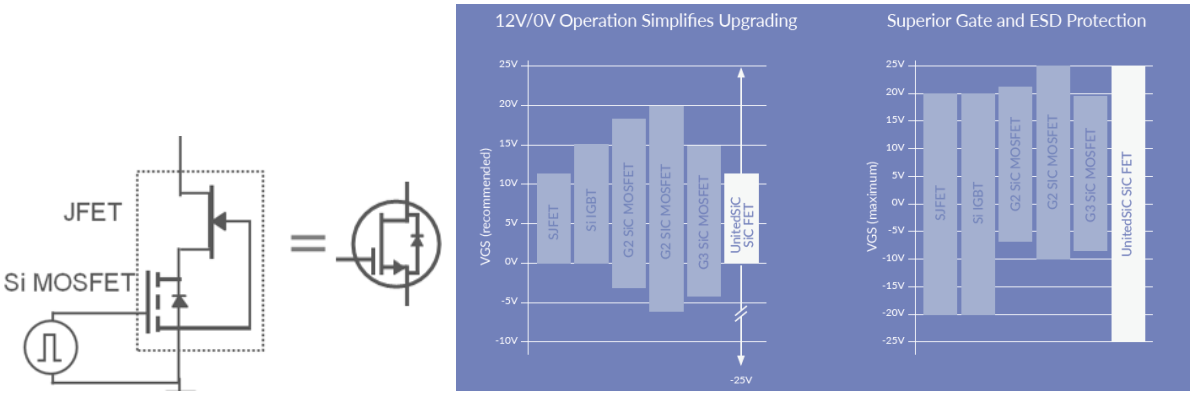

Fig. 2. A SiC JFET cascode with low-voltage Si MOSFET achieves optimum performance with a standard Si gate-drive voltage of 0 V to 12 V but allows a V_{GS} of ±25 V.

The Si-SiC cascode configuration employed by the UnitedSIC FET also exhibits a high-performance integral body diode, superior to that of a conventional SiC MOSFET or Si superjunction FET. Here, a low V_F of 1.5 V is achieved with the smaller knee voltage of the Si MOSFET's body diode (0.7 V) and low drift-resistance of the SiC JFET. The resulting integral diode maintains a low Q_{rr} even at 150°C.

However, even this performance can be improved with modern control schemes that employ synchronous rectification wherein the switches' channel is turned on in the third quadrant, further lowering the forward voltage drop after a short freewheeling dead-time. Fig. 3 shows the body diode and third-quadrant I-V characteristics of a 1200-V/80-mΩ Si-SiC cascode along with measured diode-reverse-recovery characteristics.

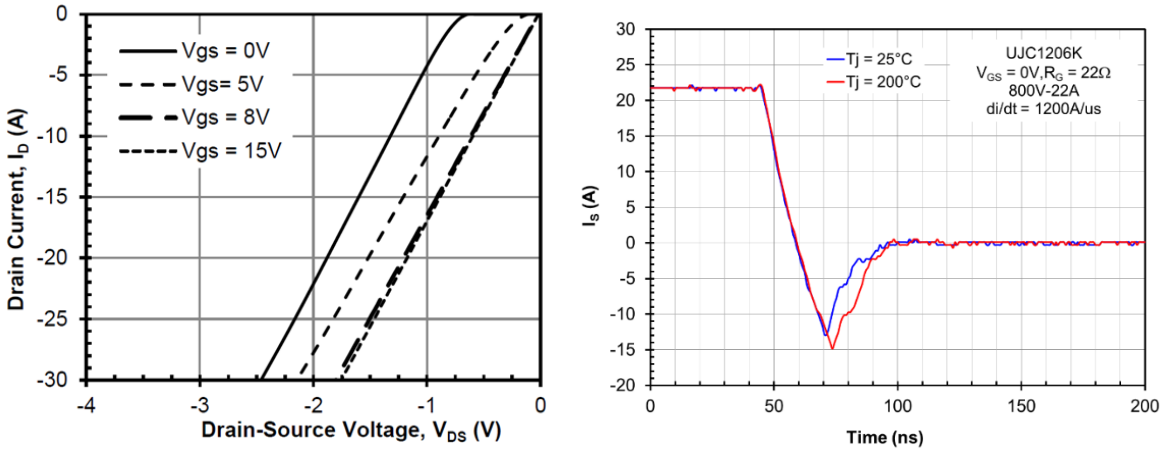

Fig. 3. Integral body diode characteristics of a 1.2-kV SiC JFET-based cascode. Note the minimal change in Q_{RR} even at 200°C.

When in cascode configuration, the JFET's low $R_{DS(ON)}$ x A (smaller die size), fast integral diode and low output capacitance (C_{oss}) result in very low switching losses. Fig. 4 shows the measured switching losses of a 1.2-kV/35-mΩ SiC JFET-based cascode when hard-switched at 800 V and T_J = 125ºC. In these measurements, the device was packaged in a 4-L, Kelvin source-connected TO-247 and a small 10-Ω/115-pF RC-snubber was connected to the drain-source of the device to achieve clean waveforms with no gate-source ringing. The device exhibits approximately 1.2-mJ total loss (1-mJ turn-on loss and less than 200 µJ of turn-off loss) when switching as much as I_D = 50 A in the leaded package.

Although the losses shown are taken hard-switched in a half-bridge configuration, even lower losses are achievable in soft-switching ZVS operation where predicted losses under the same conditions are approximately 100 µJ assuming $E_{Off,SSw} = E_{Off-HSw} - (E_{oss} + E_{CS})$.

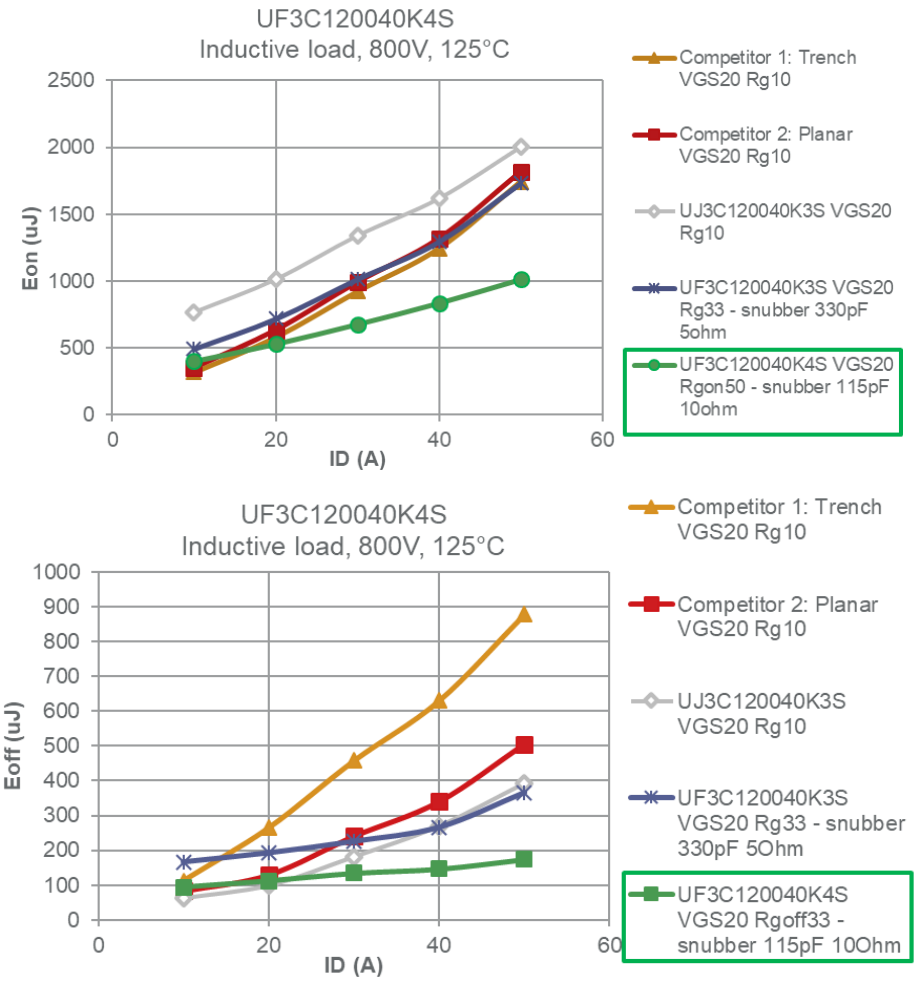

Fig. 4. Measured switching losses for a hard-switched 1.2-kV/35-mΩ SiC JFET-based UnitedSiC FET versus 1.2-kV SiC switches.

The low conduction and switching losses obtained with the SiC JFET-based cascodes make them very attractive for hard-switching applications such as totem pole PFC as well as soft-switching applications such as phase-shifted full bridge.

Normally-on SiC JFETs are also ideal devices for a wide range of low-power flyback converter applications. Ranging from 650 V to 1.7 kV, SiC JFETs provide a simple, high-efficiency, cost effective solution for these low-power, high-frequency converters across a range of consumer and industrial applications. When integrated with

the low-voltage MOSFET and control IC as depicted in Fig. 5, the SiC JFET offers no standby power dissipation with a simplified start-up scheme.

During startup, current flowing from the bus via the JFET Q2, D2 and R1 will charge C1 until the undervoltage lockout (UVLO) limit of the control IC is reached. Q1 will then begin to switch, forming the cascode and its efficient switching characteristics. During steady-state operation, control-IC power is supplied from the auxiliary winding and no steady-state bias is drawn from the HV bus.

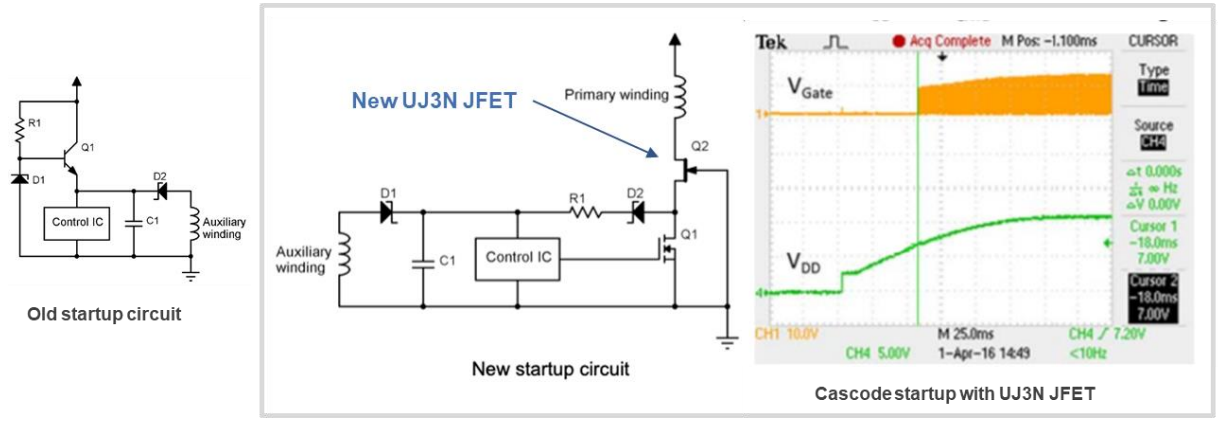

Fig. 5. A simplified flyback converter startup circuit with normally-on SiC JFET in cascode with a low-voltage MOSFET integrated with control IC. The auxilliary startup circuit is eliminated.

SiC Supercascodes For Medium- And High-Voltage Power Switching

Stemming from its large critical electric field (~10x higher than Si), SiC is an obvious candidate for medium voltage (MV) power conversion and distribution applications where high-voltage Si IGBTs (3.3 kV to 6.5 kV) and thyristors (up to 10 kV) have been the workhorse of the industry. However, achieving commercial success with high-voltage SiC switches requires overcoming several practical challenges.

First, the active layers of high-voltage SiC devices are formed by epitaxial growth of low-doping, low defect films (as opposed to a FloatZone growth processes in Si). These layers can be ~55 to 100 µm+ thick for 6.5-kV to 10-kV devices, which reduces epi-reactor throughput, increases maintenance and consumables costs, and can reduce yield. Meanwhile, since SiC devices are unipolar devices (i.e. SiC MOSFETs), their specific on-resistance increases with a power law relationship to their voltage rating ($R_{DS(ON)} \sim BV^{[2.4]}$).

These factors result in the need for large die (~1 x 1 cm), which must be parallel connected to achieve practically rated medium-voltage switches. One can imagine that the cost of such solutions can become prohibitively high and requires technology advances beyond the economy of scale that the lower-voltage (650 to 1.2 kV) SiC market is just now beginning to leverage.

Leveraging the normally-on SiC JFET, UnitedSiC has employed the "supercascode" architecture to overcome these voltage-scaling challenges.[3] In this approach, a single low-voltage, normally-off stage is used to control a series-connected, multi-stage, normally-on SiC JFET network. This allows lower voltage (ex. 1.2 kV to 1.7 kV) devices to achieve the voltage ratings required for MV power electronics applications (6.5 kV to 10 kV+). A simple, low-cost passive balancing network is used to maintain good voltage sharing among levels under both static and dynamic conditions.

Fig. 6 shows a 100-A/6.5-kV SiC supercascode half-bridge module implemented with 20, 1.7-kV, 5.7-mΩ SiC JFETs to achieve a total on-resistance of 20 mΩ per switch. The double-pulse measurements show very low switching losses (E_{SW} = 184 mJ at V_{DC} = 3.6 kV and I = 200 A) which are less than one-tenth of a comparably rated IGBT. This module is implemented with the same total SiC die area as a comparably rated module with 6.5-kV SiC MOSFETs connected in parallel, while the 1.7-kV JFETs are based on a mature product platform already running in mass production.

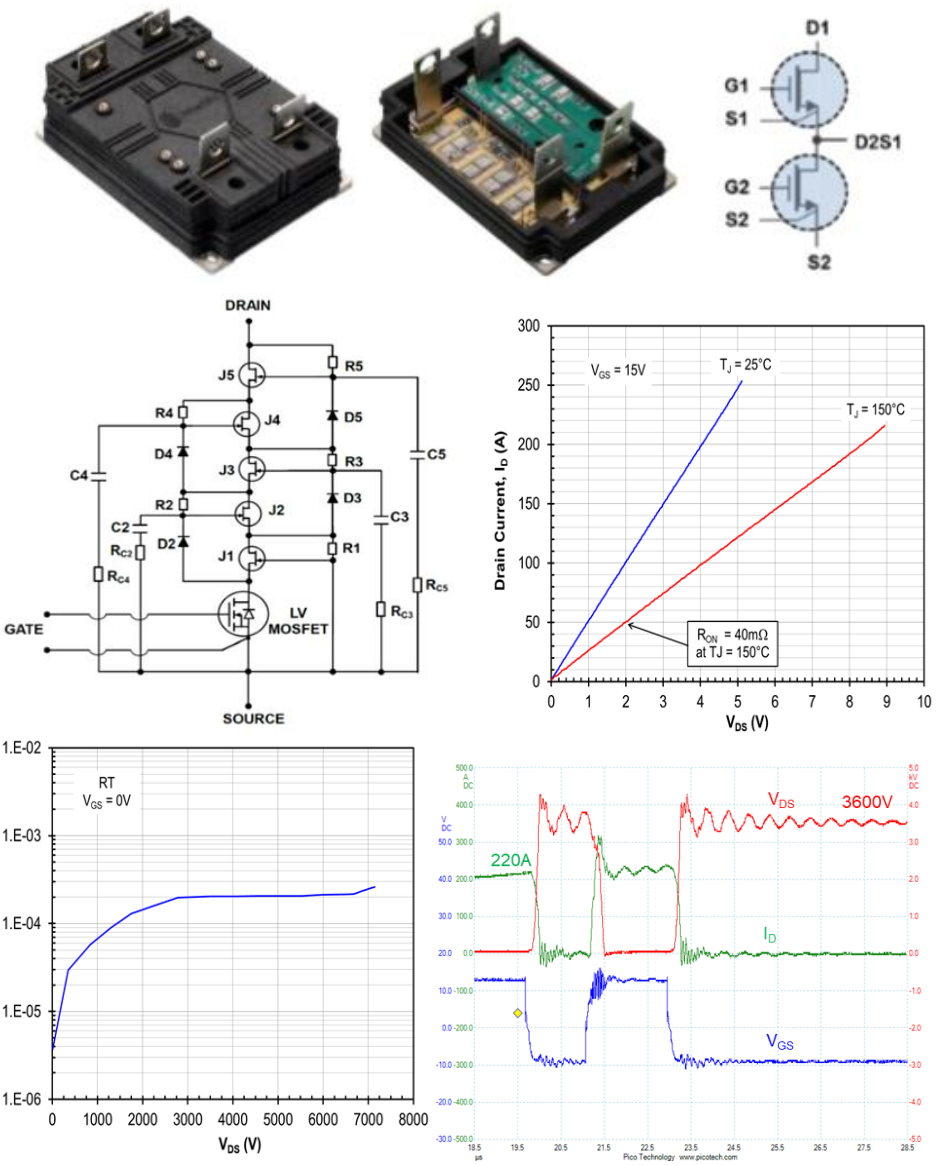

Fig. 6. 6.5-kV/100-A SiC JFET-based supercascode half-bridge modules and their measured characteristics.

Using the supercascode approach, one can scale to very high voltages while still employing commercially practical semiconductors. In this vein, UnitedSiC has recently demonstrated a compact (127-mm x 43-mm x 59-mm) 40-kV, normally-off switch using series-connected 1.7-kV SiC JFETs.[4]

Low On-Resistance And High Robustness For Switch And Protection Applications

SiC's material properties give rise to very low on-resistance, high blocking voltages, good thermal conductivity and low intrinsic carrier concentrations even at high temperatures. These factors make SiC switches near ideal candidates for use as circuit protection components such as load switches, solid-state relays, current limiters and solid-state circuit breakers. SiC JFETs offer superior characteristics for these applications including the

lowest on-resistance, easy gate control, no MOS interface, excellent current saturation and a small temperature dependence of threshold voltage.

Fig. 7 shows the specific on-resistance of SiC JFETs versus blocking voltage along with the 1-D limit for Si and SiC unipolar devices. One can see that for voltages of ~600 V and higher, the SiC JFET performance is unmatched. While Si IGBTs offer low conduction losses for power switching applications, their knee voltage (0.7 V) becomes problematic for inline protection wherein losses should be kept very low (rivaling their mechanical switch predecessors).

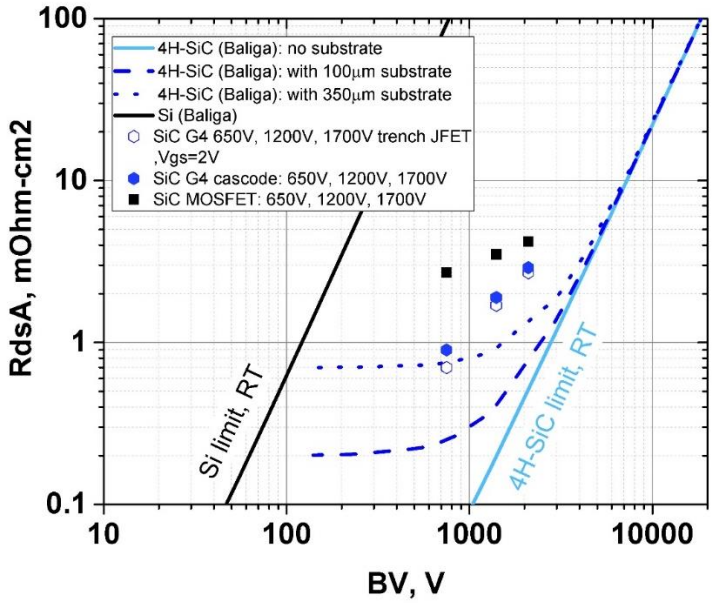

Fig. 7. 1-D unipolar limit of specific on-resistance versus breakdown voltage for Si and SiC devices.

As an example of this performance, Fig. 8 shows a very compact (SOT-227 footprint dimension of 38 mm x 28 mm) normally-off, SiC JFET-based cascode switch module (UF3SC120002SNS) that is rated at 1.2 kV and 2 mΩ, nominally. In this device, six of the 1.2-kV/8.6-mΩ stacked cascodes from UnitedSiC (UF3SC120009Z) are parallel connected to achieve very low on-resistance and high peak current capability. Also shown in Fig. 8 are the high-current (t_p = 50 µs) characteristics of the module, safely conducting >3 kA (T_j = 175˚C).

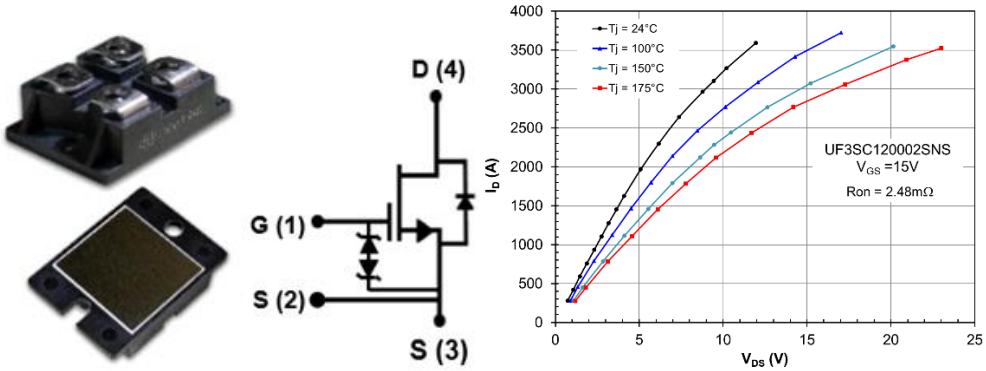

Fig. 8. A 1.2-kV/2-mΩ SiC JFET-based, normally-off switch in a 38-mm x 28-mm package (UFSC120002SNS).

Aside from their superior on-resistance, SiC JFETs also have a slight negative temperature dependence of threshold voltage, which is mitigated by the carrier mobility reduction with temperature. This yields stable active-mode operation that is critical for achieving robust current limiters. In contrast, SiC MOSFETs typically show a strong negative threshold voltage dependence, and soft saturation characteristics that result in unstable operation in the active mode.

Fig. 9 shows the active-mode transfer I-V characteristics of SiC JFETs and SiC MOSFETs at various temperatures. Note that the SiC JFET gate voltage V_{GS} required to sustain a given current in active mode increases with temperature, even down to very low currents. By plotting the parameter α_T defined as the dI_D/dT, one can see from Fig. 10 the propensity of SiC MOSFETs to form hot-spots and filament in the active mode compared to the stable operating window of SiC JFETs.

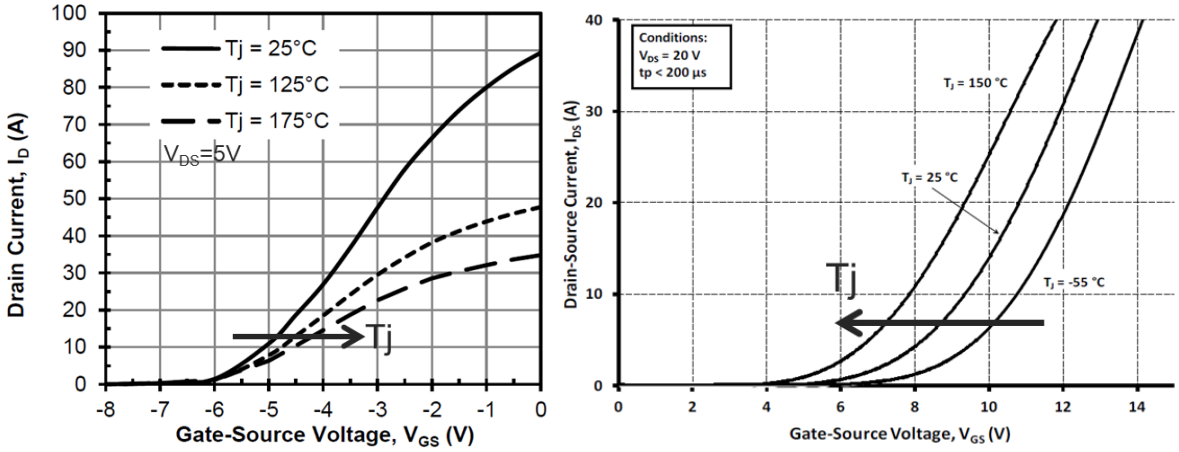

Fig. 9. Active-mode transfer IV characteristics of SiC JFET (left) and SiC MOSFET (right).

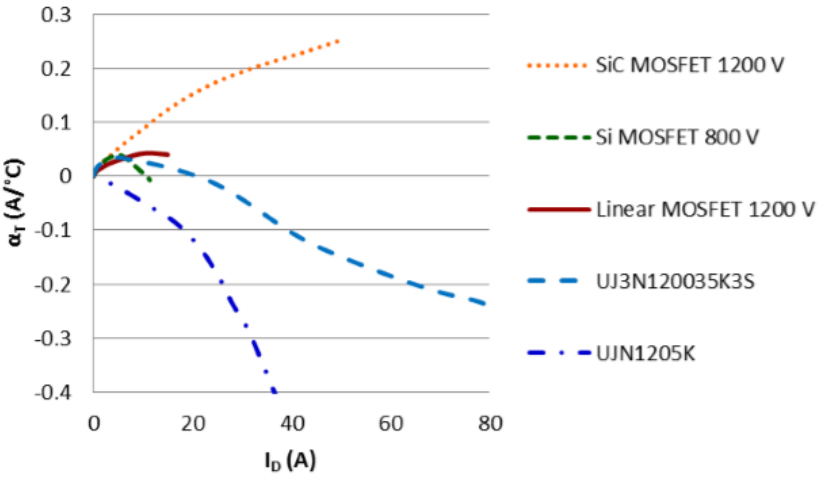

Fig. 10. Active-mode temperature stability of various power FETs as defined by the parameter α_T = dI_D/dT. SiC JFETs show a negative dependence of I_D versus temperature across a wide operating current range with little to no propensity for hot spots.

SiC JFETs can be designed to have very good current saturation characteristics at little expense of on-resistance under nominal operation. Likewise, these devices can offer superior short-circuit performance compared to their SiC MOSFET counterparts. Fig. 11 shows the tradeoff in specific on-resistance and short-circuit time (defined by topside Al metallization to reach 660˚C) versus threshold voltage for a 1.2-kV SiC JFET. It is clear that with only marginal increases in $R_{DS(ON)}$ (15% or less), the short circuit withstand time can be doubled to more than 10 µs.

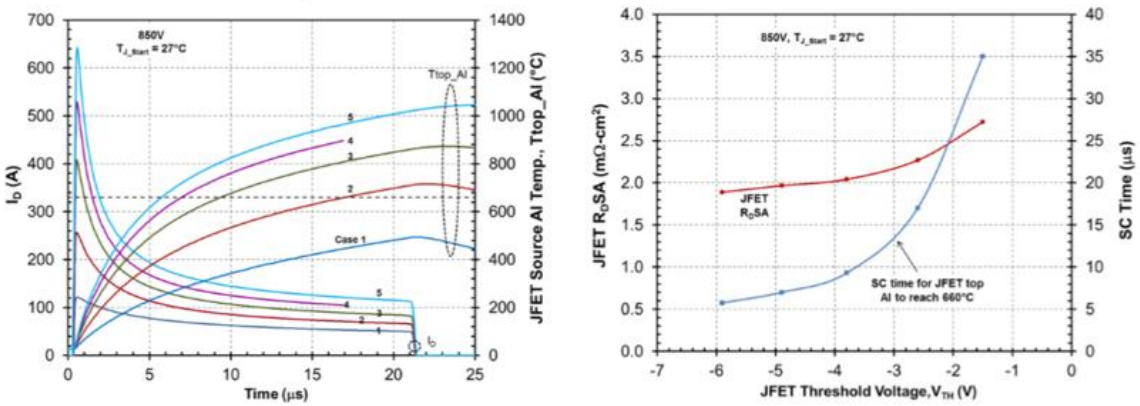

Fig. 11. Electro thermal simulations of SiC JFET short circuit performance showing simulated heating under short circuit (left) and design tradeoff between nominal R_{DS} x A and short-circuit time to reach power metal melting point (right).

Fig. 12 shows the measured short circuit waveforms of a 650-V/100-A (7-mΩ/0.9mΩ-cm^2) SiC cascode. The device safely survives more than 8 µs in short circuit with V_{DS} = 400 V after exhibiting a self-limiting peak current of 400 A, respectively (4:1 compared to nominal). The devices can safely withstand multiple shots of short circuit fault with no measurable degradation. The devices fail after a short circuit time of approximately 10 µs.

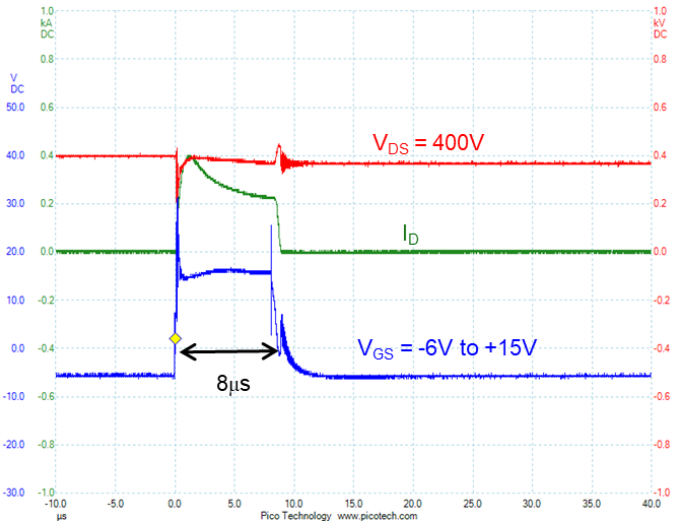

Fig. 12. Measured short-circuit waveforms of a 650-V/7-mΩ SiC cascode. The 100-A rated devices safely withstand >8 µs of short circuit and have ultra-low specific on-resistance of 0.9 mΩ-cm^2.

The intrinsic current limiting function and high intrinsic junction temperature of the SiC JFET can be exploited to achieve very robust inrush current limiters, transient suppressors and even circuit breakers. Fig. 13 depicts SiC JFETs in a common-drain configuration with gate/source shorted resulting in a two-terminal device with bidirectional current limiting characteristics. When combined with voltage clamping diodes (TVS), the simple circuit achieves both inrush current limiting and overvoltage protection functionality.

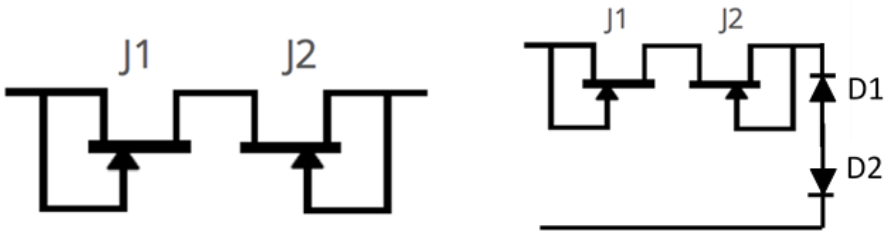

Fig. 13. Schematics for SiC JFETs connected in bidirectional current limiting mode (left) and current limiting with voltage protection using TVS, clamping diodes (right).

We apply this concept as a lightning surge protection device when exposed to a WF5A 1500-V/1500-A waveform using TCAD numerical transient thermal analysis. Fig. 14 indicates the device can safely meet the surge with the current limiting and self-heating, resulting in a peak temperature well below the intrinsic temperature of the SiC (>1000˚C) and the melting point of the topside metallization (660˚C). In this case, a source impedance of 1 Ω was required and the selected design was approximately 0.45 Ω.

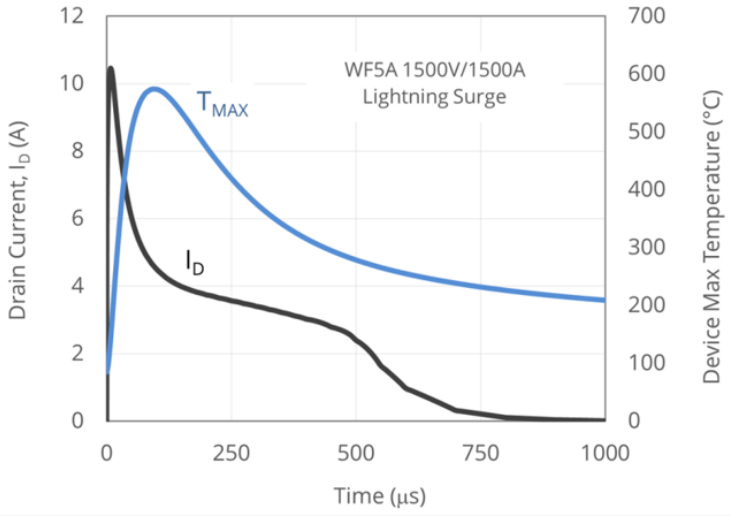

Fig. 14. Transient thermal simulations of a SiC JFET-based current limiter designed for <1 Ω when subjected to a WF5A 1500-V/1500-A surge waveform.

The ultra-low on-resistance, high blocking voltage, good avalanche and short circuit capability of SiC JFETs make them extremely attractive for dc and ac breaker applications. In Fig. 15, we show an example of a SiC JFET-based dc breaker as upstream protection for the critical power electronics.

Depending on the line inductance between the dc source and the converter, one may use clamping diodes, or metal-oxide-varistors (MOVs) in parallel with the drain-source of the SiC JFET switch to safely dissipate the stored energy during turn-off. This switch can be controlled with a standard gate drive, or even self-powered with an isolated converter connected to the gate as was demonstrated by researchers from University of Illinois.[5] Much like the supercascode, the normally-on nature of the SiC JFET also allows it to be scaled to higher-voltage current limiter or circuit breaker applications.

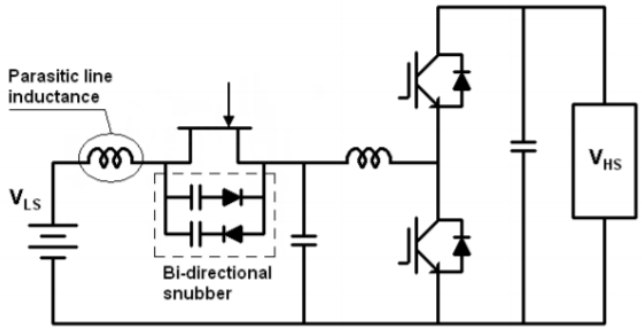

Fig. 15. A SiC JFET-based dc breaker with bidirectional snubber or MOV to absorb high amounts of energy from line inductance upon turn-off.

In this article we have reviewed the SiC JFET and its attributes that make it a uniquely versatile power switch from 650-V to 10-kV+ applications. Stemming from its ultra-low on-resistance, low output capacitance, remarkable ruggedness, stability and high-temperature capability, the SiC JFET is poised to continue its growing adoption in a wide variety of applications.

Already finding acceptance in cascode-based high-frequency power switching applications, such as PFC, dc-dc converters and inverters from 100 W to tens of kilowatts, the SiC JFET and its benchmark performance will no doubt continue to find design wins in emerging areas of solid-state protection, electronic loads and medium-voltage power electronics.

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For further reading on wide-bandgap power devices, see the How2Power Design Guide, locate the Poplar Topics category and select "Silicon Carbide and Gallium Nitride". Also see How2Power's special section on SiC and GaN Power Technology.