ISSUE: November 2019

Accelerating UPS Wake-Up Can Improve Power Supply Efficiency

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Continuous power flow is critical for reliable IT equipment operation. Unfortunately, the ac utility power isn't as steady as needed: brief power sags and outages can result in system resets, data loss, or even malfunction and fault. In dealing with transient power fluctuations an uninterruptible power supply (UPS) becomes one of the key components in the datacenter power distribution infrastructure.

A UPS takes in primary ac or dc power, stores a portion of the energy in the backup battery and transfers the remaining energy to the connected equipment. There are two major types of UPSs—online and offline (standby). An online UPS continuously converts all ac power to dc. Some of the dc power charges the battery, and the rest of it is converted back to ac to power the IT equipment. A standby (offline) UPS monitors the power that is supplied by the utility grid and does not switch over to the battery power until it detects a problem in the ac feed.

Each type of UPS has its impact on power delivery efficiency. In an online UPS the normal operation efficiency is affected by double conversion. With an offline UPS the power delivery efficiency in normal operating mode is impacted by an ac-dc power supply holdup time requirement: this time needs to exceed the time required for ac fault detection and switching over to the battery power (which usually takes several milliseconds).

For corporate data centers, where downtime is unacceptable and expensive equipment must be protected from power quality problems, standby UPSs are usually insufficient and usage of double conversion (online) UPSs is required. However, recently the standby UPS has expended its reach in the industry in the form of the dc UPS, which integrates battery backup (BBU) modules into the server power subsystems. General block diagrams of the three UPS arrangements are shown in Fig. 1.

Because such modules do not use double conversion and therefore do not dissipate power under normal operating conditions, their usage increases the datacenter infrastructure power delivery efficiency and reduces total cost of ownership (TCO). Using such dc BBU modules and integrating them into ac-dc power subsystems can also noticeably improve the scalability of the UPS, and give the user an opportunity to properly shut down equipment or to switch to the emergency (standby) generator.

When power delivery is arranged so that a battery can be coupled to the PDN without any buffer modules, it benefits ac-dc power supply efficiency. However, the wide voltage swing of the battery may require additional conversion stages to maintain regulated voltage to the load and those additional stages offset the efficiency advantage of the offline UPS.

With fast fault detection and accelerated redundant power supply wake-up methods developed for servers,[1, 2] the dc UPS wake time can be drastically shortened versus that of the standard ac offline UPS, even when the battery is not directly interfaced to the dc PDN. This means that speeding up the standby UPS wake-up process creates an opportunity for significant efficiency improvements by taking advantage of both types of UPSs (offline and online). Implementation aspects and benefits of such backup power architectures are discussed in this article.

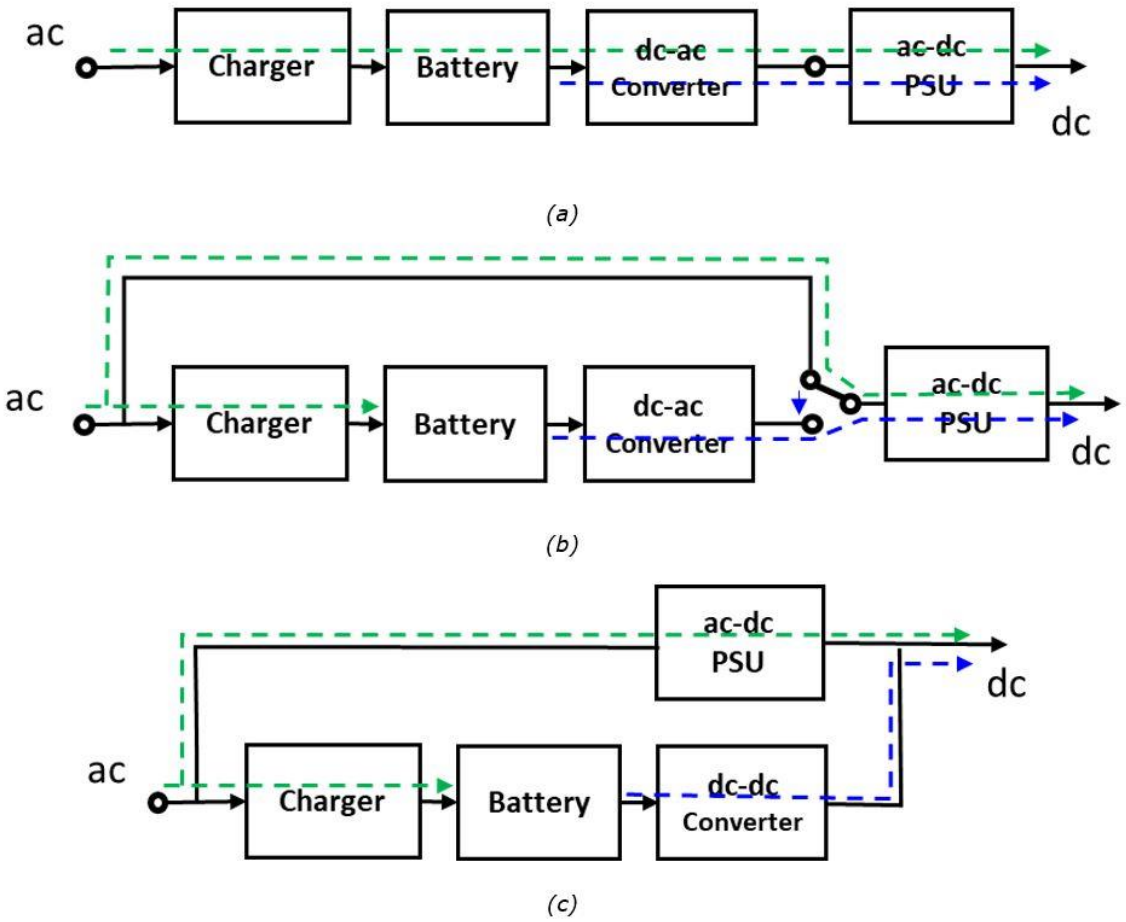

Fig. 1 General block diagrams of the three most common UPS arrangements: online UPS (a), offline (standby) UPS (b) and dc battery backup (offline-type) UPS (c). Energy flows in normal operation and backup power modes are shown with green and blue dashed lines, respectively.

We begin by explaining the processes that occur during the hold-up time (HUT), when the UPS is switching over to battery power, derive an expression for the bulk capacitor voltage as a function of HUT, and discuss how shortening HUT can improve power supply efficiency. We then discuss the techniques which can be applied to shorten HUT including disabling soft start of the BBUs and speeding up ac fault detection for the ac-dc power supply. Use of a cold redundancy technique to speed wakeup of the BBUs and a fast ac fault detection method to detect loss of ac power are described.

Then, example calculations demonstrate the potential improvement in dc UPS efficiency that is obtainable when accelerated wakeup is employed. Finally, some additional ideas are presented for using fast ac and dc fault signals to speed wakeup and improve efficiency in dc UPS architectures.

Impact Of Hold-Up Time On PSU Efficiency

The hold-up time of a power supply unit (PSU) is the time the PSU must maintain the output voltage within its specified range, after a loss of input ac power. The HUT is required for a smooth transition to the UPS power, which accounts for the time required to perform ac fault detection and switching to battery power, which can traditionally take up to 10-12 milliseconds (ms). HUT may also be required for the soft start of a dc-dc converter (buffer module) interfacing the IT equipment.

Let's take a closer look at the processes that occur inside the PSU after the ac power flow gets interrupted. During the HUT interval, energy to the PSU is supplied by its primary bulk capacitor, whose voltage reduces in

time as it supplies its energy. The cap voltage $V_c(t)$ changes according to the following expression derived from the energy balance equation:

$$V_c(t) = \sqrt{V_{c0}^2 - 2 \cdot P_o \cdot t/(Eff \cdot C)}\ ,$$

where V_{c0} is initial cap voltage, P_o is output power, *Eff* is dc-dc stage efficiency and *C* is capacitance value. Dividing both parts of this equation by V_{c0} and defining the ratio of C/P_o to be capacitance $\widehat{C_s}$—the capacitance needed to support a watt of load power—we can rewrite the above equation to obtain an expression for the normalized minimum bulk capacitor voltage at the end of the HUT interval t_{HUT}:

$$\widehat{V_{c.min}} = \sqrt{1 - 2 \cdot t_{HUT}/(Eff \cdot V_{c0}^2 \cdot \widehat{C_s})} \qquad (1)$$

A typical rule of thumb recommends starting with $\widehat{C_s}$ = 1 µF/W before optimizing the bulk capacitance.[3] Assuming *Eff* = 0.95 and V_{c0} = 400 V, we can plot the normalized minimum bulk capacitor voltage as a function of the required HUT. This graph obtained from Eqn (1) is shown in Fig. 2 for two specific capacitance values—$\widehat{C_s}$ = 1 µF/W and $\widehat{C_s}$ = 0.7 µF/W.

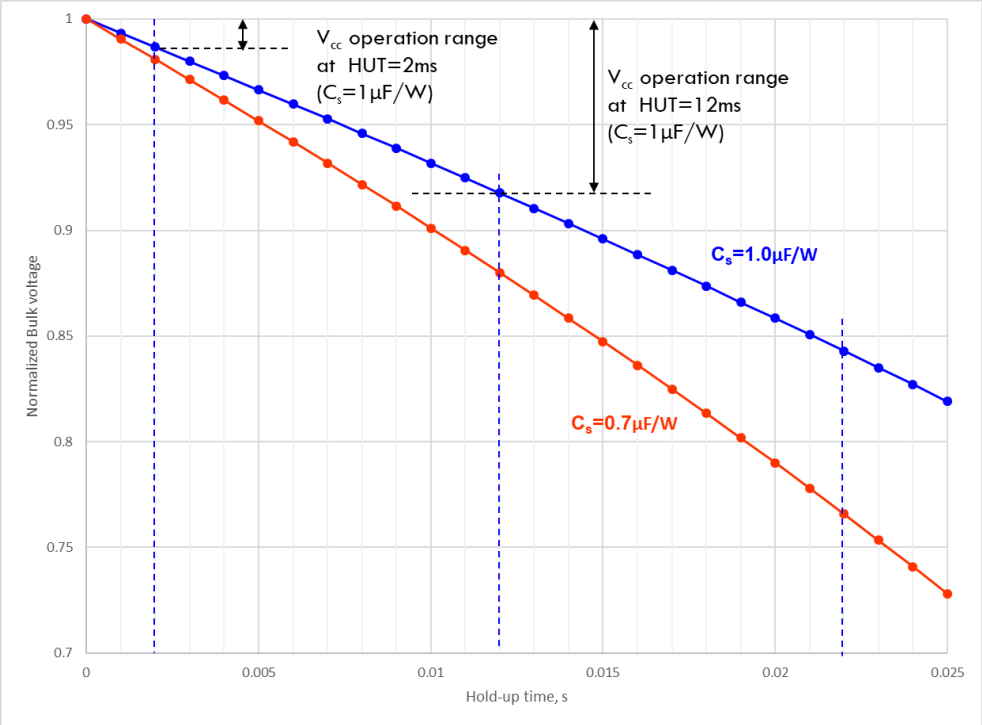

Fig. 2. Minimum normalized bulk capacitor voltage as a function of the required hold-up time. With reduced HUT, the dc-dc stage V_{cc} operating range can be also significantly decreased, which enables an improvement in PSU efficiency.

The PSU dc-dc converter parameters, such as primary transformer winding and MOSFET currents, and synchronous rectifier voltage magnitude, directly depend on the power transformer turns ratio w_2/w_1. This ratio in turn is proportional to the minimum PFC output (bulk cap) voltage at which the converter still needs to regulate ($\widehat{V_{c.min}}$). As it can be seen from the graphs in Fig. 2, a shorter HUT leads to a higher $\widehat{V_{c.min}}$, which in turn results in a narrower converter operating voltage range and therefore a potentially higher efficiency can be achieved in the dc-dc stage. Let's quantify how much the HUT can be shortened in real applications and what benefits it can provide.

Opportunities For HUT Reduction

As mentioned earlier, the PSU HUT is needed for ac fault detection and soft start of the dc-dc stage of the BBU module. The soft-start time interval has direct impact on the HUT, similar to the transition time in an off-line ac UPS case. With soft start disabled, an ac fault signal can activate the BBU output stage without any additional time delays.

Typically, PSU failure detection can be provided in a few microseconds, either by monitoring pulses generated at the filter input or by using a fast comparator monitoring the PSU module's "local" (self) voltage level, which is much faster than the detection of an ac fault, which usually takes milliseconds to detect. This means that in the PSU failure cases, "instantaneous" BBU activation would allow the system to maintain uninterruptable operation and safe replacement of a faulty PSU module even in the event of its hard failure.

Let's consider opportunities to modify the power delivery architecture to accelerate both activation of the dc stage and ac fault detection, i.e. shortening dc stage wake-up and ac fault detection time intervals.

Accelerating DC Stage Wake-Up

Any regulated power converter incorporates an output LC-filter as an integral element pulling out the dc component from a voltage signal input with both ac and dc components. Ramping up filter inductor current or capacitor voltage at initial start-up of the converter is associated with an increase of the energy stored in these components. This cannot be done instantly, because such an action would require a source of an infinite power which is not physically realizable.

Even accelerating the charge of LC-filter components can lead to large transients that can overstress the converter's active components. That is why conventional PSUs use a so-called soft start, which produces a gradual increase of pumped energy over time. Actually, the soft start spreads in time additional energy needed to charge output filter caps and to smooth the process of resonant energy exchange between the filter components.

Normally, the soft start time exceeds the output LC resonant ac cycle by an order of magnitude and a typical converter transition into steady state takes up to a few tens of milliseconds. However, in already energized systems with a redundant or backup power architecture this obstacle can be overcome with a capacitor pre-charge method used in cold redundant power distribution arrangements.[1]

A cold redundancy technique[1] can also be employed in the BBU wakeup case, allowing for "instantaneous" redundant power supply wake up using an active PSU "dc fault" signal. The cold redundancy method is based on the concept that output capacitors are pre-charged to their steady-state voltage levels either from a common bus or other active low-power source. In this non-resonant case, the soft start (gradual duty cycle increase) is not required, as only the filter inductor would need to be charged to the current matching the current consumed by the load. Let's evaluate how much time would be required to charge the filter inductor to the maximum load current $I_{LOAD.MAX}$.

The process of inductor current ramping for this case is shown in Fig. 3. In the first stage of this process, voltage pulses v_{in} (blue waveform) with maximum duty cycle are being generated at the output filter input. Once the inductor current i_L reaches the load current level, the feedback loop adjusts the pulse duty cycle to its nominal value.

Assuming the voltage pulse magnitude $V_{in.m}$ generated at the filter input and dc voltage V_o at its output remain unchanged during the pulse time, and neglecting secondary-side losses, allows us to linearize the inductor current ramps. This simplifies the evaluation without diminishing its accuracy in determining the ramp time.

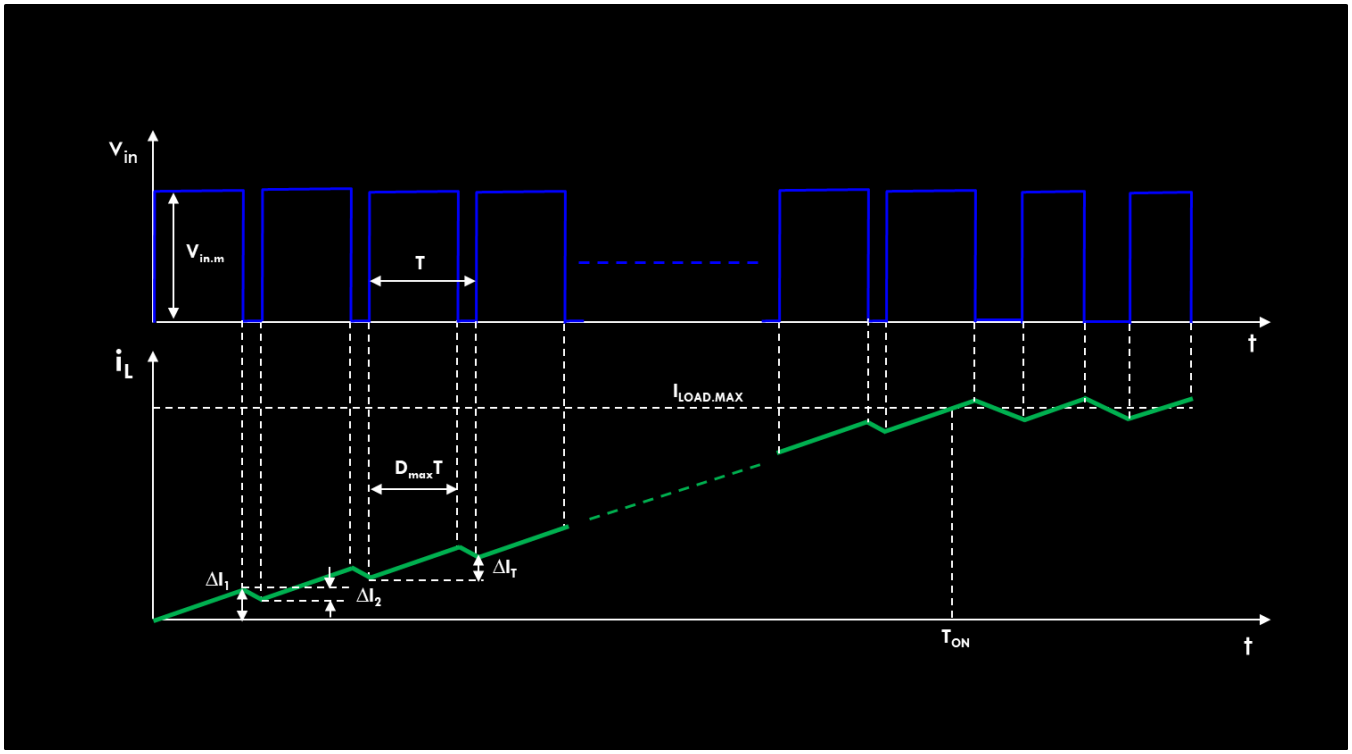

Fig. 3. PSU (or dc-dc converter) output filter inductor current ramp when output caps are precharged. At the first stage of this process maximum duty voltage pulses v_{in} (blue waveform) are being generated at the output filter input. Once the inductor current i_L reaches the load current, the feedback loop adjusts the pulse duty cycle to its nominal value.

Using expressions for current change when voltage v_{in} at the filter input is high:

$$\Delta I_1 = \frac{(V_{in.m} - V_o) T D_{max}}{L},$$

and low (freewheeling time interval):

$$\Delta I_2 = \frac{V_o T (1 - D_{max})}{L},$$

we can write the following equation for a current change over one full cycle:

$$\Delta I_T = \Delta I_1 - \Delta I_2 = \frac{(V_{in.m} D_{max} - V_o) T}{L},$$

where L is filter inductance, T is pulse frequency cycle (typically equal to a half of switching frequency cycle), and D_{max} and maximum pulse duty cycle (with feedback loop inactive).

Assuming a standard inductor current pk-pk ripple $\Delta I_1 = 0.1 I_{LOAD.MAX}$ [4] let's determine how many switching cycles N will be needed for the inductor current to reach the $I_{LOAD.MAX}$ level. Dividing down $I_{LOAD.MAX}$ by ΔI_T and assuming that in a steady state with an active feedback loop, the output voltage will be determined by the nominal duty cycle: $V_o = V_{in.m} \cdot D_{nom}$ we find:

$$N = \frac{I_{LOAD.MAX}}{\Delta I_T} = \frac{10 \Delta I_1}{\Delta I_T} = \frac{10 D_{max} (1 - D_{nom})}{D_{max} - D_{nom}} = \frac{10 (1 - D_{nom})}{D_{max}/D_{nom} - 1}$$

As it can be seen from this equation, the more that duty cycle can be increased over D_{nom} the lower the value of N and the shorter the inductor charge time is going to be. To compensate for the bulk cap voltage drop, shown in Fig. 2 for the reduced HUT case (2ms), the duty cycle D needs to have at least 2% expansion over nominal. That is, for the worst case we can assume that D_{max}/D_{nom}= 1.02 and evaluate the required N based on this assumption. The graph for N is shown in Fig. 4.

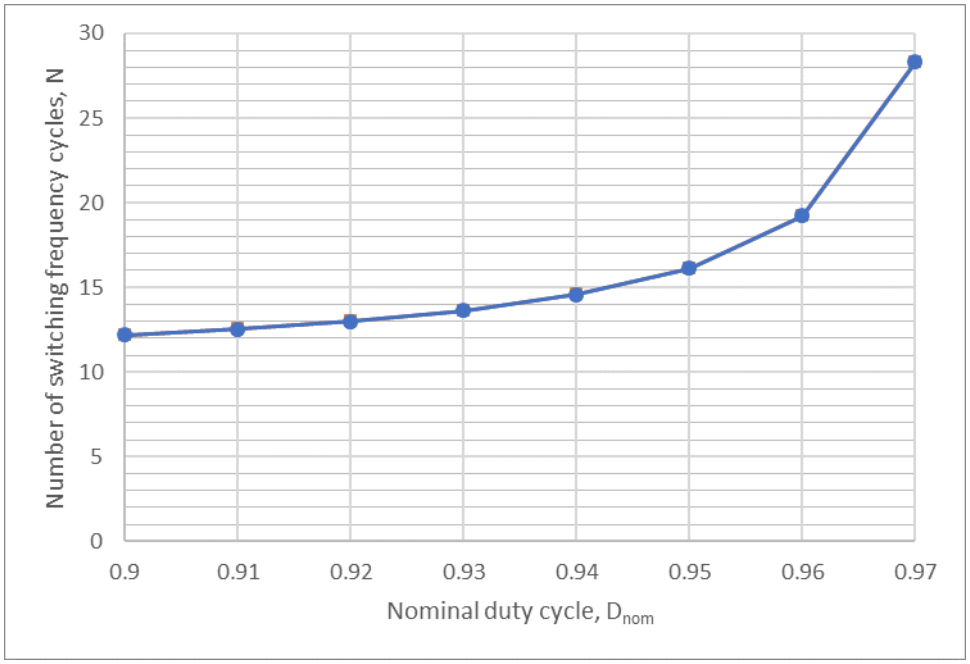

Fig. 4. Number of pulses (switching cycles) at the dc-dc converter output filter input required to make the PSU fully active in supplying maximum load current without soft start (D_{max}/D_{nom}= 1.02) vs. nominal duty cycle. At maximum practical $D_{nom} = 0.97$ the dc-dc stage can be activated in less than 30 cycles of the pulse frequency at the LC filter input.

Considering that the effective pulse frequency at the filter input gets doubled in a full-wave rectifier, typically used in high efficiency PSU designs, even with conventional silicon MOSFETs operating at a switching frequency of 100 kHz it can be concluded that at the maximum practical $D_{nom} = 0.97$, the dc-dc stage can be activated in less than 150 µs.

Fast AC Fault Detection

Since the PFC stage of a PSU operates in a wide range of instantaneous ac line voltage levels, the ac voltage sags that do not reach zero may represent a thermal or input fuse overstress issue. If the detection time of those sags does not exceed a few tens of milliseconds, such overstresses won't occur, and a detection time not exceeding, say, a period of line frequency can be considered acceptable.

In the case when the input voltage drops to zero, the inlet energy supply gets interrupted, and the required V_{cc} level at the dc-dc converter input is provided only by the bulk capacitor. To minimize the bulk capacitor voltage dip (Fig. 2), the ac fault detection needs to be provided in the shortest possible time.

One of the efficient methods of fast ac fault detection was used in a so-called SmaRT technique described in reference [2]. The SmaRT (smart ride through) technique was originally introduced for easing the server power supply's ac dropout ride-through condition and minimizing the PSU bulk cap size.

The ac fault detection in the SmaRT application is illustrated in Fig. 5. It is based on comparison of the rectified instantaneous ac voltage with a detector dc threshold V_t and generating a logic signal when the comparator pulse duration exceeds a predetermined time. In our case, once the comparator pulse duration exceeds:

$$T_{max} = \frac{2\sin^{-1}V_t/V_m}{2\pi f},$$

where V_m is the ac voltage magnitude and f is the line frequency, the enabling UPS signal can be generated.

The lower the V_t level, the faster the ac fault can be detected. In real applications, for noise immunity V_t can be reliably set within 5% to 10% of the lowest operating voltage magnitude. So, assuming the worst-case V_t/V_m = 0.1 and min line frequency f_{min} = 47 Hz, we find that T_{max} = 0.678 ms, so the determined T_{max} value can be considered the maximum time of ac dropout detection.

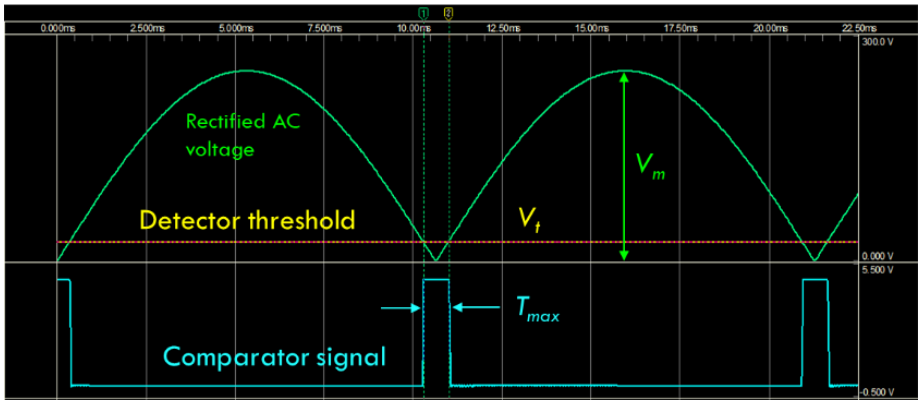

Fig. 5. AC fault detection. Once the comparator signal duration exceeds T_{max}, the signal for enabling the UPS can be generated.

Adding up the worst-case ac fault detection and wake-up time intervals (0.678 + 0.15 = 0.828 ms) we can conclude that the UPS wake-up process with some architecture modifications (which will be discussed later) could be executed in less than 1 ms.

Potential (Expected) Benefits

To evaluate the potential benefits of the UPS with the accelerated wake-up process versus conventional UPS cases, let's compare typical industry HUT requirements, which are a half and a full cycle of the lowest ac line frequency, to the decreased HUT case. Adding a 1-ms margin for the PWOK warning time[5] (PWOK is the signal preventing server board operation at improper supply voltages) we will be comparing the best conventional HUT case (a half cycle) with the accelerated fault detection/wakeup case.

Thus, the following two conditions will be compared: HUT1 = 12 ms, HUT2 = 2 ms. These cases are marked with blue dashed lines in Fig. 2 along with a 22-ms case shown for reference. Using Eqn (1) and assuming that in the ZVS converters, used in high-efficiency PSU designs, conduction losses dominate, and that the on-resistance of a MOSFET is proportional to the blocking voltage raised to the 2.6 power,[6] we can compute the projected P_{loss} reduction factors for different components under different values of C_s. These numbers are given in Table 1.

Table 1. Calculating P_{loss} reduction factors for different components given a reduction in HUT from 12 ms to 2 ms.

Specific bulk capacitance	1 µF/W	0.7 µF/W
Synchronous rectifier reverse voltage, MOSFET current and primary winding current reduction	1.065	1.115
SR on-resistance and power loss reduction	1.208	1.326
Primary power loss reduction	1.135	1.243

To gauge the potential efficiency improvement let's use a Titanium-class efficiency PSU with HUT = 1/2 ac cycle as a baseline. The data is given in Table 2.

Table 2. Comparing the efficiency improvements obtained with the accelerated wake-up process versus the conventional case.

PSU	Primary-side impacted losses	Secondary-side impacted losses	Not impacted losses	Total losses	DC-DC efficiency	PFC efficiency	PSU efficiency	Efficiency improvement
Original, HUT = 12 ms	3.025%	2.750%	1.375%	7.150 %	93.33%	98.20%	91.647%	-
With HUT = 2 ms @ Cs = 1 µF/W	2.666%	2.277%		6.318 %	94.06%		92.364%	0.717%
With HUT = 2 ms @ Cs = 0.7 µF/W	2.281%	2.073%		5.729 %	94.58%		92.879%	1.232%

This data shows noticeable efficiency improvements (0.7% to 1.2%), which are more clearly reflected in the PSU loss reduction—6.3% vs. 7.15% (11.6% reduction for C_s = 1 µF/W) and 19.9% reduction for C_s = 0.7 µF/W. Such improvements would allow for significant reduction in power supply cost and size.

It has to be stated that the improvement can be achieved with BBU architecture modifications alone, and does not include usage of 277-Vac line, GaN components, which could allow further shortening of dc-dc stage wake-up time and provide additional efficiency improvements. Understandably, as compared with the one-cycle HUT baseline (see graphs in Fig. 2) accelerated UPS wakeup can provide much greater efficiency improvements.

Enhanced Architecture Options

Ac fault and dc fault signals can be used in a variety of power delivery arrangements when battery and bus voltages are different, so buffer dc-UPS modules need to be accommodated between the battery and the bus. Two typical high- and low-voltage application examples are shown in Fig. 5.

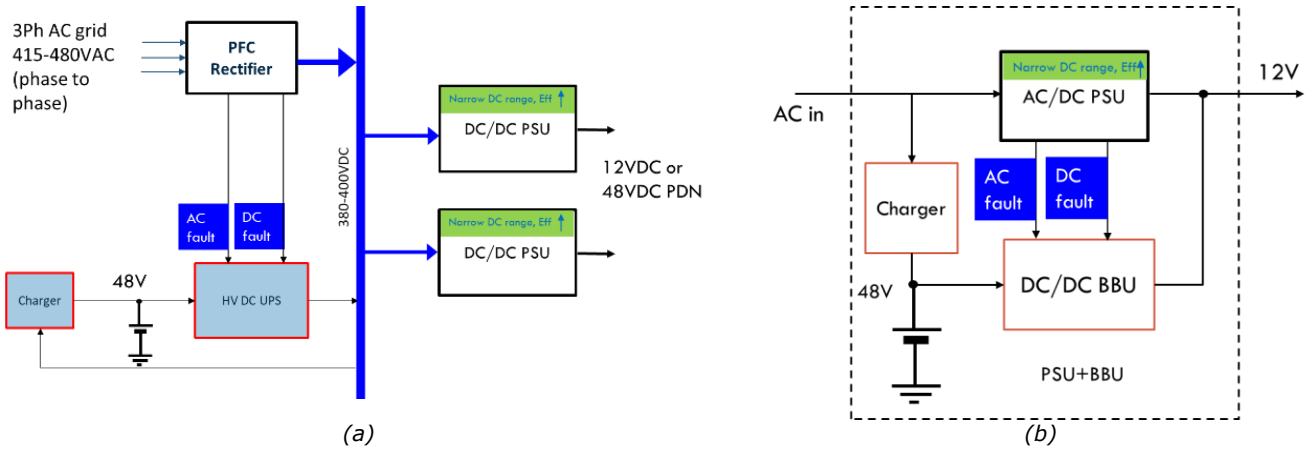

Fig. 6. Accelerated BBU wakeup architecture examples for high-voltage (a) and low-voltage (b) applications.

In Fig. 6a, a PFC rectifier forming high-voltage power distribution network having fast ac fault and dc fault links to dc UPS allows use of dc-dc PSUs with a narrow supply voltage range. It allows activation of the BBU in case of an ac grid fault or a PFC rectifier fault. Similarly, in Fig. 6b, fast ac and dc fault signals provide accelerated dc-dc BBU wakeup and uninterruptible power flow from a 48-V battery to a 12-V PDN, while the main ac-dc PSU can operate with a narrow PFC voltage range and have a higher efficiency.

In many cases a dc fault can be the result of an ac failure. This means that generally only one dc fault signal can be used for a dc UPS activation. However, having an ac fault link provides more transition time margin at typical system loads below maximum or when system load throttling mechanisms such as SmaRT are enabled. Such margin guarantees the smoothest transition to the backup power source because in these cases the UPS becomes fully active when PDN voltage remains at its nominal level.

Conclusions

Using ac fault detection and activating BBU module methods developed for SmaRT and cold redundancy power supply architectures allows significant shortening of the wake-up time of a dc UPS. Accelerating the UPS wake-up process, in turn, creates an opportunity for significant power loss reduction and efficiency improvements.

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Viktor Vogman currently works at Power Conversion Consulting as an analog design engineer, specializing in the design of various power test tools for ac and dc power delivery applications. Prior to this, he spent over 20 years at Intel, focused on hardware engineering and power delivery architectures. Viktor obtained an MS degree in Radio Communication, Television and Multimedia Technology and a PhD in Power Electronics from the Saint Petersburg University of Telecommunications, Russia. Vogman holds over 50 U.S. and foreign patents and has authored over 20 articles on various aspects of power delivery and analog design.

For more information relating to UPS designs, see How2Power's Design Guide, locate the Power Supply Function category and select UPSs.