ISSUE: December 2019

Integrated Current Limiter Eases Power Protection In High-Voltage Space Applications

by Salvo Pappalardo, STMicroelectronics, Milan, Italy and Ignazio Mirabella, STMicroelectronics, Catania, Italy

Latched current limiters (LCLs) have been extensively used in the aerospace environment, especially in the European institutional missions and for many years have been the fundamental power protection devices in earth observation satellites. In addition, in recent years, LCLs have increasingly being proposed as a viable alternative to fuses for protection in commercial telecommunication satellites. Or, when the fuse is made mandatory, LCLs offer a means of protecting the fuse, thus avoiding a single overcurrent event that forces the switch to redundant equipment. From this perspective, the development, qualification and availability in the aerospace market of an integrated current limiter is significant.

The LCLs are power distribution and protection devices, several of which are typically used in a solid-state protection (SSP) system. Historically, based on the state-of-the-art, they were typically realized as solid-state switch devices used for bus protection purposes in case of excessive current demands from the load/users side.

However, nowadays, even if the functionality and the main performance requirements of these LCLs do not change from one project to another, they are routinely redesigned and implemented using discrete components. Obviously, an integration of certain key LCL functions could reduce or eliminate such redesigns, while also providing cost and size savings. This opportunity was recognized by the ESA[1], which proposed development of an integrated current limiter of universal use and containing most of the components required for the relevant current limiter functions (such as the latching and retriggerable modes), in order to avoid the repeated redesign and implementation using discretes.

The ESA's proposal gave rise to the RHRPMICL1A IC, a rad-hard integrated current limiter (ICL) designed and developed by STMicroelectronics. This device has been recently qualified to the QML-V standard for radiation hardness with SMD number 5962-17211. The high-voltage application solution, presented in the final section of this article, allows its use in a power bus of 100 V or higher, such as those required more and more in satellites (mainly telecom).

This article provides a brief overview of the main features embedded in the RHRPMICL1A, describes circuit-level details of how to use the device in the intended applications, and presents some experimental results demonstrating its performance. Readers will find more detailed technical descriptions of the RHRPMICL1A device along with exhaustive application tests in references [2] and [3]. Such tests demonstrate that the RHRPMICL1A embeds the most important features that an ICL device should have.

Overview Of Device Features And Operation

The RHRPMICL1A is a versatile device that can be configured in latched, retriggerable or foldback current mode, through the proper setting of a few configuration pins. Fig. 1 shows a typical application circuit in which the ICL device is embedded.

From an application point of view, the RHRPMICL1A is part of an SSP architecture in a power conversion and distribution unit (PCDU) and it is placed between the main supply bus (labeled "SUPPLY BUS" in Fig. 1) and the relevant loads, driving an external p-channel power MOSFET, the switch element. It is worth emphasizing that both the switch and the current sensing R_{SENSE} elements are placed upstream of the supplied loads and not on the return power line. This generally represents a mandatory requirement if the ICL power output is distributed outside the unit containing the ICL itself, as in the case of Fig. 1. That's done to protect the power output lines against accidental short circuits to ground caused by failures in the connectors, in the harness or in the supplied load.[4]

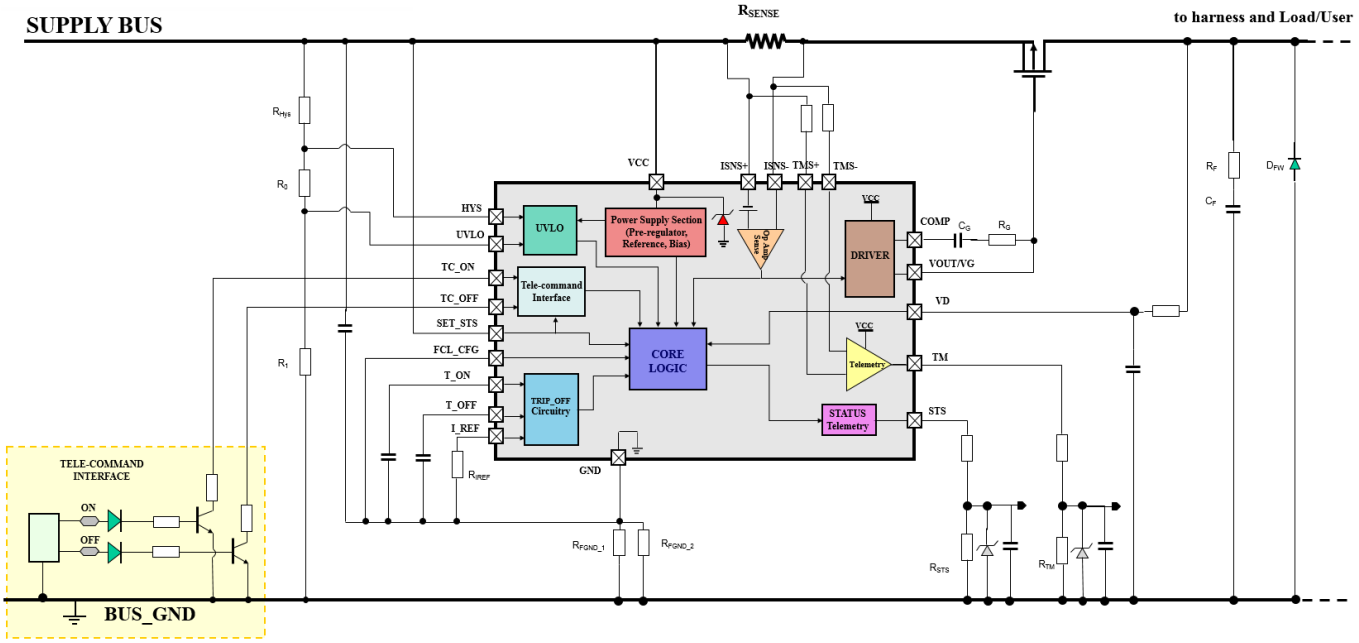

Fig. 1. An RHRPMICL1A application circuit.

The core of the RHRPMICL1A is represented by the current limiting and the driving circuits designed for driving an external p-channel power MOSFET connected in high-side configuration. Current sensing, current limit detection, analog and digital telemetries and some protection functions are also embedded, resulting in a smart device suitable for high-reliability systems (see Fig. 2).

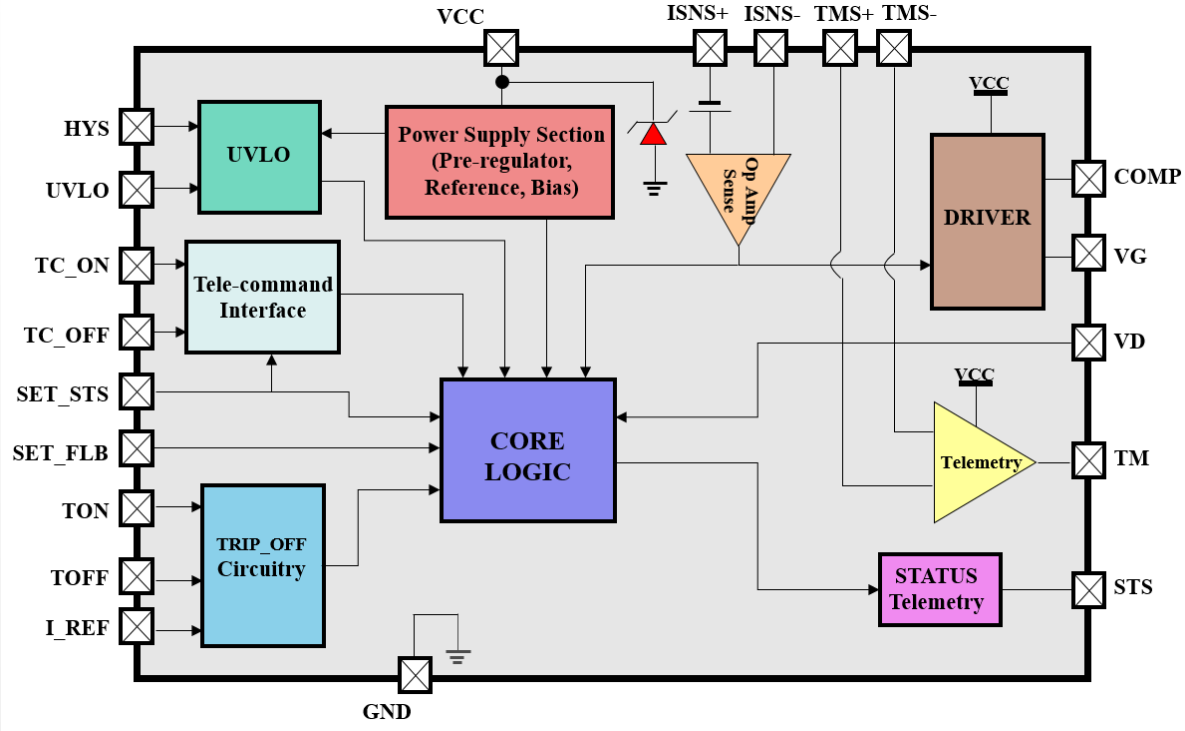

Fig. 2. The RHRPMICL1A block diagram.

One of the most important features of this device is its ability to operate "floating ground". This is done by means of resistor R_{FGND}, which decouples the device ground reference GND from the ground system reference BUS_GND, and by the integrated voltage clamp (shown in red in Figs. 1 and 2, whose typical value $V_Z \sim 14.8$ V), according to the schematic of Fig. 1 and as explained in more detail in references [2] and [3].

This key feature allows the RHRPMICL1A to be connected to the hot line of the power bus without requiring implementation of the device in a high voltage (HV) semiconductor process technology, especially if the power MOSFET is not embedded in the ICL device (as is the case with the RHRPMICL1A). Nevertheless, even if the silicon technology used is able to sustain high-voltage values, the floating ground functionality is mandatory because it is not possible to exclude a potential short circuit failure of the VCC supply line (i.e. the main supply bus) vs. GND inside the IC device. This kind of failure is not acceptable in aerospace systems as it would result in a short circuit of the main supply bus to BUS_GND that could compromise the mission.

In case a short occurs inside the device, the resistor R_{FGND} will sustain the voltage stress rather than the ICL device. So this resistor has to be sized properly to be able to dissipate the power level determined by the steady-state value of the supply bus.

The RHRPMICL1A device can be turned on/off by means of two external dedicated and independent command signals (with separated paths), coming from a Tele-command Interface (see Figs. 1 and 2) referred to the ground reference of the system. This system ground is called BUS_GND here in order to distinguish it from GND, which is the ground of the RHRPMICL1A device.

In addition, the behavior of the device is always reproducible and well defined during the main bus start-up, as the device might be required to be either in off or on status at first turn-on of the main supply bus, according to specific PCDU manufacturer needs. This feature is achieved by means of the configuration pin SET_STS. When the device is configured On at start-up (pin SET_STS connected to VCC), it is not necessary to send the On command from the Tele-command Interface and the device is ready to drive the external power MOSFET as soon as the main supply bus reaches the turn-on threshold V_{TH_ON} (Fig. 3.)

On the other hand, when the device is configured Off at start-up (pin SET_STS connected to GND), after the main supply bus will have reached the V_{TH_ON} threshold, the device remains in the off state (Fig. 4). In this case, it is mandatory to send the On command from the Tele-command Interface to switch the device On, so that it can properly drive the external power MOSFET.

An embedded UVLO circuit, whose only aim is to protect the device against incorrect bias conditions, establishes the threshold voltage levels for the connection (V_{TH_ON}) and disconnection (V_{TH_OFF}) of the RHRPMICL1A. The values of both thresholds can be set independently by means an external resistor divider connected between the main supply bus and the BUS_GND (see Fig. 1), in order to cope with different input undervoltage requirements depending on the particular application and loads types.

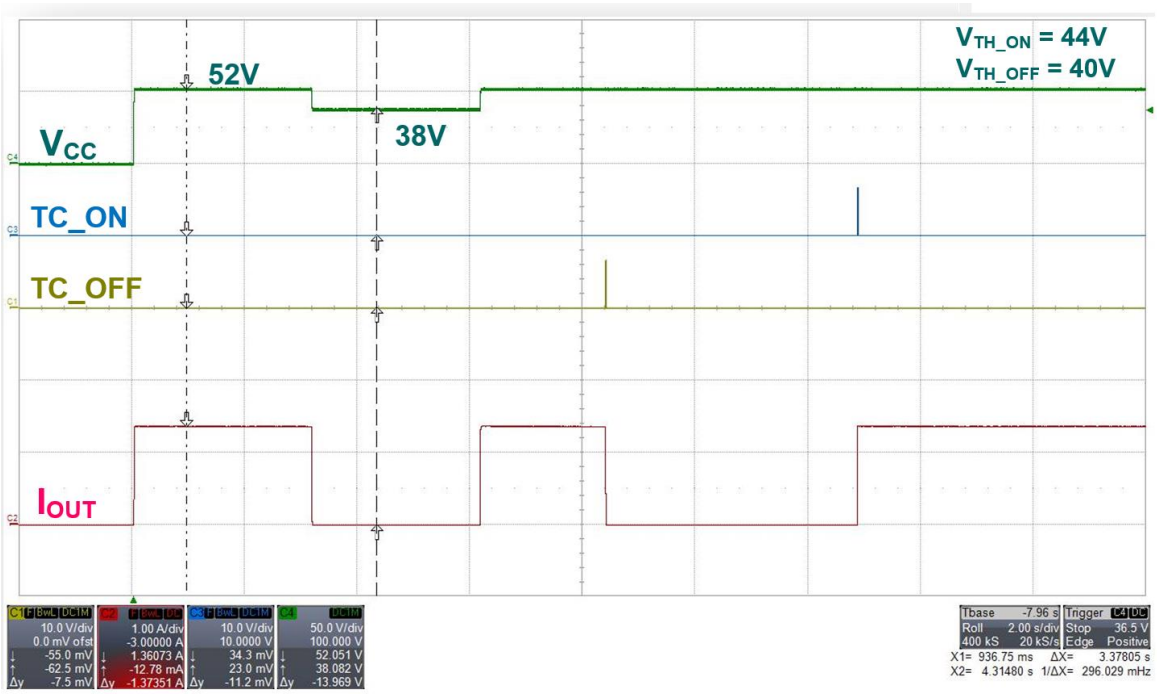

Fig. 3. RHRPMICL1A configured On at start-up.

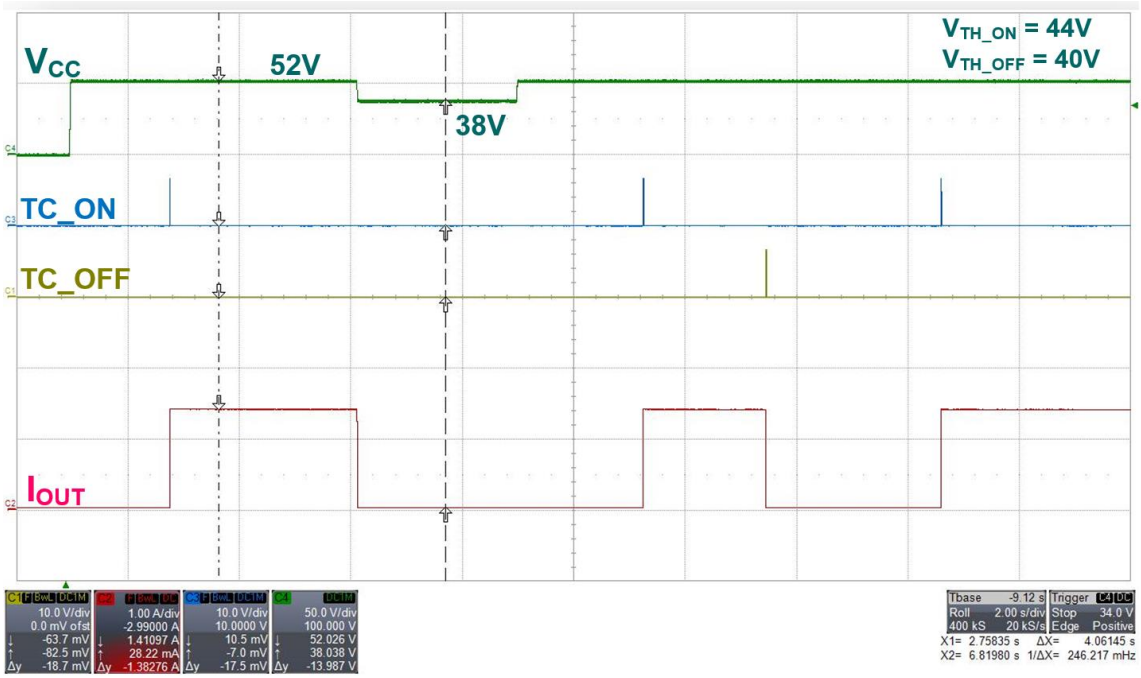

Fig. 4. RHRPMICL1A configured Off at start-up.

Another key feature is represented by the current limiting function which is managed by the trip-off circuitry. This circuital section allows safe thermal operation of the power MOSFET when a current limiting event occurs. When an overcurrent condition is detected, the RHRPMICL1A triggers a timer that will turn off the external MOSFET if the overcurrent condition persists more than the trip-off time T_{ON}. (Though it describes the trip-off

time, T_{ON} is so named because during this time period the device is still On but limiting the current.) This time can be set through an external capacitor C_{ON} connected between pin TON and GND.

For the duration of time T_{ON}, the device will stay in current limiting and after this time is elapsed, the device's behavior will depend on its configuration. If the device is configured in latched mode (i.e. pin TOFF is shorted to GND), once the T_{ON} time is elapsed, the external MOSFET will be latched off and this condition shall be reset by cycling the device. For example, this can be done through the Tele-command Interface or by cycling the device off/on through the UVLO thresholds.

If the device is configured in the retriggerable mode (i.e. external capacitor C_{OFF} is connected between pin TOFF and GND), once the time T_{ON} elapses, the external MOSFET will be turned off only for the duration of another interval T_{OFF} (called the "recovery time"). The value of T_{OFF} can be externally set by properly choosing the value of capacitor C_{OFF}. The recovery time T_{OFF} shall be made larger then T_{ON} in order to allow safe thermal operation of the external power MOSFET. When time T_{OFF} has elapsed, the device will try to restart autonomously. In this manner, if the overcurrent event disappears, the device will be able to restart, recovering its normal operation.

The current limiting value can be externally set by choosing the appropriate value of the sense resistor R_{SENSE}, according to the application requirements. The voltage drop across R_{SENSE} is compared with a fixed 100-mV voltage reference internally generated. If the voltage drop across R_{SENSE} tends to get higher than the internal offset, it means that the current demand by the load is going to overcome the value of current limit set for the specific application. The sensing loop reacts very quickly, minimizing the reaction time and leading the system in current limitation: the embedded timer will start to count-up to the trip-off time T_{ON}.

Finally, the RHRPMICL1A device also embeds two telemetry sections. On pin TM, the analog telemetry provides a voltage that is an exact replica, properly scaled, of the current flowing through the power line. The external resistor R_{TM}, connected between pin TM and BUS_GND, realizes the expected current/voltage conversion.

Meanwhile, on pin STS, the digital telemetry provides a bilevel voltage value (i.e. on/off) providing instantaneous information about the status of the device. An external resistor R_{STS}, connected between pin STS and BUS_GND, converts an internal fixed 100-μA output source current to a fixed voltage in the case where the status of the device is on. If the status of the device is off, the value of the output source current on pin STS will be zero and therefore pin STS will be tied to BUS_GND. Refer to references [2] and [3] for more details.

Operating At High Voltage

Although the "floating ground" feature allows the RHRPMICL1A to be used in applications where the voltage bus is higher than 15 V, constraints of the BCD6s-SOI technology (in which the device is fabricated), impose a maximum voltage limit for the main supply bus. Above this value, the correct operation of this device is no longer guaranteed.

Looking at Fig. 5, it is clear that there are some pins (TC_ON, TC_OFF, VD, TM and STS, highlighted in the colored boxes) that are "indirectly" referred to BUS_GND, the ground path of the main bus. TC_ON and TC_OFF represent the pins directly connected to the Tele-command Interface typically used in the latched configuration mode in order to remotely control the device in On and Off status. VD is the pin connected at the drain of the external power MOSFET and used inside the device for detecting an overcurrent event and consequently for starting the counter of the trip-off time T_{ON}.

As described in the previous section, TM and STS pins represent, respectively, the outputs for the analog and digital telemetries. It is clear that for the relative reference system of the RHRPMICL1A, BUS_GND will be a negative voltage, given that GND is the ground reference (0 V) of the device itself.

Depending on the operating voltage value of the main supply bus, during the different working phases, the voltage values on some of these pins might be even several tens of volts negative with respect to GND, which obviously is also the potential of the silicon substrate for the device. Therefore, particular care has been taken in designing the output stages of these pins, as well as in the architecture of their protection circuits against ESD events, to ensure that the device functionality is not lost if these pins are biased negative with respect to the silicon substrate.

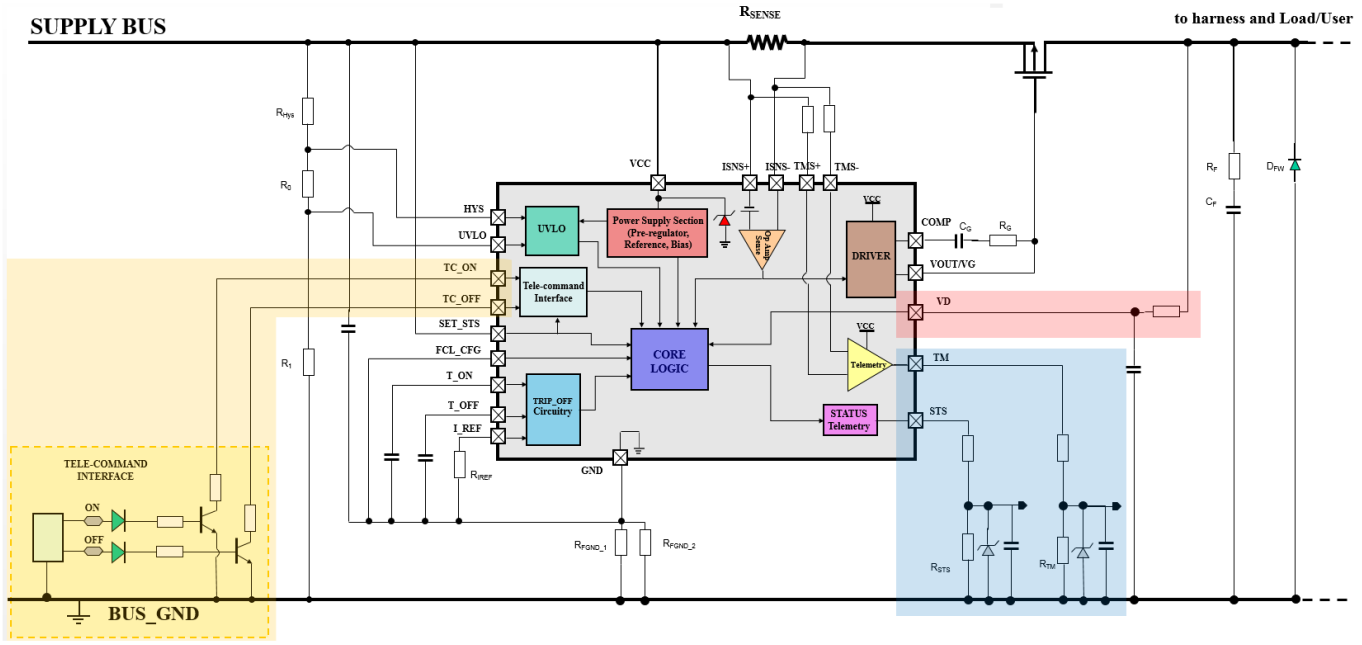

Fig. 5. RHRPMICL1A application diagram: circuit sections referred to BUS_GND.

However, due to the intrinsic structure of the high-voltage elementary components used in the output stage circuits connected to these pins, the vertical voltage limits of the BCD6s-SOI process technology cause the breakdown voltage of these components to be degraded if one of their terminals (in this specific case, the drain terminal) is negative biased at several tens of volts with respect to the silicon substrate. Indeed, in this case, an unexpected and uncontrolled current will begin to flow from these pins down to BUS_GND, thus altering the device functionality connected to the related pins. Moreover, depending on the value of this current, the component itself could be damaged, compromising the correct functionality of the RHPMICL1A within the system in which it is embedded.

For example, when the RHRPMICL1A is working in the normal mode, the VD pin is only a few tens or hundreds of millivolts (the sum of the voltage drop on R_{SENSE} plus V_{DSON} of the power MOSFET) lower than the main supply bus (V_{CC}). Therefore the elementary components embedded in the RHRPMICL1A circuitry work in a standard way. However, when a short-circuit condition occurs downstream (on the load side), the drain terminal of the embedded high-voltage p-channel MOS used in the circuitry (and therefore the pin VD) is tied to BUS_GND. Therefore, this drain terminal will be biased negative with respect to its substrate. In particular, it will be biased at VCC-VZ negative with respect to its substrate.

A detailed characterization of the breakdown voltage BV for the high-voltage p-channel MOS component used in the output stages of the device highlights a degradation of BV when V_{SUB} (the substrate voltage of this component) becomes higher than a voltage threshold. This degradation is greater with decreasing temperature and this phenomenon tends to saturate for V_{SUB} > 120 V.

In the specific case of the RHRPMICL1A, this BV degradation imposes a voltage limit for the value of the main supply bus up to which the device can be used without problems. Taking into account that the embedded Zener clamp voltage is typically ~ 14.8 V, and also the intrinsic process spread of the BCD6s-SOI technology, a safe value for the main bus supply is ~ 90 V to 95 V. Up to this voltage level, the device can operate without a problem over the whole operating temperature range of -55ºC to +125ºC.

To make sure that the RHRPMICL1A can be safely used in applications with a supply bus >90 V, it is necessary to use a few additional external components to guarantee that the above-mentioned pins can never be biased at dangerous negative values. Such values would be those high enough to compromise the correct functioning of the device.

Fig. 6 shows how the typical application circuit of Fig. 1 should be modified for those applications operating from a high-voltage supply bus. Indeed, due to the fact the device has been fully qualified up to VCC = 52 V and no radiation data is available in the range of 52 V to 90 V, it is strongly recommended that designers observe the following guidelines in applications with supply bus values greater than 52 V.

- The values of the pull-down resistors of the Tele-command circuitry shall be properly selected in order to guarantee that pins TC_ON and TC_OFF will never go ~ -37 V with respect to GND, the substrate reference of the device (resulting from ~52 V of supply bus less 15 V of the embedded Zener clamp). Indeed, during the transient transmission of the tele-command signals, it is sufficient to drive these pins just 1 V higher than GND to guarantee that the embedded logic section of the device switches properly, assuring a proper transmission of the tele-command signals inside the device.

- The TM and STS pins, respectively for the analog and the digital telemetries, shall be referred to BUS_GND by means of the external high-voltage p-channel transistors (highlighted in the red circles) connected in cascode configuration, as shown in Fig. 6 (i.e. with their gates connected to GND).

- The VD pin shall be properly clamped (for example through an external Zener diode, as shown in Fig. 6) to avoid this pin being pulled-down to BUS_GND, as occurs when the device is in the off state or in case of a short-circuit event from the load side. The value of the external clamp must be such as to avoid this pin taking negative voltage values lower than ~ -37 V, for the reasons explained above.

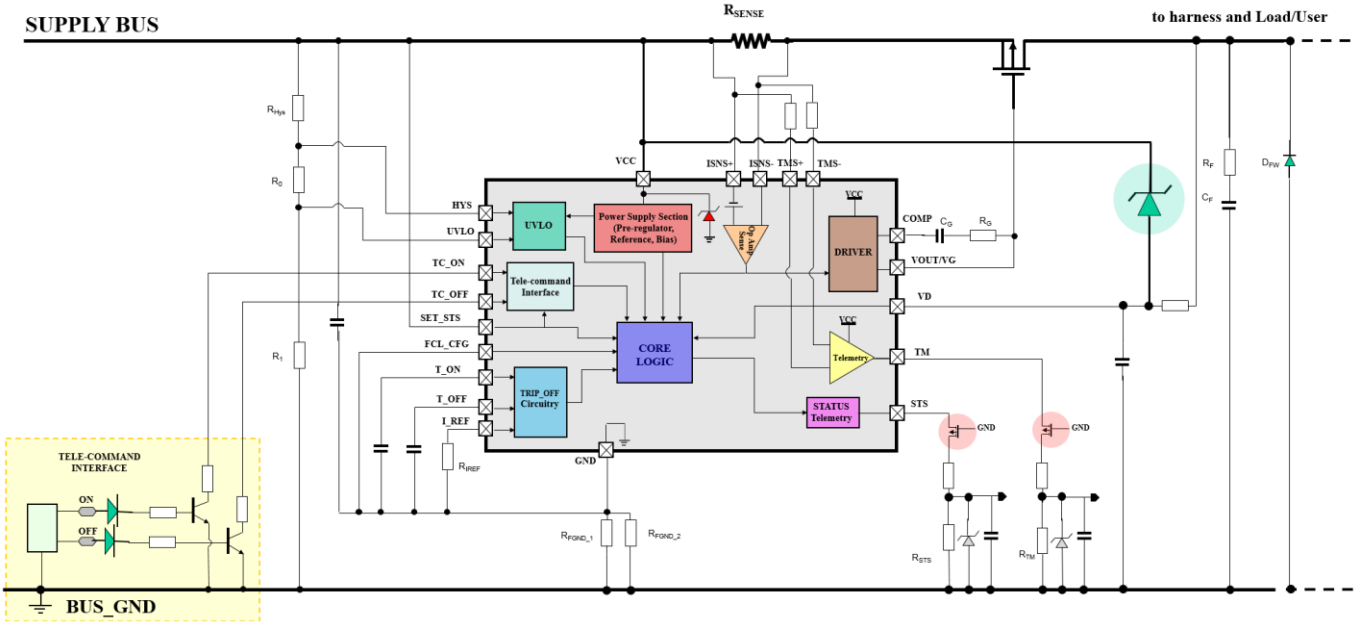

Fig. 6. RHRPMICL1A application circuit for operation at high voltage.

This application solution has been first checked by simulations with positive results and then verified and validated with some application tests in our laboratory. The application board and the equipment used during the high-voltage tests are shown in Fig. 7. All three configuration modes (latched, re-triggerable and foldback) have been successfully tested up to 180 V. But the most demanding case was surely the re-triggerable mode with a permanent short-circuit condition already in place at start-up.

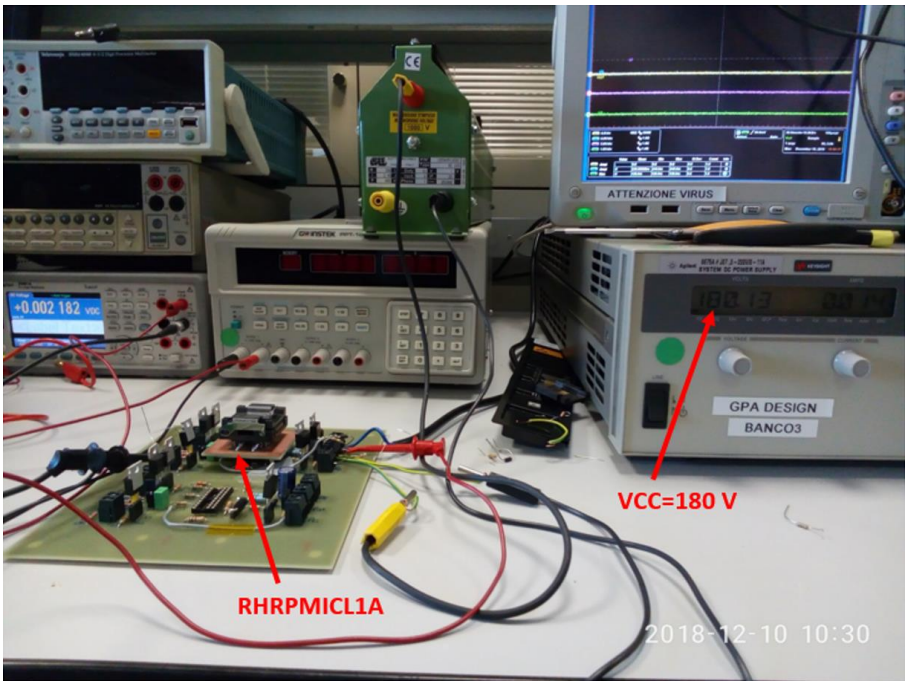

Fig. 7. Equipment set-up for high-voltage application tests.

This case is shown in Fig. 8 where the cyan waveform shows V_{CC} the main supply bus, in this case at 150 V. As it can be seen, the analog and digital telemetries, respectively the magenta and yellow waveforms, behave as expected, even at so high a value for the bus supply. Moreover, these signals correctly follow the dynamic of the power output current flowing through the load. The value of I_{LIM} in this case was set at 2 A.

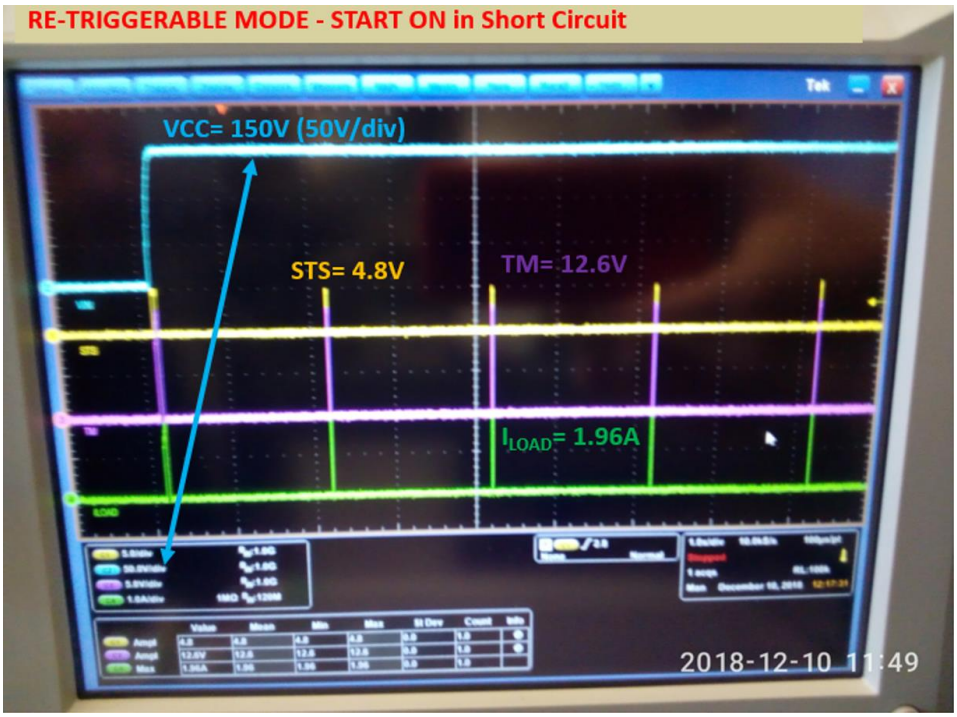

Fig. 8. Operation of the RHRPMICL1A configured in the re-triggerable mode while starting up into a permanent short-circuit and powered from a high-voltage supply bus.

It is important to remark that with this application solution, the RHRPMICL1A no longer limits the maximum value of the main supply bus. The maximum voltage level of the application will be limited mainly by the voltage class of the external p-channel power MOSFET used as a switch element, as well as by the voltage classes of the external components used on the application board. In fact, whatever the value of the main supply bus, it will be enough to properly size the external components to make the RHRPMICL1A continue to work as expected.

Acknowledgment

This paper is dedicated to the memory of Manuel Martin Alfonso, who is missed by all of us. Through his great professionalism, technical knowledge and devotion to work, he was able to create a strong synergy between ESA and STMicroelectronics and made a fundamental contribution to the design and realization of the RHRPMICL1A device.

References

1. ESA Statement of Work (2008) - Invitation to Tender (ITT) AO/1-5784/08/NL/AT.
2. "Integrated Current Limiter" by S. Pappalardo, M.M. Alfonso and I.B. Mirabella, 9th European Space Power Conference (ESPC 2011), June 6-10, 2011.
3. "Integrated Current Limiter: Application Tests" by S. Pappalardo, C. Ribellino, I. Mirabella, M.M. Alfonso and F. Tonicello, 19th European Space Power Conference (ESPC 2014), April 13 -17, 2014, Noordwijkerhout, The Netherlands.
4. Power Distribution by Latching Current Limiters, Source-Load Specification Rationale, Power Conditioning Section, TEC-EPC ESA-ESTEC, Ref. TEC-EPC/2009/500/FT-Dec, 2009.

About The Authors

Salvo Pappalardo is currently the technical office manager for the Space & High Rel Product Line within STMicroelectroncs' GPA & RF division. He first joined this division in 2013 as the Radhard Design Manager, and in the years Salvo held this role he lead the development of several rad-hard products, some of them co-funded by the European Space Agency (ESA). Previously, he served as the coordinator of Analog Group activities, where he was responsible for the Analog Design Team for the Display Division and then for the Photovoltaic business unit, contributing to the development of products by these two groups. Prior to that, Salvo worked for many years as an analog designer at ST, developing MOSFET driver ICs, switched mode power supply and power management ICs for industrial, mobile phone and battery charger applications. He joined ST in 1995, shortly after graduating in electronic engineering. Salvo holds several patents on analog and smart power ICs in the U.S., and he is also author and co-author of papers on ASICs and general purpose ICs.

Ignazio Mirabella is the radiation design expert for the Space & High Rel Product Line within STMicroelectroncs' GPA & RF division. In this role he is a key contributor to the development of devices suitable for operating in the space environment, studying and providing solutions applicable to analog and mixed-signal devices to increase their immunity to single event effects (SEE) and their hardening to TID effects. Previously, Ignazio was a HW design senior engineer in this division, dealing with the development of radiation-hardened devices in the field of STMicroelectronics research programs and in co-funded activities with the ESA. Before that, he worked for ST's R&D department, developing logic devices for the space environment. Ignazio joined STMicroelectronics in 2000 after graduating in electronic engineering in 1999. He holds many patents filed in the U.S. and is co-author of papers presented in conferences and published in journals.

For more on rad hard power components, see How2Power's special section on Space Power.