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PMIC Powers Application-Processor-Based Systems

STMicroelectronics' STPMIC1 power-management IC (PMIC) features four buck converters, a boost converter, and six low-dropout regulators (LDOs) to meet the power demands of highly integrated application-processor-based systems. The chip is optimized as a companion PMIC for ST's STM32MP1 heterogeneous multicore microprocessors, which target a broad range of applications by integrating single or dual Arm Cortex-A7 and Cortex-M4 cores, an optional 3D graphics processing unit, and rich digital and analog peripherals (see the figure).

More than simply saving board space and BOM cost, compared to generating the same number of power rails using discrete components, the STPMIC1 also provides power-rail monitoring and protection, handles power-up/down sequencing, and meets the ST32MP1 accuracy and settling-time specifications. ST Authorized Partner Octavo Systems has used the STM32MP1 and STPMIC1 to create the OSD32MP1x family of microprocessor system-in-package (SiP) devices. These devices are said to occupy a footprint up to 64% smaller than an equivalent system implemented with discrete components while also addressing engineering challenges such as power sequencing.

In addition to supplying power rails for the microprocessor unit (MPU) and external system components, the STPMIC1 also provides a DDR memory reference voltage, a 500-mA USB OTG power switch, and a general-purpose power switch. An I^2C interface and additional pins allow the MPU to manage the PMIC.

The four buck converters in the PMIC are designed for fast transient response and precise output-voltage control to handle a wide range of operating conditions. A pulse-frequency modulation mode boosts energy efficiency at low loads. During normal operation, pulse-width modulation (PWM) synchronization minimizes EMI. The boost converter, with bypass-mode capability, can power up to two USB ports and ensures smooth regulation either when operating from a battery or low-cost 5-V ac-dc adapter.

Among the six LDO channels, one is featured for DDR3 termination and can operate in bypass mode for low-power DDR, while another provides automatic source detection to power a USB PHY. The remaining four LDOs are general-purpose outputs.

An evaluation board, STEVAL-PMIC1K1, is also available, which simplifies prototyping with the STPMIC1. The board is easy to use, with pushbuttons and digital I/Os for triggering the PMIC features, and header connectors for accessing the regulators and switches. A USB dongle is also included for configuring the device registers.

The STPMIC1 is in production now and available in a 5-mm x 6-mm x 0.8-mm, 44-lead WFQFN, priced from $1.70 for orders of 1000 pieces. See the STPMIC1 product page for more information.

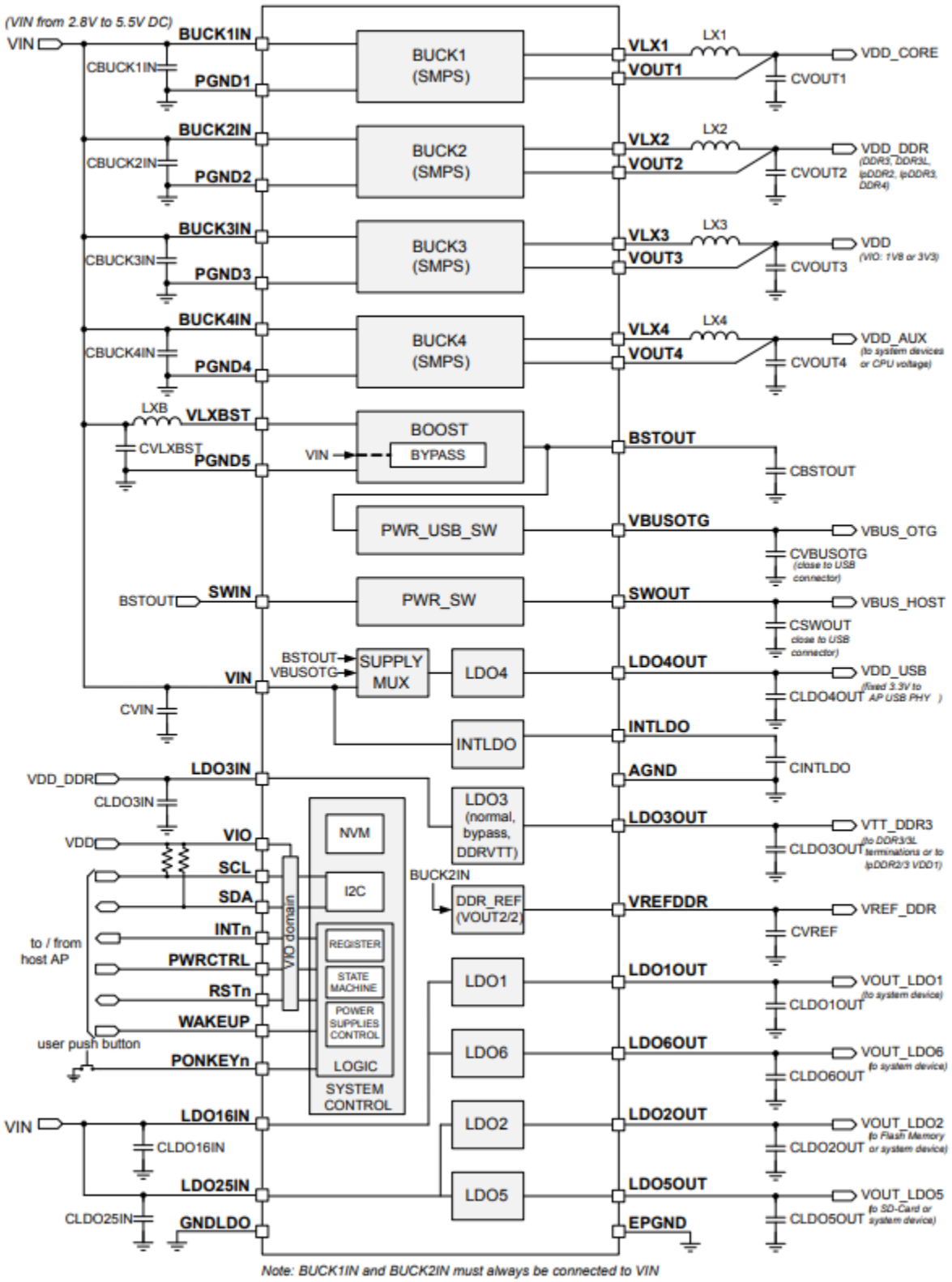

Figure. Housed in a 5-mm x 6-mm x 0.8-mm WFQFN, the STPMIC1 is a fully integrated power management IC designed for products based on highly integrated application processor designs requiring low power and high efficiency. The PMIC's regulators are designed to supply power to the application processor as well as to external system peripherals such as DDR, Flash memories and other system devices. The device integrates advanced low-power features controlled by a host processor via I²C and IO interface.